



ExpressLane PEX 8747-BA/CA 48-Lane, 5-Port PCI Express Gen 3 Switch Data Book

Version 1.1

June 2012

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Revision History

Version	Date	Description of Changes
1.0	March, 2012	Production Release, Silicon Revision BA.
1.1	June, 2012	Production Release, Silicon Revision CA / Production Update, Silicon Revision BA. Changed many register bits from RO to ROS. Changed offsets 700h[0], 704h[0], and 760h[19:17] to Factory Test Only . For Silicon Revision CA, re-purposed offset 760h[16] to enable ECAM access to all PEX 8747 registers. Added register offset F4Ch[28:24]. Applied miscellaneous corrections and enhancements.

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Document Number: 8747-BA/CA-SIL-DB-P1-1.1

Preface

The information in this data book is subject to change without notice. This PLX data book to be updated periodically as new information is made available.

Audience

This data book provides functional details of PLX Technology's ExpressLane PEX 8747-BA/CA 48-Lane, 5-Port PCI Express Gen 3 Switch, for hardware designers and software/firmware engineers. The information provided pertains to both Silicon Revisions (BA and CA), unless specified otherwise.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc., www.plxtech.com
 The [PLX PEX 8747 Toolbox](#) includes this data book and other supporting documentation, *such as* errata, and design and application notes.
- The Institute of Electrical and Electronics Engineers, Inc. (IEEE), www.ieee.org
 - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture*
 - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
 - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
 - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
- Intel Corporation, www.intel.com
 = [PHY Interface for the PCI Express Architecture, Version 2.00](#)
- NXP Semiconductors, ics.nxp.com
 = [The I2C-Bus Specification, Version 2.1](#)
- PCI Special Interest Group (PCI-SIG), www.pcisig.com
 - *PCI Local Bus Specification, Revision 3.0*
 - *PCI Bus Power Management Interface Specification, Revision 1.2*
 - *PCI Code and ID Assignment Specification, Revision 1.2*
 - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
 - *PCI Express Base Specification, Revision 1.1*
 - *PCI Express Base Specification, Revision 2.0*
 - *PCI Express Base Specification, Revision 2.0 Errata*
 - *PCI Express Base Specification, Revision 2.1*
 - *PCI Express Base Specification, Revision 3.0*
 - *PCI Express Card Electromechanical Specification, Revision 2.0*
 - *PCI Express Mini Card Electromechanical Specification, Revision 1.1*
 - [PCI Express Architecture PCI Express Jitter and BER White Paper, Revision 1.0](#)

- Personal Computer Memory Card International Association (PCMCIA), www.pcmcia.org
 - *ExpressCard Standard Release 1.0*
- PXI System Alliance (PXI), www.pxisa.org
 - *PXI-5 PXI Express Hardware Specification, Revision 1.0*
- SBS Implementers Forum, smbus.org
 - *System Management Bus (SMBus) Specification, Version 2.0*

Note: In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.

Abbreviation	Document
<i>PCI r3.0</i>	<i>PCI Local Bus Specification, Revision 3.0</i>
<i>PCI Power Mgmt. r1.2</i>	<i>PCI Bus Power Management Interface Specification, Revision 1.2</i>
<i>PCI-to-PCI Bridge r1.2</i>	<i>PCI to PCI Bridge Architecture Specification, Revision 1.2</i>
<i>PCI Express Base r1.1</i>	<i>PCI Express Base Specification, Revision 1.1</i>
<i>PCI Express Base r2.0</i>	<i>PCI Express Base Specification, Revision 2.0</i>
<i>PCI Express Base r2.1</i>	<i>PCI Express Base Specification, Revision 2.1</i>
<i>PCI Express Base r3.0</i>	<i>PCI Express Base Specification, Revision 3.0</i>
<i>PCI ExpressCard CEM r2.0</i>	<i>PCI Express Card Electromechanical Specification, Revision 2.0</i>
<i>PCI ExpressCard Mini CEM r1.1</i>	<i>PCI Express Mini Card Electromechanical Specification, Revision 1.1</i>
<i>IEEE Standard 1149.1-1990</i>	<i>IEEE Standard Test Access Port and Boundary-Scan Architecture</i>
<i>IEEE Standard 1149.6-2003</i>	<i>IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions</i>
<i>I²C Bus v2.1</i> <i>I2C Bus v2.1^a</i>	<i>The I²C-Bus Specification, Version 2.1</i>
<i>SMBus v2.0</i>	<i>System Management Bus (SMBus) Specification, Version 2.0</i>

- a. Due to formatting limitations, the specification name may appear without the superscripted “2” in its title.

Terms and Abbreviations

The following table lists common terms and abbreviations used in this data book. Most terms and abbreviations defined in the *PCI Express Base r3.0* are generally not included in this table.

Terms and Abbreviations	Definitions
8b/10b	Data-encoding scheme used on data transferred across a Link that is operating at either Gen 1 or Gen 2 Link speed (2.5 or 5.0 GT/s, respectively).
128b/130b	Data-encoding scheme used on data transferred across a Link that is operating at Gen 3 Link speed (8.0 GT/s).
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge data packet receipt. A signal that acknowledges signal receipt.
AHB	Advanced High-Performance Bus.
ARI	Alternative Routing-ID Interpretation.
ARP	Address Resolution Protocol.
ATT	Attenuator.
BAR	Base Address register.
BER	Bit error rate.
BIST	Built-In Self Test.
CDR	Clock and Data Recovery.
CMU	Clock Management Unit.
CRC	Cyclic Redundancy Check.
CSR	Configuration Space register.
Data Beat	Single data transfer in a single clock period.
DFE	Decision Feedback Equalization. Optionally added to a Receiver to improve the signal.
DLL	Data Link Layer.
Downstream Device	Device that is connected to a Downstream Port.
Downstream Port	Port that is used to communicate with a device below it in the system hierarchy. A switch can have one or more Downstream Ports.
DRI	<i>Data Rate Identifier</i> field in Training Sets.
ECC	Error-Correcting Code.
ECRC	End-to-end Cyclic Redundancy Check.
EDB	TLP framing symbol used in place of an END symbol to indicate that the TLP is bad.
EIES	Electrical Idle Exit Sequence.
EIOS	Electrical Idle Ordered-Set.
Electrical Idle	Transmitter is in a High-Impedance state (+ and - are both at common mode voltage).
EP	Endpoint.
FC	Flow Control.
Field	Multiple register bits that are combined for a single function.
FTS	Fast Training Sequence.

Terms and Abbreviations	Definitions
Gen 1	<i>PCI Express Base r1.1</i> and below. Link transfer rate of 2.5 GT/s.
Gen 2	<i>PCI Express Base r2.1</i> . Link transfer rate of 5.0 GT/s.
Gen 3	<i>PCI Express Base r3.0</i> . Link transfer rate of 8.0 GT/s.
GPIO	General-Purpose Input/Output.
GPU	Graphics Processing Unit.
GT/s	Giga-Transfers per second.
INCH	Ingress Credit Handler.
ISR	Interrupt Service Routine.
Lane	Bidirectional pair of differential PCI Express I/O signals.
LCRC	Link Cyclic Redundancy Check.
LFSR	Linear Feedback Shift register.
Link	Active connection between two Ports.
Local	Reference to PCI Express attributes (<i>such as</i> credits) that belong to the PCI Express Station.
LTSSM	Link Training and Status State Machine.
LVDS	Low-Voltage Differential Signaling.
MPS	Maximum Payload Size.
NACK	Negative Acknowledge. Used in the SMBus-related content.
NAK	Negative Acknowledge.
N_FTS	Number of Fast Training Sequences field in Training Sets.
NOP	No Operation.
OS	Ordered-Set.
P2P	Peer-to-Peer or PCI-to-PCI (as identified at point of use).
PCH	Intel Platform Controller Hub.
PCI Express Station	Functional unit that provides the PCI Express conforming system interface. Includes the Serializer/De-Serializer (SerDes) hardware interface modules and PCI Express interface, which provides the Physical Layer (PHY), Data Link Layer (DLL), and Transaction Layer (TL) logic.
PCS	Physical Coding Sublayer.
PEC	Packet Error Code.
PEX	PCI Express.
PHY	Physical Layer.
PIPE	PHY Interface for PCI Express architecture.
PLL	Phase-Locked Loop.
PM	Power Management.
PMA	Physical Media Attachment layer.
PME	Power Management Event.
PN	Port Number.
Port	Interface to a group of SerDes and supporting logic that is capable of creating a Link, for communication with another Port.
Port ID	Number, assigned in hardware, that associates a SerDes with a Port.

Terms and Abbreviations	Definitions
P-P	PCI-to-PCI.
PRBS	Pseudo-Random Bit Sequence.
QoS	Quality of Service.
RAS	Reliability, Availability, and Serviceability.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RR	Round-Robin scheduling.
Rx	Receiver.
SATA	Serial ATA. Computer bus interface used for connecting Host Bus adapters to mass storage devices, <i>such as</i> hard disk and optical drives.
SerDes	Serializer/De-Serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to Lane pads.
SMBus	System Management Bus.
SN	SerDes Number.
SPI	Serial Peripheral Interface.
SSC	Spread-Spectrum Clock.
Station	Logic block that implements the PCI Express function, bounded by the external pins of the differential Transceivers and the interface to the internal switch fabric.
Sticky Bits	Register bits in which the current values are unchanged by a Hot Reset, Link Down event or a Secondary Bus Reset, while the switch is powered. Sticky bits are reset to default values by a Fundamental Reset. HwInit, ROS, RWICS, and RWS CSR types. (Refer to Table 11-4, “Register Types, Grouped by User Accessibility,” for CSR type definitions.)
Sticky State	Condition that causes a state machine to be stuck in a particular state, unable to make forward progress.
TC	Traffic Class.
TCB	Training Control Bits field in Training Sets.
TDM	Time Division Multiplex.
TL	Transaction Layer.
TLC	Transaction Layer Control. The module performing PCI Express Transaction Layer functions.
TLP	Transaction Layer Packet. PCI Express packet formation and organization.
TS	Tri-statable Output (High-Impedance when output is not driven). (Used in Chapter 3, “Signal Ball Description,” in the Type column of the Signal tables.)
TS	Training Sequence.
TS1	Type 1 Training Sequence Ordered-Set.
TS2	Type 2 Training Sequence Ordered-Set.
Tx	Transceiver.
UDID	Unique Device Identifier.
UI	Unit Interval – 400 ps at 2.5 GT/s, 200 ps at 5.0 GT/s, 125 ps at 8.0 GT/s.
Upstream Device	Device that is connected to the Upstream Port.
Upstream Port	Port that is used to communicate with a device above it in the system hierarchy.
UTP	User Test Pattern.

Terms and Abbreviations	Definitions
VC	Virtual Channel. The PEX 8747 supports one Virtual Channel – VC0.
VC&T	Virtual Channel and Type.
Vector	Address and data.
WRR	Weighted Round-Robin scheduling.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXn[x] PEX_XXXp[x]	When the signal name appears in all CAPS, with the primary Port description listed first, field [x] indicates the number associated with the signal balls/pads assigned to a specific SerDes module/Lane. The lowercase “n” (negative) or “p” (positive) suffix indicates the differential pair of signals, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a “#” appended to the term (<i>for example</i> , PEX_PERST#).
Program/code samples	Monospace font (<i>program or code samples</i>) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
command_done	Interrupt format.
Command/Status	Register names.
<i>Parity Error Detected</i>	Register parameter [bit or field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].
Number multipliers	k = 1,000 (10^3) is generally used with frequency response. K = 1,024 (2^{10}) is used for Memory size references. KB = 1,024 bytes. M = meg. = 1,000,000 when referring to frequency (decimal notation) = 1,048,576 when referring to Memory sizes (binary notation)
255d	d = Suffix that identifies decimal values.
1Fh	h = Suffix that identifies hex values. Each prefix term is equivalent to a 4-bit binary value (Nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (<i>for example</i> , 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 nor 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	Eight bits – abbreviated to “B” (<i>for example</i> , 4B = 4 bytes).
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord or DW	Double-Word (32 bits) is the primary register size in these devices.
QWord	Quad-Word (64 bits).
Reserved	Do not modify Reserved bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.
word	16 bits.

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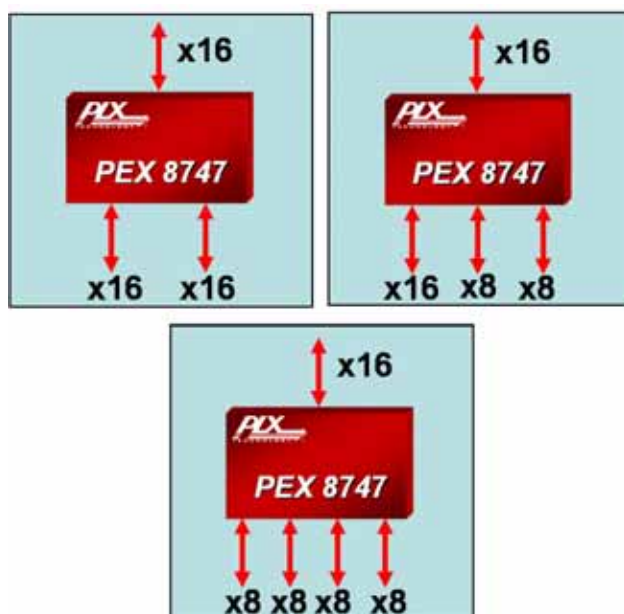
1.1 Overview

This data book describes PLX Technology's ExpressLane™ PEX 8747, a fully non-blocking, low-latency, low-cost, and low-power 48-Lane, 5-Port PCI Express Gen 3 Switch. Conforming to the *PCI Express Base r3.0*, the PEX 8747 enables users to add high-bandwidth input/output (I/O) to graphics applications. The PEX 8747's flexible hardware configuration and software programmability allows the switch to be tailored for a wide variety of graphics usage models.

The PEX 8747 is principally aimed at high-resolution graphics and dual-graphics applications with Host-centric fan-out or peer-to-peer communication traffic.

The PEX 8747 supports multiple Port configuration options, to provide flexible solutions for optimal product design. [Figure 1-1](#) illustrates the possible PEX 8747 Port configurations, using differing Link widths, of x8¹ or x16. When used with endpoints that require smaller Link widths, the PEX 8747 auto-negotiates down to support x1, x2, and x4 Link width as well.

Figure 1-1. Port Configurations



1. x8 is valid only for Stations 1 and 2.

1.2 Features

The PEX 8747 supports the following features:

- 5-Port PCI Express switch
 - 48 Lanes with integrated on-chip SerDes
 - Low-power SerDes (under 90 mW per Lane)
 - Relaxed Ordering
 - Port configuration
 - 5 independent Ports
 - Choice of Link width (quantity of Lanes) per unique Link/Port – x8¹ or x16, depending upon Port configuration; x1, x2, and x4 Link widths are also supported
 - Configurable with serial EEPROM, I²C, SMBus, and/or Host software
 - Designate any Port as the *Upstream Port*
- High Performance
 - 768 GT/s aggregate bandwidth (8.0 GT/s/Lane x 48 SerDes x 2 (full duplex))
 - Integrated 8.0 GT/s SerDes speed negotiation, for each Port
 - Full line rate on all Ports
 - Cut-Thru packet latency of less than 126 ns between symmetric (x16 to x16) ingress and egress Ports
 - Non-blocking Crossbar Switch interface supports TLP bandwidth capacity of each Link
 - Maximum Payload Size – 2,048 bytes
- *performancePAK*[™]
 - Read Pacing[™] (intelligent bandwidth allocation)
 - Multicast
 - Dynamic Buffer Pool Architecture for faster credit updates
- *visionPAK*[™]
 - Performance Monitoring
 - Per-Port Payload and Header Counters
 - Per-traffic type (Write, Read, Completion) Counters
 - PCI Express Packet Generator
 - Capable of saturating a x16 Gen 3 Link
 - Error Injection and Pseudo-Random Bit Sequence (PRBS)
 - SerDes Loopback
 - SerDes Eye Capture
- Access Control Services (ACS) – Protection mechanisms for added data integrity in peer-to-peer transactions
- Alternative Routing-ID Interpretation (ARI) – Enables virtualized systems and/or highly integrated multi-function devices
- Quality of Service (QoS) support
 - All Ports support one, full-featured Virtual Channel, VC0
 - All Ports support eight Traffic Class (TC[7:0]) mapping, independently of the other Ports
 - Round-Robin (RR) and Weighted Round-Robin (WRR) Port arbitration

1. x8 is valid only for Stations 1 and 2.

- Reliability, Availability, Serviceability (RAS) features
 - End-to-end Cyclic Redundancy Check (ECRC) and Poison bit support
 - Data path protection
 - Memory (RAM) error correction
 - Baseline and Advanced Error Reporting capability
 - Port (Link) Status bits available
 - Per-Port error diagnostics
 - Joint Test Action Group (JTAG) AC/DC boundary scan
- INTA# ([PEX_INTA#](#)) and FATAL ERROR ([FATAL_ERR#](#)) (Conventional PCI SERR# equivalent) ball support
- 11 General-Purpose Input/Output (GPIO) balls
- Other PCI Express Capabilities
 - Lane reversal
 - Polarity reversal
 - Conventional PCI-compatible Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3 (with Vaux *not supported*)
 - Conventional PCI-compatible Device Power Management states – D0 and D3hot
 - Active State Power Management (ASPM)
 - Dynamic speed (2.5, 5.0, or 8.0 GT/s (Gen 1, Gen 2, and Gen 3, respectively)) negotiation, for each Port
 - Dynamic Link width negotiation
- Out-of-Band Initialization options
 - Serial EEPROM
 - I²C and SMBus (7-bit Slave address with 100 Kbps)
- Testability – AC/DC JTAG support
- Available in three different packages
 - **27 x 27 mm² package** – 676 balls, Flip-Chip Ball Grid Array with Heat Spreader (HFC-BGA) (referred to as the *27 x 27 mm² package*)
 - **19 x 21 mm² packages** – 575 balls, Fine-Pitch Flip-Chip Ball Grid Array with or without Heat Spreader (HFC-BGA or FC-BGA, respectively) (referred to singularly as the *19 x 21 mm² package*, unless indicated otherwise)
- Typical power – 7.34W at 8.0 GT/s, with all Ports enabled
- Microsoft® Windows® Logo (WHQL)-compliant

- Compliant to the following specifications:
 - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
 - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
 - *PCI Code and ID Assignment Specification, Revision 1.2*
 - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
 - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
 - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
 - *PCI Express Base Specification, Revision 2.0 Errata*
 - *PCI Express Base Specification, Revision 2.1 (PCI Express Base r2.1)*
 - *PCI Express Base Specification, Revision 3.0 (PCI Express Base r3.0)*
 - *PCI Express Card Electromechanical Specification, Revision 2.0 (PCI ExpressCard CEM r2.0)*
 - *PCI Express Mini Card Electromechanical Specification, Revision 1.1 (PCI ExpressCard Mini CEM r1.1)*
 - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Standard 1149.1-1990)*
 - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
 - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
 - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
 - *The I²C-Bus Specification, Version 2.1 (I²C Bus v2.1)*
 - *PHY Interface for the PCI Express Architecture, Version 2.00*
 - *System Management Bus Specification, Version 2.0 (SMBus v2.0)*



Chapter 2 Features and Applications

2.1 Flexible and Feature-Rich 48-Lane, 5-Port Switch

2.1.1 Highly Flexible Port Configurations

The PLX ExpressLane PEX 8747 PCI Express Gen 3 Switch offers a maximum of five configurable Ports (one per Station 0, and two each per Stations 1 and 2). (Refer to [Figure 1-1, “Port Configurations.”](#)) To support specific bandwidth needs, Link widths can be individually configured as any power-of-two, from x1 to x8¹ or x16, through auto-negotiation, hardware strapping, an optional serial EEPROM, and/or the I²C Slave interface. Flexible buffer allocation, along with the PEX 8747’s flexible packet flow control, maximizes throughput for applications where more traffic flows in the Downstream, rather than Upstream, direction.

The PEX 8747 architecture allows for the combining of multiple Lanes to flexible Port Link widths, as needed. *For example*, x16 Lanes can form a single x16 Port, two x8 Ports, or four x4 Ports.

[Figure 1-1, “Port Configurations,”](#) illustrates the possible PEX 8747 Port configurations. Any one Port can be designated as, or dynamically changed to be, the Upstream Port.

2.1.2 Non-Blocking Crossbar Switch Architecture

The Non-Blocking Crossbar Switch architecture is an on-chip interconnect switching fabric, which is built upon the existing PLX Switch Fabric Architecture technology. In addition to addressing simultaneous multiple flows, the Crossbar Switch architecture incorporates functions required to support an efficient PCI Express switch fabric, including:

- Deadlock avoidance
- Priority preemption
- PCI Express Ordering rules
- Packet fair queuing
- Oldest first scheduling

The Crossbar Switch interconnect physical topology is that of a packet-based Crossbar Switch fabric (internal fabric), designed to simultaneously connect multiple on-chip Stations. The Crossbar Switch protocol is sufficiently flexible and robust to support a variety of embedded system requirements. The protocol is specifically designed to ease chip integration, by strongly enforcing Station boundaries and standardizing communication between Stations. The Crossbar Switch architecture basic features include:

- Multiple concurrent Data transfers
- Global ordering within the PEX 8747
- Three types of transactions – Posted, Non-Posted, and Completion (P, NP, and Cpl, respectively) – meet PCI and PCI Express Ordering and Deadlock Avoidance rules
- Optional weighting of source Ports, to support Source Port arbitration

1. x8 is valid only for Stations 1 and 2.

2.1.3 Low Packet Latency and High Performance

The PEX 8747 architecture supports packet **Cut-Thru with a latency of less than 126 ns** between symmetric (**x16 to x16**) ingress and egress Ports. This, combined with large Packet memory, flexible common buffer/FC credit pool, and Non-Blocking Internal Switch architecture, provides full line rate on all Ports for performance-hungry graphics applications. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the PEX 8747 supports a Packet Payload size of up to 2,048 bytes, enabling users to achieve even higher throughput.

2.1.3.1 Data Payloads

The Data Payloads are variable length with a maximum of 2,048 bytes, as defined by the *Maximum Payload Size* field (available sizes are 128, 256, 512, 1,024, and 2,048). Read Requests **do not** include a Data Payload.

Note: Refer to the **Device Control** register *Maximum Payload Size* field (offset 70h[7:5]) for Maximum Payload Size Port limitations.

2.1.3.2 Cut-Thru Mode

Cut-Thru mode can reduce latency, especially for longer packets, because the entire packet does not need to be stored before being forwarded. Instead, after the Header is decoded, the packet can be immediately forwarded. The PEX 8747 is designed to cut through TLPs, to and from every Port. By default, all Ports are enabled for Cut-Thru.

Caution: *One of the drawbacks to using Cut-Thru mode is that the TLP is not known to be good until the last byte. If the TLP proves to be bad, the Cut-Thru packet must be discarded. If the TLP has already been forwarded to another device, that TLP will be framed with an EDB (End Data Bad), as opposed to the standard END.*

2.1.4 Virtual Channel and Traffic Classes

The PEX 8747 supports one Virtual Channel (VC0) and eight Traffic Classes (TC[7:0]). VC0 and TC0 are required by the *PCI Express Base r3.0*, and configured at device start-up.

2.1.5 Data Integrity

To enable designs that require **guaranteed error-free packets**, the PEX 8747 provides **End-to-end Cyclic Redundancy Check (ECRC)** protection and **Poison** bit support, as well as **Error-Correcting Code (ECC)** protection on the internal data paths and memory (RAM). ECC maintains packet integrity through the PEX 8747, by providing automatic correction of any 1-bit errors. These features are optional in the *PCI Express Base r3.0*; however, PLX provides them across its entire ExpressLane PCI Express Gen 2 and Gen 3 switch product lines.

2.1.6 Configuration Flexibility

The PEX 8747 provides several ways to configure its operations. *For example*, the PEX 8747 can be configured through Strapping balls, Host software, an optional serial EEPROM, and/or the I²C Slave interface. Additionally, the I²C Slave interface allows for easy debug during the Development phase, performance monitoring during the Operation phase, and driver or software upgrade.

2.1.7 Interoperability

The PEX 8747 is designed to be fully compliant with the *PCI Express Base r3.0*, and is backward-compatible to the *PCI Express Base r2.1*, *PCI Express Base r2.0*, *PCI Express Base r1.1*, and *PCI Express Base r1.0a*. Additionally, the switch supports **auto-negotiation**, **Lane reversal**, and **polarity reversal**, for maximum board design and board layout flexibility. Furthermore, the PEX 8747 is designed to be interoperable with many popular motherboards and server boards with PCI Express connections, and PCI Express endpoints (Ethernet, RAID Controllers), as well as PLX's family of PCI Express switches and bridges. All PLX ExpressLane devices undergo thorough interoperability testing at PLX's **Interoperability Lab** and compliance testing at the **PCI-SIG Compliance Workshop**, to ensure compatibility with PCI Express devices in the market.

2.1.8 Low Power with Granular SerDes Control

The PEX 8747 provides **low-power** capability that is fully compliant with the *PCI Express Base r3.0* and *PCI Power Mgmt. r1.2* Power Management (PM) specifications. Unused SerDes can be disabled, to further reduce power consumption.

The PEX 8747 supports **SerDes output software control**, to allow power and signal strength optimization within a system. The PLX SerDes implementation supports four power levels – *Off*, *Low*, *Typical*, and *High*. The SerDes block also supports **Loopback modes** and **Advanced Error Reporting**, which enables efficient system debug and management.

2.1.9 Dynamic Lane Reversal

The PEX 8747 supports dynamic Lane reversal during the Link training process. Lane reversal capability allows flexibility in determining board routing, so that PCI Express components can be connected without having to criss-cross wires. If the wiring of Lanes to a device is reversed (on both Transmitters and Receivers), only one of the two connected devices must support Lane reversal.

Either of the outside Lanes (Transmitter and Receiver pairs) of the PEX 8747 programmed Link width must be identified as being Lane 0. During Link training, both devices on the Link negotiate the Lane numbering. During the Link Training and Status State Machine (LTSSM)'s *Configuration* state, the Upstream device sends TS1 Ordered-Sets, in which each connected Lane is identified by a consecutive Lane Number, starting with Lane 0 corresponding to the physical Lane Number associated with the Port.

The Port reverses its Lane Numbers and attempts to re-train when any of the following conditions occur:

- No Receiver is detected on preferred Lane 0
- No valid Training Sets are received on preferred Lane 0 during the LTSSM's *Polling* state
- TS1 with a non-zero Lane Number Port is received on the Port's Lane 0

To confirm successful Lane Number negotiation, both devices exchange TS2 Ordered-Sets with identical Lane Numbers on each connected Lane.

2.1.10 Fully Compliant Power Management

The PEX 8747 supports Link (L0, L0s, L1, L2/L3 Ready, and L3) and Device (D0 and D3hot) PM states, in compliance with the *PCI Express Base r3.0* and *PCI Power Mgmt. r1.2* PM specifications.

For further details, refer to [Chapter 10, "Power Management."](#)

2.1.11 General-Purpose Input/Output Signals

The PEX 8747 contains 11 General-Purpose Input/Output (GPIO) balls and associated registers, that can be programmed to function as GPIO, Link Status (PORT_GOOD) indicators, and/or Interrupt inputs. Default functionality is GPIO input; however, serial EEPROM, I²C/SMBus, and/or software can program the **GPIO** registers to define functionality for each I/O. Default functionality can also be modified by the logical value of the STRAP_TESTMODE0 3-state input, sampled at Fundamental Reset. Because typical designs implement PORT_GOOD functionality for enabled Ports, GPIO[9:8, 5:4, 0] are renamed as **PORT_GOOD[9:8, 5:4, 0]#**.

For details, refer to the GPIO[10, 7:6, 3:1], PORT_GOOD[9:8, 5:4, 0]#, and STRAP_TESTMODE0 signal descriptions in [Section 3.4, "Signal Ball Descriptions – 27 x 27 mm2 Package,"](#) and [Section 3.5, "Signal Ball Descriptions – 19 x 21 mm2 Package."](#)

2.1.12 **performancePAK**

Exclusive to PLX, *performancePAK* is a suite of unique and innovative performance features that enable PLX switches to be the highest-performing switches available in the market today. The *performancePAK* features consist of Read Pacing, Multicast, and Dynamic Buffer Pool.

2.1.12.1 **Read Pacing**

The Read Pacing feature allows users to throttle the quantity of Read Requests being made by Downstream devices. When a Downstream device requests several long Reads back-to-back, the Root Complex services the Read Requests from this Downstream Port in a sequential order. If this Port has a narrow Link and is therefore slow in receiving these Read packets from the Root Complex, other Downstream Ports may become starved, thus negatively impacting performance. This feature enhances performance by allowing for the adequate servicing of all Downstream devices, by intelligent handling of Read Requests.

For further details, refer to [Section 8.5, “Read Pacing.”](#)

2.1.12.2 **Multicast**

Multicast (MC) allows programs to concurrently write the same data to a group of multiple destinations. When Posted Memory Write or Address Routed Message TLPs entering the PEX 8747 are addressed to the MC Address range (*MC BARs*), the PEX 8747 automatically generates and transmits, if enabled, a copy of the original TLP (referred to as the *MC Copy TLP*) to the destination Ports. The MC Address space is divided into *MC Groups (MCG)*, defined by using *MC Base Address* and *MC Index Position*. Each PEX 8747 Port can elect to receive an MC Copy TLP by belonging to an *MCG*, by Setting the corresponding *MC Receive* bit. An MC TLP can be blocked using the *MC Block All* bit, if required. *MC Overlay Bar* can be used to replace the original MC TLP's address to a Unicast Address space, if the endpoint does not support MC.

For further details, refer to [Section 8.6, “Multicast.”](#)

2.1.12.3 **Dynamic Buffer Pool**

The PEX 8747 uses a dynamic buffer pool for FC management, which uses a common pool of FC Credits that is shared among other Ports within the same Station. This shared buffer pool is user-programmable, so FC credits can be allocated among the enabled Ports, as needed. Not only does this prevent wasted buffers and inappropriate buffer assignments, any un-allocated buffers remain in the common buffer pool, which can then be used by other Ports within the same Station, for faster FC credit updates.

2.1.13 visionPAK

Another PLX exclusive, *visionPAK* is a debug diagnostics suite of integrated hardware and software instruments that users can use to help bring their systems to market faster. *visionPAK* features consist of Performance Monitoring, Error Injection, SerDes Loopback, SerDes Eye Capture, and more.

2.1.13.1 Performance Monitoring

The PEX 8747's real-time performance monitoring allows users to literally “see” ingress and egress performance on each Port as traffic passes through the switch, using PLX's Software Development Kit (SDK). The monitoring is completely passive, and therefore, has no effect on overall system performance. Internal Counters provide extensive granularity down to traffic and packet type, and even allow for the filtering of traffic (*that is*, count only Memory Writes).

2.1.13.2 Error Injection

Using the PEX 8747's Error Injection feature, users can inject malformed packets and/or Fatal errors into their system, then evaluate the system's ability to detect and recover from such errors.

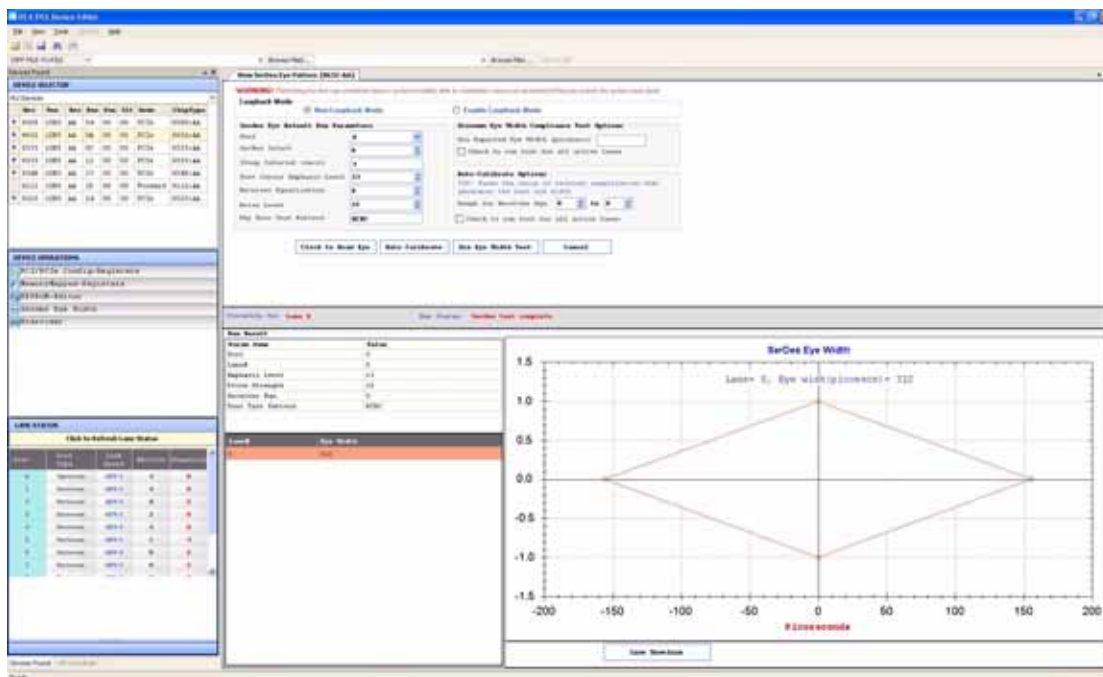
2.1.13.3 SerDes Loopback

The PEX 8747 supports External Tx, Recovered Clock, and Recovered Data Loopback modes.

2.1.13.4 SerDes Eye Capture

Users can evaluate their system's signal integrity at the Physical Layer (PHY), using the PEX 8747's SerDes Eye Capture feature. Using PLX's SDK, users can view the Receiver eye width of any Lane on the PEX 8747. Users can then modify SerDes Settings and see the impact on the Receiver eye. [Figure 2-1](#) presents a screenshot of the SDK's SerDes Eye Capture feature.

Figure 2-1. PLX SDK SerDes Eye Capture Feature



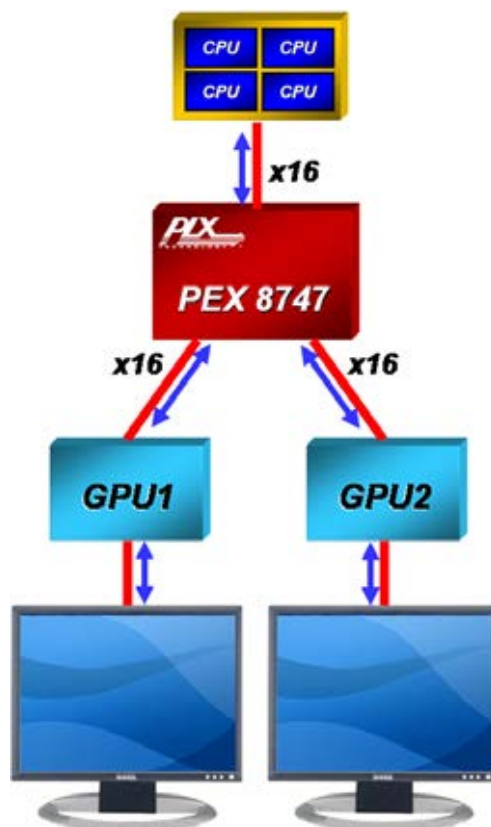
2.2 Graphics Applications

High-resolution 3D graphics applications can take full advantage of the PEX 8747 three-Port configuration. Applications *such as* dual graphics, high-resolution gaming, high-resolution scientific use, and image processing can benefit from PEX 8747 performance. The PEX 8747 is suitable for Host-centric graphics fan-out, as well as dual graphics with peer-to-peer communication applications.

2.2.1 Host-Centric Fan-Out in Dual-GPU Applications

In a Host-centric graphics fan-out application, the PEX 8747 drives a dual-output display. The PEX 8747 fans out to two Graphics Modules (the two Graphics Processing Units (GPUs), in [Figure 2-2](#)), by way of the two x16 Downstream Ports, while the x16 Upstream Port links to the Root Complex. Increasing memory and bandwidth requirements have put a strain on local GPU memory. The PEX 8747 allows for highly efficient Data transfers over the PCI Express interface, allowing the Graphics Module to use the System memory and render the memory as if it is local Graphics memory. In a fan-out application such as this, the traffic is Host-centric, with each GPU driving its own output.

Figure 2-2. Dual-GPU Applications

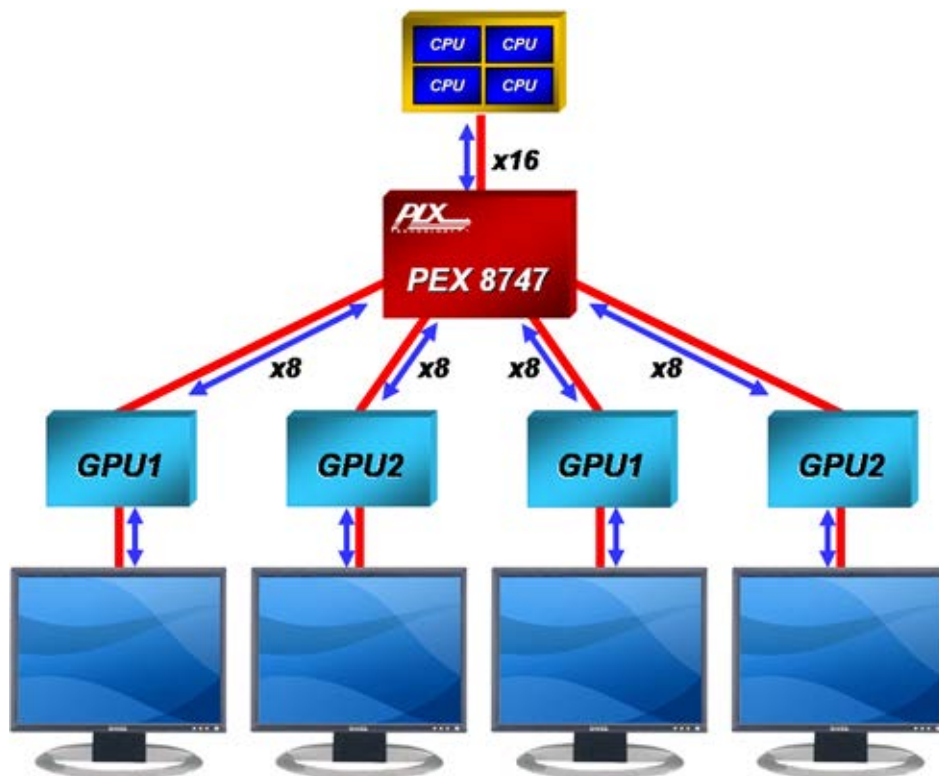


2.2.2 Host-Centric Fan-Out in Quad-GPU Applications

For Quad-GPU applications using four GPUs to drive four separate displays, users can take advantage of the PEX 8747's four x8 Downstream Ports. Mid-range to low-end systems that may not require the bandwidth provided by a x16 Link can instead take advantage of the PEX 8747's x8 Links and fan-out to up to four display units, such as in the system illustrated in [Figure 2-3](#).

A combination of x16 and x8 Downstream Ports can be used as well. *For example*, one x16 Downstream Port can drive one display, while two x8 Downstream Ports drive two other displays.

Figure 2-3. Quad-GPU Applications



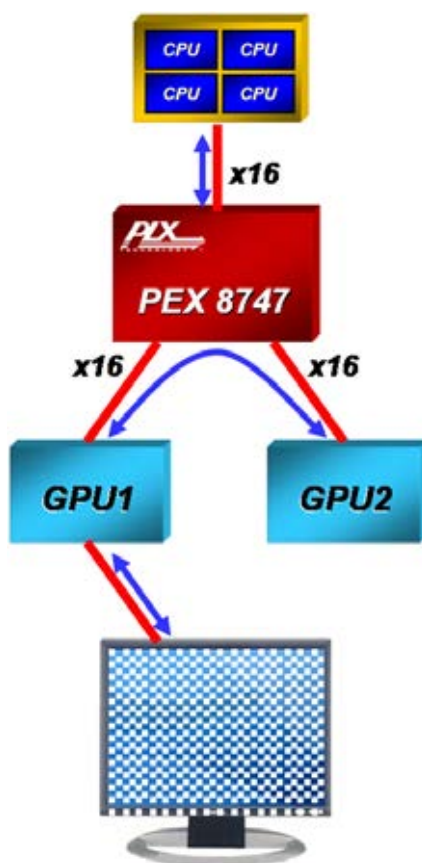
2.2.3 Dual Graphics with Peer-to-Peer Communication

Figure 2-4 illustrates the PEX 8747 used in a dual-graphics gaming application, where two GPUs drive a single monitor for the ultimate gaming experience. The Upstream Port links to the Root Complex and the two Downstream Ports connect to the GPUs. The PEX 8747's peer-to-peer support allows the two GPUs to communicate with one another, in addition to Upstream, for maximum performance.

In this example, the two GPUs divide the screen into a checkerboard pattern. In Figure 2-4, the screen is divided into white and blue frames, with one GPU managing the white frames and the other managing the blue frames. This mode of operation is referred to as *Supertiling*, and is generally the most efficient because it evenly divides the processing and graphics rendering workload across the two GPUs.

This usage model calls for heavy peer-to-peer communication between the two GPUs. The PEX 8747 can also support dual-graphics solutions running in Scissor, or Alternate Frame Rate modes. In each of these modes, the processing and graphics rendering workload is shared by the GPUs, and therefore requires a great amount of peer-to-peer communication between the GPUs to monitor one another's progress and execution.

Figure 2-4. Dual Graphics with Peer-to-Peer Communication



2.3 Software Usage Model

From the system model viewpoint, each PCI Express Port is a virtual PCI-to-PCI bridge, with its own set of PCI Express Configuration registers. The recommended Upstream Port is Port 0; however, any Port can be configured as the Upstream Port through optional configuration, by way of a serial EEPROM, the I²C Slave interface, and/or Strapping balls. The BIOS or Host can configure the other Ports, by way of the Upstream Port, using Conventional PCI enumeration.

2.3.1 System Configuration

The virtual PCI-to-PCI bridges within the PEX 8747 are compliant to the PCI and PCI Express system models. The Configuration Space registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0 and Type 1 Configuration Requests, through the virtual primary bus interface (matching Bus Number, Device Number, and Function Number).

2.3.2 Interrupt Sources and Events

The PEX 8747 supports the INTx Interrupt Message type (compatible with *PCI r3.0* Interrupt signals) or Message Signaled Interrupts (MSIs), when enabled. The PEX 8747 generates interrupts/Messages for the following:

- Link State events
- PCI Express Hot Plug events
- GPIO-generated events
- Baseline and Advanced Error Reporting

Internally generated interrupts and interrupts forwarded from Downstream Ports are re-mapped and collapsed at the Upstream Port.



Chapter 3 Signal Ball Description

3.1 Introduction

This chapter describes the following signal ball-related information:

- [Ball Assignment Abbreviations](#)
- [Internal Pull-Up/Pull-Down Resistors](#)
- [Signal Ball Descriptions – 27 x 27 mm² Package](#)
- [Signal Ball Descriptions – 19 x 21 mm² Package](#)
- [Physical Layout](#)

3.2 Ball Assignment Abbreviations

Table 3-1 lists the abbreviations used within this chapter.

Table 3-1. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
3-state input	Associated with the Strapping signals. Can be High (1), Low (0), or High-Impedance (Z; not connected/floating).
A	Analog Input signal
APWR	Power (VDD09A) balls for SerDes Analog circuits
HCSLn ^a	High-Speed Current Steering Logic (HCSL) negative Clock inputs
HCSLp ^a	HCSL positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	0.9V Power (VDD09) balls for low-voltage Core circuits
GND	Common Ground (VSS) for all circuits
I	Input
I/O	Bidirectional (Input or Output)
I/OPWR	1.8V Power (VDD18) balls for Input and Output interfaces
O	Output
OD	Open Drain output
PD	Weak internal pull-down resistor
PLLWR	1.8V Power (VDD18A) balls for Phase-Locked Loop (PLL) circuits
PU	Weak internal pull-up resistor
SerDes	Serializer/De-Serializer differential low-voltage, high-speed, I/O signal pairs (negative and positive)
STRAP	Signals used for PEX 8747 configuration, operational mode Setting, and Factory Test ; these signals generally are not toggled at runtime
TS ^b	Tri-statable Output (High-Impedance when output is not driven)

a. For REFCLK inputs, HCSL source is recommended.

b. Used in the Signal tables, **Type** column. All other use of TS is for “Training Sequence.”

3.3 Internal Pull-Up/Pull-Down Resistors

The PEX 8747 contains I/O buffers that have weak internal pull-up or pull-down resistors, indicated in this chapter by PU or PD, respectively, in the signal ball tables (**Type** column). If a signal with this notation is used and no board trace is connected to the ball, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace and is not used nor driven by an external source at all times, the internal resistors might not be sufficiently strong, to hold the signal in the inactive state. In cases such as these, it is recommended that the signal be pulled or tied High to **VDD18** or Low to **VSS** (Ground), as appropriate, through a 3K Ω to 10K Ω resistor.

Table 3-2 lists the internal pull-up and pull-down resistor values.

Table 3-2. Internal Resistor Values

Internal Resistor	Minimum	Typical	Maximum	Units
PU	38K	57K	92K	Ω
PD	37K	53K	99K	Ω

3.4 Signal Ball Descriptions – 27 x 27 mm² Package

Notes: *If there is more than one ball per signal name that includes a numbered range, the locations are listed in the same sequence in which the range is listed, starting at the top row, from left to right. For example, PEX_PERn11 is located at AC17, PEX_PERn10 is located at AC16, and so forth.*

If there is more than one ball per signal name that does not include a numbered range (such as VDD09), the locations are listed in ascending alphanumeric order.

For signal names and locations of the 19 x 21 mm² package, refer to [Section 3.5](#).

The following signals exist only in the 27 x 27 mm² package; they do not exist in the 19 x 21 mm² package – STRAP_GEN1_GEN2, STRAP_PROBE_MODE#, STRAP_RESERVED[18, 12:0, 4:1], STRAP_SERDES_MODE_EN#, STRAP_UPSTRM_PORTSEL2, THERMAL_DIODEn, and THERMAL_DIODEp.

The PEX 8747 signals associated with the 27 x 27 mm² package are divided into the following groups:

- [PCI Express Signals – 27 x 27 mm² Package](#)
- [Serial EEPROM Signals – 27 x 27 mm² Package](#)
- [Strapping Signals – 27 x 27 mm² Package](#)
- [JTAG Interface Signals – 27 x 27 mm² Package](#)
- [I2C/SMBus Slave Interface Signals – 27 x 27 mm² Package](#)
- [Device-Specific Signals – 27 x 27 mm² Package](#)
- [External Resistor Signals – 27 x 27 mm² Package](#)
- [Thermal Diode Signals – 27 x 27 mm² Package](#)
- [No Connect Signals – 27 x 27 mm² Package](#)
- [Power and Ground Signals – 27 x 27 mm² Package](#)

3.4.1 PCI Express Signals – 27 x 27 mm² Package

Table 3-3 defines the PCI Express SerDes and Control signals.

Table 3-3. PCI Express Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PEX_PERn[15:0]	AC22, AC21, AC20, AC19, AC17, AC16, AC15, AC14, AC13, AC12, AC11, AC10, AC8, AC7, AC6, AC5	CMLRn	No	–
		Negative Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)		
PEX_PERn[31:16]	D13, D12, D11, D10, D8, D7, D6, D5, J4, K4, L4, M4, P4, R4, T4, U4	CMLRn	No	–
		Negative Half of PCI Express Receiver Differential Signal Pairs for Station 1 (16 Balls)		
PEX_PERn[47:32]	D14, D15, D16, D17, D19, D20, D21, D22, J23, K23, L23, M23, P23, R23, T23, U23	CMLRn	No	–
		Negative Half of PCI Express Receiver Differential Signal Pairs for Station 2 (16 Balls)		
PEX_PERp[15:0]	AB22, AB21, AB20, AB19, AB17, AB16, AB15, AB14, AB13, AB12, AB11, AB10, AB8, AB7, AB6, AB5	CMLRp	No	–
		Positive Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)		
PEX_PERp[31:16]	E13, E12, E11, E10, E8, E7, E6, E5, J5, K5, L5, M5, P5, R5, T5, U5	CMLRp	No	–
		Positive Half of PCI Express Receiver Differential Signal Pairs for Station 1 (16 Balls)		
PEX_PERp[47:32]	E14, E15, E16, E17, E19, E20, E21, E22, J22, K22, L22, M22, P22, R22, T22, U22	CMLRp	No	–
		Positive Half of PCI Express Receiver Differential Signal Pairs for Station 2 (16 Balls)		
PEX_PERST#	AC1	I, PU	No	–
		PCI Express Reset Used to cause a Fundamental Reset. Refer to Section 5.1, “Reset,” for further details.		
PEX_PETn[15:0]	AF22, AF21, AF20, AF19, AF17, AF16, AF15, AF14, AF13, AF12, AF11, AF10, AF8, AF7, AF6, AF5	CMLTn	No	–
		Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls) PEX_PETn[15:0] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETn[31:16]	A13, A12, A11, A10, A8, A7, A6, A5, J1, K1, L1, M1, P1, R1, T1, U1	CMLTn	No	–
		Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (16 Balls) PEX_PETn[31:16] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETn[47:32]	A14, A15, A16, A17, A19, A20, A21, A22, J26, K26, L26, M26, P26, R26, T26, U26	CMLTn	No	–
		Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (16 Balls) PEX_PETn[47:32] must be AC-coupled. Use a 0.22 µF capacitor.		

Table 3-3. PCI Express Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PEX_PETp[15:0]	AE22, AE21, AE20, AE19, AE17, AE16, AE15, AE14, AE13, AE12, AE11, AE10, AE8, AE7, AE6, AE5	CMLTp	No	–
		Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls) PEX_PETp[15:0] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETp[31:16]	B13, B12, B11, B10, B8, B7, B6, B5, J2, K2, L2, M2, P2, R2, T2, U2	CMLTp	No	–
		Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (16 Balls) PEX_PETp[31:16] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETp[47:32]	B14, B15, B16, B17, B19, B20, B21, B22, J25, K25, L25, M25, P25, R25, T25, U25	CMLTp	No	–
		Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (16 Balls) PEX_PETp[47:32] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_REFCLKn	AF9	HCSLn	No	–
		Negative Half of 100-MHz PCI Express Constant Frequency Reference Clock Input Signal Pair An internal coupling capacitor is provided (an external capacitor is not needed).		
PEX_REFCLKp	AE9	HCSLp	No	–
		Positive Half of 100-MHz PCI Express Constant Frequency Reference Clock Input Signal Pair An internal coupling capacitor is provided (an external capacitor is not needed).		

3.4.2 Serial EEPROM Signals – 27 x 27 mm² Package

The PEX 8747 includes four signals for interfacing to a serial EEPROM, defined in [Table 3-4](#). The serial EEPROM is used to load register values immediately following Reset (PEX_PERST# or Hot Reset/DL_Down). Most registers can be programmed by serial EEPROM, as indicated in the register descriptions.

For information regarding serial EEPROM use, refer to [Chapter 6, “Serial EEPROM Controller.”](#)

Table 3-4. Serial EEPROM Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
EE_CS#	E26	I/O, PU	No	–
		Active-Low Serial EEPROM Chip Select Output <i>Note:</i> Although this is an I/O signal, its logical operation is output.		
EE_DI	G23	I/O, TS	No	–
		PEX 8747 Output to Serial EEPROM Data Input <i>Note:</i> Although this is an I/O signal with tri-statable output, its logical operation is output that is always driven.		
EE_DO	F26	I/O, PU	No	–
		PEX 8747 Input from Serial EEPROM Data Output Should be pulled High to VDD18 . <i>Note:</i> Although this is an I/O signal, its logical operation is input.		
EE_SK	E25	I/O, PU	No	–
		Serial EEPROM Clock Frequency Output Programmable, by way of the Serial EEPROM Clock Frequency register EepFreq[2:0] field (Port 0, offset 268h[2:0]), to the following: <ul style="list-style-type: none"> • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz <i>Note:</i> Although this is an I/O signal, its logical operation is output.		

3.4.3 Strapping Signals – 27 x 27 mm² Package

Note: [Table 4-1](#) indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.

The PEX 8747 Strapping signals, described in [Table 3-5](#), define the configuration of Upstream Port assignment, Link width, and various setup and test modes.

Many of the Strapping signals are I/O 3-state inputs, which can be High (1), Low (0), or High-Impedance (Z; not connected/floating).

Strapping signals that have 2-state inputs (rather than 3-state inputs; indicated simply as “inputs”) use internal pull-up and pull-down resistors to define the default configuration; if the PEX 8747 configuration must be changed from the default, external pull-up and/or pull-down resistors can be connected. External resistors are not required unless the Strapping signals:

- Must be changed from the default logic state, –or–
- Are connected to circuit traces (the internal resistors are relatively weak, and may not be sufficiently strong, to hold circuit traces to the default input states)

After a Fundamental Reset, the **Link Capability**, **Port Configuration**, and **Upstream Port** registers (offsets 74h, 300h, and 360h, respectively) capture Strapping ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the serial EEPROM (if present). I²C/SMBus can also change Strapping ball Configuration data; however, the STRAP_I2C_SMBUS_CFG_EN# input should be pulled or tied Low to VSS (Ground), to prevent linkup and Host enumeration. Then, when I²C programming is complete, I²C/SMBus should lastly Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]), to enable linkup and allow subsequent Host enumeration.

Table 3-5. Strapping Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State			
		Description					
STRAP_GEN1_GEN2	H24	I/O, 3-state input	No	–			
		PCI Express Data Rate Select Selects the maximum PCI Express data rate for all Ports, by globally changing the values for Maximum Link Speed and Target Link Speed (offsets 74h[3:0] and 98h[3:0]), respectively), in all Ports. The value of this 3-state input is latched and reflected in the Strap Configuration register Gen 2 Mode Status and Gen 1 Mode Status bits (Port 0, offset 46Ch[12:11] , respectively).					
		STRAP_GEN1_GEN2 Input State and Link Speed	Offset 74h[3:0] Value	Offset 98h[3:0] Value	Offset 46Ch[12:11] Value		
		0 = Gen 1 (2.5 GT/s)	1h	1h	10b		
		Z = Gen 2 (5.0 GT/s)	2h	2h	01b		
		1 = Gen 3 (8.0 GT/s)	3h	3h	11b		

Table 3-5. Strapping Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
STRAP_I2C_SMBUS_CFG_EN#	W6	I/O, PU	No	–
		<p>I²C Bus Configuration Enable</p> <p>Enables or disables the I²C/SMBus for initial device configuration prior to initial Link training. Must be pulled or tied High to VDD18 or Low to VSS (Ground). The value of this input is latched and reflected in the Strap Configuration register <i>I2C Configuration Enable Status</i> bit (Port 0, offset 46Ch[5]).</p> <p>L = Enables I²C/SMBus for initial device configuration. The serial EEPROM can also be used in this mode. After I²C and/or the serial EEPROM Sets the Configuration Release register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]), all Ports start Link training.</p> <p>H = Disables I²C/SMBus for initial device configuration. The <i>Initiate Configuration</i> bit is Set by hardware, immediately after the PEX 8747 comes out of reset. After the serial EEPROM load finishes, all Ports start Link training (assuming that the serial EEPROM does not Clear the <i>Initiate Configuration</i> bit).</p> <p>Notes: The Delayed Linkup option might require software support to delay Host enumeration until I²C/SMBus completes switch initialization (by Setting the <i>Initiate Configuration</i> bit; otherwise system software could miss detection of the PCI Express hierarchy (precluding device enumeration). Although this is an I/O signal, its logical operation is input.</p>		
STRAP_I2C_SMBUS_EN	F2	I/O, 3-state input	No	–
		<p>I²C/SMBus Protocol Select Enable</p> <p>Selects the I²C or SMBus protocol, and defines the default SMBus Configuration register <i>SMBus Enable</i> and <i>ARP Disable</i> bit (Port 0, offset 2C8h[0 and 8], respectively) values, as listed in the subtable below. The value of this 3-state input is latched and reflected in the Strap Configuration register <i>SMBus Enable Status</i> bit (Port 0, offset 46Ch[6]).</p>		
		STRAP_I2C_SMBUS_EN Input State	Offset 2C8h[0] Value	Offset 2C8h[8] Value
		0	0	–
		Z, 1	1	1
		<p>0 = Enables I²C Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus</p> <p>Z, 1 = Enables SMBus with ARP, on the I2C_SCL0 and I2C_SDA0 2-wire bus</p>		

Table 3-5. Strapping Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
STRAP_PLL_BYPASS#	Y26	I, PU	No	–
		Factory Test Only Must be pulled or tied High to VDD18 .		
STRAP_PROBE_MODE#	Y21	I, PU	No	–
		Factory Test Only Must be pulled or tied High to VDD18 .		
STRAP_RESERVED[21:20], STRAP_RESERVED19#, STRAP_RESERVED[18, 16:14, 12:9, 7, 5, 4:0]	AD4, AD3, B3, G2, AE24, AE25, AC25, G6, A2, AA18, C26, G1, AF24, F3, W3, N21, N6, AD25	I (all but 16) PWR (16)	No	–
		Factory Test Only (18 Balls) Reserved for future use Refer to Table 3-6 for specific pull-up/pull-down resistor requirements.		
STRAP_SERDES_MODE _EN#	W26	I, PU	No	–
		Factory Test Only Must be pulled or tied High to VDD18 .		

Table 3-5. Strapping Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
STRAP_STN1_PORTCFG0	C4	I/O, 3-state input	No	–
		<p>Strapping Signal to Select Port Configuration for Station 1 (Quantity of Enabled Ports (1 or 2), and Maximum Quantity of Lanes for Each Specific Port)</p> <p>Defines the enabled Port Numbers and their Link widths, for Station 1. Programs the Port Configuration register <i>Port Configuration for Station 1</i> field (Port 0, offset 300h[5:3]) default value.</p> <p><i>Notes:</i> The default Maximum Payload Size supported is based upon the STRAP_STNx_PORTCFG0 3-state inputs. If the serial EEPROM or I²C/SMBus changes the Port configuration (from the strapped value), it must also program the value of the Port's Device Capability register <i>Maximum Payload Size Supported</i> field (offset 6Ch[2:0]), accordingly (with the value dependent upon the Station having the most enabled Ports).</p> <p>Refer to Table 4-1 for the Port Configurations associated with these values.</p> <p>0 = 0 = Reserved Z = 1 = x16 1 = 2 = x8x8</p>		
STRAP_STN2_PORTCFG0	C23	I/O, 3-state input	No	–
		<p>Strapping Signal to Select Port Configuration for Station 2 (Quantity of Enabled Ports (1 or 2), and Maximum Quantity of Lanes for Each Specific Port)</p> <p>Defines the enabled Port Numbers and their Link widths, for Station 2. Programs the Port Configuration register <i>Port Configuration for Station 2</i> field (Port 0, offset 300h[8:6]) default value.</p> <p><i>Notes:</i> The default Maximum Payload Size supported is based upon the STRAP_STNx_PORTCFG0 3-state inputs. If the serial EEPROM or I²C/SMBus changes the Port configuration (from the strapped value), it must also program the value of the Port's Device Capability register <i>Maximum Payload Size Supported</i> field (offset 6Ch[2:0]), accordingly (with the value dependent upon the Station having the most enabled Ports).</p> <p>Refer to Table 4-1 for the Port Configurations associated with these values.</p> <p>0 = 0 = Reserved Z = 1 = x16 1 = 2 = x8x8</p>		

Table 3-5. Strapping Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State																
		Description																		
STRAP_TESTMODE0	Y6	I/O, 3-state input	No	–																
		Test Mode Select The STRAP_TESTMODE0 input state (first value listed below) indicates the test mode (second value listed below), which defines the default functionality of the PORT_GOODx# and GPIOx signals. The value of this 3-state input is latched and reflected in the Strap Configuration register <i>Strap Test Mode Status</i> field (Port 0, offset 46Ch[28:24]). 0 = 0 = PORT_GOOD[9:8, 5:4, 0]# functionality defaults to PORT_GOOD for Ports 17, 16, 9, 8, and 0, respectively Z = 1 = Factory Test Only 1 = 2 = PORT_GOOD[9:8, 5:4, 0]# and GPIO[10, 7:6, 3:1] functionality defaults to GPIO input																		
STRAP_UPSTRM_PORT SEL[2:0]	G26, G24, G25	I/O, 3-state input	No	–																
		Select Upstream Port (3 Balls) Select any Port as the Upstream Port. These inputs map to the Upstream Port register <i>Upstream Port</i> field (Port 0, offset 360h[4:0]). If I ² C/SMBus is used to configure the PEX 8747, the STRAP_I2C_SMBUS_CFG_EN# input can be pulled or tied Low to VSS (Ground), to delay linkup until I ² C/SMBus initialization is complete. After I ² C initialization is complete, I ² C/SMBus must then Set the Configuration Release register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]). <table><tr><th>STRAP_UPSTRM_PORTSEL[2:0]] Input States</th><th>Offset 360h[4:0] Value</th><th>Port Number</th></tr><tr><td>000</td><td>0_0000b</td><td>0</td></tr><tr><td>011</td><td>0_1000b</td><td>8</td></tr><tr><td>Z00</td><td>0_1001b</td><td>9</td></tr><tr><td>Z1Z</td><td>1_0000b</td><td>16</td></tr><tr><td>Z11</td><td>1_0001b</td><td>17</td></tr></table> All other encodings are Reserved .			STRAP_UPSTRM_PORTSEL[2:0]] Input States	Offset 360h[4:0] Value	Port Number	000	0_0000b	0	011	0_1000b	8	Z00	0_1001b	9	Z1Z	1_0000b	16	Z11
STRAP_UPSTRM_PORTSEL[2:0]] Input States	Offset 360h[4:0] Value	Port Number																		
000	0_0000b	0																		
011	0_1000b	8																		
Z00	0_1001b	9																		
Z1Z	1_0000b	16																		
Z11	1_0001b	17																		

Table 3-6. Factory Test Only STRAP_RESERVED[21:20], STRAP_RESERVED19#, STRAP_RESERVED[18, 16:14, 12:9, 7, 5, 4:0] Input External Pull-Up/Pull-Down Resistor Requirements

Ball/Signal Name	Location	PU/PD	Pull-Up/Pull-Down Requirement
STRAP_RESERVED21	AD4	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED20	AD3	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED19#	B3	PU	Pull High to VDD18 ; can optionally remain unconnected, due to its internal pull-up resistor.
STRAP_RESERVED18	G2	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED16	AE24	–	Must be tied directly to VSS (Ground).
STRAP_RESERVED15	AE25	–	Must be pulled High to VDD18 .
STRAP_RESERVED14	AC25	–	Must be pulled High to VDD18 .
STRAP_RESERVED12	G6	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED11	A2	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED10	AA18	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED9	C26	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED7	G1	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED5	AF24	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED4	F3	PU	Pull or tie High to VDD18 ; can optionally remain unconnected, due to its internal pull-up resistor.
STRAP_RESERVED3	W3	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED2	N21	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED1	N6	–	Must be pulled or tied High to VDD18 .
STRAP_RESERVED0	AD25	PU	Pull or tie High to VDD18 ; can optionally remain unconnected, due to its internal pull-up resistor.

3.4.4 JTAG Interface Signals – 27 x 27 mm² Package

The PEX 8747 includes five signals for performing Joint Test Action Group (JTAG) boundary scan, defined in [Table 3-7](#). The JTAG interface is described in [Section 12.6, “JTAG Interface.”](#)

Table 3-7. JTAG Interface Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
JTAG_TCK	B2	I, PD	No	–
		JTAG Test Clock Input JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 15 MHz.		
JTAG_TDI	C3	I, PD	No	–
		JTAG Test Data Input Serial input to the JTAG TAP Controller, for test instructions and data.		
JTAG_TDO	G5	I/O, TS	No	–
		JTAG Test Data Output Serial output from the JTAG TAP Controller test instructions and data. <i>Note: Although this is an I/O signal with tri-statable output, its logical operation is output that is driven when the TAP Controller is being used; otherwise, the output is High-Impedance.</i>		
JTAG_TMS	B1	I, PD	No	–
		JTAG Test Mode Select Input decoded by the JTAG TAP Controller, to control test operations.		
JTAG_TRST#	C2	I, PD	No	–
		JTAG Test Reset Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the JTAG_TRST# input should be driven Low, or pulled Low to VSS (Ground) through a 1.5K Ω resistor, to place the JTAG TAP Controller into the <i>Test-Logic-Reset</i> state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the <i>Test-Logic-Reset</i> state by initializing the JTAG TAP Controller's Instruction register to contain the <i>IDCODE</i> instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.		

3.4.5 I²C/SMBus Slave Interface Signals – 27 x 27 mm² Package

Table 3-8 defines the three I²C/SMBus Slave interface signals. The I²C/SMBus Slave interface provides access to the PEX 8747 registers. Most registers that can be programmed by serial EEPROM (including registers that are Read Only to PCI Express), can be also programmed by I²C/SMBus. However, I²C/SMBus cannot replace the serial EEPROM programming of some registers, *such as* SerDes- and Hot Plug-related registers that (generally) must be configured prior to automatic link training, immediately following Reset. I²C/SMBus can also be used to program the serial EEPROM.

The I²C/SMBus Slave interface used with PLX software is a powerful debugging tool that enables register access, regardless of whether the PCI Express Link is Up. Figure 3-1 illustrates the suggested Header pin layout on 0.1-inch centers, for direct connection to the Total Phase Aardvark I²C-USB converter (as used with PLX Rapid Development Kits (RDKs)).

For further details, refer to Chapter 7, “I²C/SMBus Slave Interface Operation.”

Figure 3-1. Suggested I²C Header Pin Layout on 0.1-Inch Centers

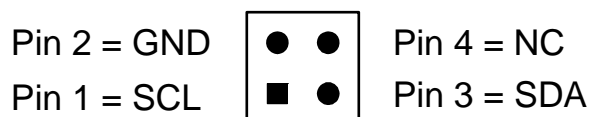


Table 3-8. I²C/SMBus Slave Interface Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
I2C_ADDR0	E2	I/O, 3-state input	No	–
		I²C Slave/SMBus Device Address Bit		
		Used to define the two least significant bits of the PEX 8747 I ² C/SMBus 7-bit Slave Address, which is reflected in both the I²C Configuration register <i>Slave Address</i> and SMBus Configuration register <i>SMBus Device Address</i> fields (Port 0, offsets 294h[6:0] and 2C8h[7:1], respectively). If I ² C or SMBus configuration is used, the I2C_ADDR0 3-state input should be strapped to a unique address, to avoid an address conflict with any other I ² C/SMBus devices (on the same I ² C Bus/ SMBus segment).		
		The three possible default I ² C Slave/SMBus Device Address values are listed below.		
		I2C_ADDR0 Input State		I²C Slave/SMBus Device Address
		0	0111_000b (default)	
Z	0111_001b			
1	0111_010b			

Table 3-8. I²C/SMBus Slave Interface Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
I2C_SCL0	G4	OD	No	—
		I²C/SMBus Serial Clock Line I ² C/SMBus bidirectional Clock line. Data on the I ² C Bus can be transferred at rates of up to 100 kbit/s (Standard mode). Because the 1.8V signaling is less than the voltage defined by the I ² C Bus v2.1 (5V, 3.3V), external voltage translation circuitry might be required. I2C_SCL0 requires an external pull-up resistor. <i>Note: The PEX 8747 I²C/SMBus Slave Interface can stretch the Low period of the I²C/SMBus clock while a simultaneous in-band Request that also targets PEX 8747 registers is being processed.</i>		
I2C_SDA0	E3	OD	No	—
		I²C/SMBus Serial Data Line Transmits and receives I ² C/SMBus data during I ² C/SMBus accesses to PEX 8747 registers. Because the 1.8V signaling is less than the voltage defined by the I ² C Bus v2.1 (5V, 3.3V), external voltage translation circuitry might be required. I2C_SDA0 requires an external pull-up resistor.		

3.4.6 Device-Specific Signals – 27 x 27 mm² Package

Table 3-9 defines the Device-Specific signals – signals that are unique to the PEX 8747.

Table 3-9. Device-Specific Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
FATAL_ERR#	C24	I/O, TS	No	–
		<p>Fatal Error Output</p> <p>FATAL_ERR# is asserted Low when a Fatal error is detected in the PEX 8747 and the following conditions are met (all the same conditions that are required to send a Fatal Error Message to the Host).</p> <p>For <i>PCI Express Base r3.0</i> errors:</p> <ul style="list-style-type: none"> Specific error is defined as <i>Fatal</i> in the Uncorrectable Error Severity register (offset FC0h), and Reporting of the specific error condition is enabled, not masked by the Uncorrectable Error Mask register's (offset FBCh) corresponding <i>Interrupt Mask</i> bit, and Device Control register <i>Fatal Error Reporting Enable</i> bit (offset 70h[2]) or PCI Command register <i>SERR# Enable</i> bit (offset 04h[8]) is Set <p>Device-Specific (RAM ECC) errors can be reported as a PCI Express Uncorrectable Error, and/or by interrupt (INTx, MSI, or PEX_INTA#) signaling, by the FATAL_ERR# output:</p> <ul style="list-style-type: none"> Reporting of the specific error condition in the Device-Specific Error Status x register bit(s), if not masked in their corresponding Device-Specific Error Mask x register bit(s) (Port 0, 8, or 16, offsets 700h, 708h, 710h, and/or 718h (Status) and offsets 704h, 70Ch, 714h, and/or 71Ch (Mask)). Uncorrectable Internal error in the Uncorrectable Error Status register <i>Uncorrectable Internal Error Status</i> bit (Port 0, 8, or 16, offset FB8h[22]) is defined as <i>Fatal</i> in the Uncorrectable Error Severity register <i>Uncorrectable Internal Error Severity</i> bit (Port 0, 8, or 16, offset FC0h[22]), and Reporting of Uncorrectable Internal errors is enabled (not masked) by the Uncorrectable Error Mask register <i>Uncorrectable Internal Error Mask</i> bit (Port 0, 8, or 16, offset FBCh[22]), and Device Control register <i>Fatal Error Reporting Enable</i> bit (offset 70h[2]) or PCI Command register <i>SERR# Enable</i> bit (offset 04h[8]) is Set <p>The Device Status register <i>Fatal Error Detected</i> bit (offset 70h[18]) is Set, and the specific error is flagged in the Uncorrectable Error Status register (offset FB8h).</p> <p style="text-align: right;">Continued...</p>		

Table 3-9. Device-Specific Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
FATAL_ERR#	C24	I/O, TS	No	—
		<p>Continued...</p> <p>Software can be used to de-assert FATAL_ERR#, with the following procedure:</p> <ol style="list-style-type: none"> 1. Set the Port's ECC Error Check Disable register <i>Software Force Error Enable</i> bit (Downstream Ports, offset 720h[2]). 2. Write 5h to bits [11:8] of the Uncorrectable Error Status register (offset FB8h), in addition to Clearing <i>Status</i> bits that are Set, using a Read-Modify-Write operation. When the Port's <i>Software Force Error Enable</i> bit is Set, writing 1 to an <i>Error Status</i> bit that is Cleared causes that bit to be Set, and generates the corresponding ERR_FATAL or ERR_NONFATAL Message, if enabled and not masked. Therefore, software should not, <i>for example</i>, write all 1s to this register while the Port's <i>Software Force Error Enable</i> bit is Set. 3. Clear the Port's <i>Software Force Error Enable</i> bit. <p>If FATAL_ERR# output is not used, this signal can remain unconnected.</p> <p><i>Notes:</i> Although this is an I/O signal with tri-statable output, its logical operation is output that is always driven.</p> <p>Device-Specific errors (RAM ECC errors) are reported in the lowest numbered enabled Port within the Station.</p>		

Table 3-9. Device-Specific Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
GPIO[10, 7:6, 3:1]	AD2, Y3, W5, AE1, AB3, AB1	GPIO7 – I/O, PD, GPIO[10, 6, 3:1] – I/O, PU	No	–
		General-Purpose I/O (6 Balls) GPIO[10, 7:6, 3:1] provide GPIO functionality, determined according to the GPIO registers associated with each GPIO (Port 0, offsets 600h through 63Ch). GPIO interrupts are described in Section 9.5, “General-Purpose Input/Output.”		
PEX_INTA#	D1	OD	No	–
		Interrupt Output PEX_INTA# Interrupt output is enabled if: <ul style="list-style-type: none"> INTx Messages are enabled (Port’s PCI Command register Interrupt Disable bit, offset 04h[10], is Cleared), and MSIs are disabled (Port’s MSI Control register MSI Enable bit, offset 48h[16], is Cleared) PEX_INTA# output is enabled (ECC Error Check Disable register Enable PEX_INTA# Interrupt Output(s) for x Interrupt bit(s) (Port 0, 8, or 16, offset 720h[6] and/or 4) are Set) The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources: <ul style="list-style-type: none"> Conventional PCI INTx Message generation Native MSI transaction generation Device-Specific PEX_INTA# assertion PEX_INTA# assertion (Low) indicates that one or more of the following events and/or errors (if not masked) were detected: <ul style="list-style-type: none"> Link State events PCI Express Hot Plug events General-Purpose Input Interrupt events Refer to Section 9.1.1, “Interrupt Sources or Events,” for details. If used, PEX_INTA# output requires an external pull-up resistor; otherwise, this output can remain unconnected.		

Table 3-9. Device-Specific Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PORT_GOOD[9:8, 5:4, 0]#	AC3, AC2, AD1, AB2, D3	PORT_GOOD8# – I/O, PD, PORT_GOOD[9, 5:4, 0]# – I/O, PU	No	Refer to STRAP_TESTMODE0
		<p>Active-Low PCI Express Port Linkup Status Indicator Outputs –or– Programmable General-Purpose I/O (5 Balls)</p> <p>PORT_GOODx# signals can function as PORT_GOODx# outputs or General-Purpose input/output (I/O). Default functionality for all PORT_GOODx# signals is selected according to the STRAP_TESTMODE0 input state (sampled at Fundamental Reset (PEX_PERST#) de-assertion), and the functionality of each signal can be programmed by the serial EEPROM, I²C/SMBus, and/or software.</p> <p>The General-Purpose Input/Output (GPIO) signals can function independently, as General Purpose inputs (default functionality), General-Purpose outputs, or Interrupt inputs (that can trigger interrupt outputs using MSI Writes, INTx Messages, or PEX_INTA# signaling).</p> <p>Notes: <i>Table 4-1 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i></p> <p><i>PORT_GOOD[9:8, 5:4, 0]# signals that are enabled to function as PORT_GOODx# outputs correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals that are enabled to function as PORT_GOODx# outputs can be re-assigned to any Port, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h.</i></p> <p><i>PORT_GOODx# signals that are enabled to function as GPIO are always mapped to Port 0 registers.</i></p> <p style="text-align: right;">Continued...</p>		

Table 3-9. Device-Specific Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PORT_GOOD[9:8, 5:4, 0]#	AC3, AC2, AD1, AB2, D3	PORT_GOOD8# – I/O, PD, PORT_GOOD[9, 5:4, 0]# – I/O, PU	No	Refer to STRAP_TESTMODE0
		<p>Continued...</p> <p>PORT_GOOD Output Function</p> <p>For PORT_GOODx# signals that are assigned to enabled Ports (according to the Port Good Selector x register(s), Port 0), offset(s) 6A0h through 6A8h) and are configured for PORT_GOOD output functionality (by the STRAP_TESTMODE0 input state, sampled at Fundamental Reset), or by subsequent programming (by serial EEPROM, I²C, and/or software) of the appropriate GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and/or 604h) value(s). The output states are not directly available from a single register (due to encoded, possibly blinking output); however, software can determine LANE_GOOD status (Physical Layer Link status for each Lane) from the Station x Lane Status register(s) <i>Lane x Up Status</i> bits (Port 0, offset(s) 330h[31:0] and 334h[15:0]). Software can also determine the Port's Maximum Link Width and Maximum Link Speed, from the Port's Link Capability register (offset 74h[9:4 and 3:0], respectively), as well as the Port's Negotiated Link Width and Current Link Speed, from the Port's Link Status register (offset 78h[25:20 and 19:16], respectively).</p> <p>If PORT_GOOD output functionality is enabled, but some Ports are not enabled due to the STRAP_STNx_PORTCFG0 input states, the PORT_GOODx# signals associated with non-enabled Ports function as GPIOx signals.</p> <p>LED behavior when connected to PORT_GOODx# signals:</p> <ul style="list-style-type: none"> • Off – Link is Down • Blinking, 512 ms On, 512 ms Off (1 Hz) – Link is Up, 2.5 GT/s, any negotiated width • Blinking, 256 ms On, 256 ms Off (2 Hz) – Link is Up, 5.0 GT/s, any negotiated width • On – Link is Up, 8.0 GT/s, any negotiated width <p>The PORT_GOODx#/GPIOx I/Os operate from the VDD18 supply, and maximum input voltage is 2.5V. Because LED forward voltage drop is typically greater than 1.8V, the LED voltage source will likely be higher than 2.5V. In this case, if the LED is connected directly to the PORT_GOODx# input, the input voltage level (while the LED is turned Off) would exceed the specification. Therefore, a PORT_GOODx# signal typically cannot drive an LED directly; however, it can be used to gate a transistor that switches the LED On and Off.</p> <p>For further details regarding LED behavior, refer to Section 12.7, “Port Good Status LEDs.”</p> <p style="text-align: right;">Continued...</p>		

Table 3-9. Device-Specific Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PORT_GOOD[9:8, 5:4, 0]#	AC3, AC2, AD1, AB2, D3	PORT_GOODx# – I/O, PD, PORT_GOOD[9, 5:4, 0]# – I/O, PU	No	Refer to STRAP_TESTMODE0
		<p>Continued...</p> <p>General-Purpose Inputs</p> <p>For PORT_GOODx# signals that are configured as General-Purpose inputs (by the STRAP_TESTMODE0 input state, sampled at Fundamental Reset), or by subsequent programming (by serial EEPROM, I²C, and/or software) of the appropriate GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and/or 604h) value(s), input states are reflected in the GPIO 0_10 Input Data register (Port 0, offset 61Ch).</p> <p>Inputs can be internally de-bounced, by Setting the corresponding GPIO 0_10 Input De-Bounce register bits (Port 0, offset 614h). De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched.</p> <p>General-Purpose Outputs</p> <p>For PORT_GOODx# signals that are configured as General-Purpose outputs in the GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and/or 604h), output states are controlled by the corresponding GPIO 0_10 Output Data register (Port 0, offset 624h) bit values.</p> <p>Interrupt Inputs</p> <p>For PORT_GOODx# signals that are configured as Interrupt inputs in the GPIO 0_x Direction Control register <i>Direction Control</i> bit(s), input states are reflected in the GPIO 0_10 Interrupt Status register (Port 0, offset 634h).</p> <p>Inputs can be internally de-bounced, by Setting the corresponding GPIO 0_10 Input De-Bounce register (Port 0, offset 614h) bits. De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched.</p> <p>Interrupt polarity (Active-High or Active-Low) is individually programmable in the GPIO 0_10 Interrupt Polarity register (Port 0, offset 62Ch).</p> <p>Interrupt generation can be selectively masked in the GPIO 0_10 Interrupt Mask register (Port 0, offset 63Ch). If a GPIO 0_10 Interrupt Mask register bit is Set, a read of the corresponding GPIO 0_10 Interrupt Status register <i>Interrupt Status</i> bit returns a value of 0.</p>		

3.4.7 External Resistor Signals – 27 x 27 mm² Package

Table 3-10. External Resistor Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
REXT_A[11:0]	D18, E24, N23, Y25, D9, A3, H3, N4, AB24, AC18, AC9, Y4	A	No	–
		External Bias Resistor Balls (12 Balls) One REXT_Ax ball is provided for each SerDes quad, per Station. An external resistor (3.00KΩ, 1%) must be connected between each REXT_Ax ball and VSS (Ground). Each resistor should be placed close to the PEX 8747, for minimal noise injection. Bypass capacitors must not be connected to these balls. <i>Note: A 3.01K 0.1% resistor can be used, because that value is within the 3.00K ±1% specification.</i>		
REXT_B[11:0]	E18, F18, N22, W23, E9, C1, G3, N5, Y22, AB18, AB9, Y5	A	No	–
		External Bias Resistor Balls (12 Balls) One REXT_Bx ball is provided for each SerDes quad, per Station. An external resistor (3.00KΩ, 1%) must be connected between each REXT_Bx ball and VSS (Ground). Each resistor should be placed close to the PEX 8747, for minimal noise injection. Bypass capacitors must not be connected to these balls. <i>Note: A 3.01K 0.1% resistor can be used, because that value is within the 3.00K ±1% specification.</i>		
REXT_CMU	Y1	A	No	–
		Clock Management Unit for SerDes An external resistor (3.00KΩ, 1%) must be attached between REXT_CMU and VSS (Ground). <i>Note: A 3.01K 0.1% resistor can be used, because that value is within the 3.00K ±1% specification.</i>		

3.4.8 Thermal Diode Signals – 27 x 27 mm² Package

The PEX 8747 includes a thermal-sensing diode, to facilitate the measurement of on-die device junction temperature. On the package level, the thermal diode inputs listed in [Table 3-11](#) connect to anode and cathode terminals of a diode-connected transistor (PNP) implemented on the die.

For further details, refer to [Section 12.8, “Thermal Sensor Diode – 27 x 27 mm² Package.”](#)

Table 3-11. Thermal Diode Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
THERMAL_DIODEn	AC24	I	No	–
		Thermal Diode Negative THERMAL_DIODEn can be connected to the negative terminal of a Temperature Sensor IC, to monitor the approximate temperature of the die. <i>Note: Subtract 24°C from the temperature value reported by the Temperature Sensor IC, to determine the correct die temperature.</i>		
THERMAL_DIODEp	AF25	I	No	–
		Thermal Diode Positive THERMAL_DIODEp can be connected to the positive terminal of a Temperature Sensor IC, to monitor the approximate temperature of the die. <i>Note: Subtract 24°C from the temperature value reported by the Temperature Sensor IC, to determine the correct die temperature.</i>		

3.4.9 No Connect Signals – 27 x 27 mm² Package

Caution: *Do not connect these balls to board electrical paths.
These balls are internally connected to the device.*

Table 3-12. No Connect Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
N/C	A9, A18, A24, B9, B18, B24, B25, B26, C25, D24, D25, D26, E1, F1, F9, F24, F25, G21, G22, N1, N2, N25, N26, W1, W2, W4, W21, W22, W24, W25, Y2, Y23, Y24, AA9, AA24, AA25, AA26, AB25, AB26, AC26, AD24, AD26, AE2, AE3, AE18, AE26, AF2, AF3, AF18	<i>Reserved</i>	No	–
		No Connect (49 Balls) Do not connect these balls to board electrical paths.		
SPARE3	AA1	I/O, PD	No	–
		Spare 3 <i>Reserved for future use</i> Note: Normally, this I/O should be pulled Low to VSS (Ground). Optionally, this I/O can remain unconnected, because the internal pull-down resistor holds the input Low.		
SPARE2	AA2	I/O, PU	No	–
		Compatibility Enable for Non-Compliant Gen 1 Endpoints When SPARE2 is Low and the Link training sequence fails during either the LTSSM <i>Polling</i> or <i>Configuration</i> state, the next time the LTSSM exits the <i>Detect</i> state, TS Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support. When SPARE2 is High, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 3 data rate and Autonomous Change. Notes: This feature should be enabled only if a non-compliant Gen 1 device will not linkup if these Data Rate Identifier bits are Set. Normally, this I/O should be pulled High to VDD18 . Although this is an I/O signal, its logical operation is input. Optionally, this I/O can remain unconnected, because the internal pull-up resistor holds the input High.		

Table 3-12. No Connect Signals – 27 x 27 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
SPARE1	AA3	I/O, PU	No	—
		Spare 1 <i>Reserved for future use</i> <i>Note:</i> Normally, this I/O should be pulled High to VDD18 . Optionally, this I/O can remain unconnected, because the internal pull-up resistor holds the input High.		
SPARE0	D2	I/O, PU	No	—
		Spare 0 <i>Reserved for future use</i> <i>Note:</i> Normally, this I/O should be pulled High to VDD18 . Optionally, this I/O can remain unconnected, because the internal pull-up resistor holds the input High.		

3.4.10 Power and Ground Signals – 27 x 27 mm² Package

In general, each power ball should connect to one de-coupling capacitor. Use a mix of values, *such as* 0.1 and 0.01 μ F.

Due to VDD09 in-rush current at the moment **PEX_PERST#** input is de-asserted, bulk capacitance is needed, to prevent the voltage rail from falling below minimum voltage requirements. *For example*, the PEX 8747 RDK uses three 680 μ F capacitors for this. This particular capacitance value is not required; however, it is best to use multiple capacitors in parallel. Inductance must be low.

Table 3-13. Power and Ground Signals – 27 x 27 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
VDD09	L11, L13, L15, M12, M14, M16, N11, N13, N15, P12, P14, P16, R11, R13, R15, T12, T14, T16	CPWR	No	–
		0.9V -5%, +5.55% Power for Core and SerDes Digital Logic (18 Balls)		
VDD09A	G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, J7, J11, J13, J14, J16, J20, K7, K20, L7, L9, L18, L20, M7, M9, M18, M20, N7, N20, P7, P9, P18, P20, R7, R10, R17, R20, T7, T9, T18, T20, U7, U20, V11, V13, V14, V16, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18	APWR	No	–
		0.9V -5%, +5.55% Power for SerDes Analog Circuits (56 Balls)		
VDD18	G7, G20, H8, H19, J9, J18, K10, K17, U10, U17, V8, V9, V18, V19, W7, W8, W19, W20, Y7, Y20	I/OPWR	No	–
		1.8V -5%, +10% Power for I/O Logic Functions (20 Balls)		
VDD18A	K12, K15, N10, N17, U12, U15	PLL PWR	No	–
		1.8V -5%, +10% Power for PLL Circuits (6 Balls)		
VSS	A1, A4, A23, A25, A26, B4, B23, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, D4, D23, E4, E23, F4, F5, F6, F7, F8, F10, F11, F12, F13, F14, F15, F16, F17, F19, F20, F21, F22, F23, G8, G19, H1, H2, H4, H5, H6, H7, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H20, H21, H22, H23, H25, H26, J3, J6, J8, J10, J12, J15, J17, J19, J21, J24, K3, K6, K8, K9, K11, K13, K14, K16, K18, K19, K21, K24, L3, L6, L8, L10, L12, L14, L16, L17, L19, L21, L24, M3, M6, M8, M10, M11, M13, M15, M17, M19, M21, M24, N3, N8, N9, N12, N14, N16, N18, N19, N24, P3, P6, P8, P10, P11, P13, P15, P17, P19, P21, P24, R3, R6, R8, R9, R12, R14, R16, R18, R19, R21, R24, T3, T6, T8, T10, T11, T13, T15, T17, T19, T21, T24, U3, U6, U8, U9, U11, U13, U14, U16, U18, U19, U21, U24, V1, V2, V3, V4, V5, V6, V7, V10, V12, V15, V17, V20, V21, V22, V23, V24, V25, V26, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, Y8, Y19, AA4, AA5, AA6, AA7, AA8, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA19, AA20, AA21, AA22, AA23, AB4, AB23, AC4, AC23, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AE4, AE23, AF1, AF4, AF23, AF26	GND	No	–
		Ground Connections (246 Balls)		

3.5 Signal Ball Descriptions – 19 x 21 mm² Package

Notes: *If there is more than one ball per signal name that includes a numbered range, the locations are listed in the same sequence in which the range is listed, starting at the top row, from left to right. For example, PEX_PERn11 is located at AE17, PEX_PERn10 is located at AE16, and so forth.*

If there is more than one ball per signal name that does not include a numbered range (such as VDD09), the locations are listed in ascending alphanumeric order.

For signal names and locations of the 27 x 27 mm² package, refer to [Section 3.4](#).

The following signals exist only in the 27 x 27 mm² package; they do not exist in the 19 x 21 mm² package – STRAP_GEN1_GEN2, STRAP_PROBE_MODE#, STRAP_RESERVED[18, 12:0, 4:1], STRAP_SERDES_MODE_EN#, STRAP_UPSTRM_PORTSEL2, THERMAL_DIODEn, and THERMAL_DIODEp.

The PEX 8747 signals associated with the 19 x 21 mm² package are divided into the following groups:

- [PCI Express Signals – 19 x 21 mm² Package](#)
- [Serial EEPROM Signals – 19 x 21 mm² Package](#)
- [Strapping Signals – 19 x 21 mm² Package](#)
- [JTAG Interface Signals – 19 x 21 mm² Package](#)
- [I2C/SMBus Slave Interface Signals – 19 x 21 mm² Package](#)
- [Device-Specific Signals – 19 x 21 mm² Package](#)
- [External Resistor Signals – 19 x 21 mm² Package](#)
- [No Connect Signals – 19 x 21 mm² Package](#)
- [Power and Ground Signals – 19 x 21 mm² Package](#)

3.5.1 PCI Express Signals – 19 x 21 mm² Package

Table 3-14 defines the PCI Express SerDes and Control signals.

Table 3-14. PCI Express Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PEX_PERn[15:0]	AE23, AE22, AE20, AE19, AE17, AE16, AE14, AE13, AE11, AE10, AE8, AE7, AE5, AE4, AE2, AE1	CMLRn	No	–
		Negative Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)		
PEX_PERn[31:16]	D11, D10, D8, D7, D5, D4, D2, D1, H4, J4, L4, M4, P4, R4, U5, V5	CMLRn	No	–
		Negative Half of PCI Express Receiver Differential Signal Pairs for Station 1 (16 Balls)		
PEX_PERn[47:32]	D13, D14, D16, D17, D19, D20, D22, D23, H20, J20, L20, M20, P20, R20, U20, V20	CMLRn	No	–
		Negative Half of PCI Express Receiver Differential Signal Pairs for Station 2 (16 Balls)		
PEX_PERp[15:0]	AD23, AD22, AD20, AD19, AD17, AD16, AD14, AD13, AD11, AD10, AD8, AD7, AD5, AD4, AD2, AD1	CMLRp	No	–
		Positive Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)		
PEX_PERp[31:16]	E11, E10, E8, E7, E5, E4, E2, E1, H5, J5, L5, M5, P5, R5, U4, V4	CMLRp	No	–
		Positive Half of PCI Express Receiver Differential Signal Pairs for Station 1 (16 Balls)		
PEX_PERp[47:32]	E13, E14, E16, E17, E19, E20, E22, E23, H19, J19, L19, M19, P19, R19, U19, V19	CMLRp	No	–
		Positive Half of PCI Express Receiver Differential Signal Pairs for Station 2 (16 Balls)		
PEX_PERST#	V7	I, PU	No	–
		PCI Express Reset Used to cause a Fundamental Reset. Refer to Section 5.1, “Reset,” for further details.		

Table 3-14. PCI Express Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PEX_PETn[15:0]	AB23, AB22, AB20, AB19, AB17, AB16, AB14, AB13, AB11, AB10, AB8, AB7, AB5, AB4, AB2, AB1	CMLTn	No	–
		Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls) PEX_PETn[15:0] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETn[31:16]	A11, A10, A8, A7, A5, A4, A2, A1, H1, J1, L1, M1, P1, R1, U1, V1	CMLTn	No	–
		Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (16 Balls) PEX_PETn[31:16] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETn[47:32]	A13, A14, A16, A17, A19, A20, A22, A23, H23, J23, L23, M23, P23, R23, U23, V23	CMLTn	No	–
		Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (16 Balls) PEX_PETn[47:32] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETp[15:0]	AA23, AA22, AA20, AA19, AA17, AA16, AA14, AA13, AA11, AA10, AA8, AA7, AA5, AA4, AA2, AA1	CMLTp	No	–
		Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls) PEX_PETp[15:0] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETp[31:16]	B11, B10, B8, B7, B5, B4, B2, B1, H2, J2, L2, M2, P2, R2, U2, V2	CMLTp	No	–
		Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 1 (16 Balls) PEX_PETp[31:16] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_PETp[47:32]	B13, B14, B16, B17, B19, B20, B22, B23, H22, J22, L22, M22, P22, R22, U22, V22	CMLTp	No	–
		Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 2 (16 Balls) PEX_PETp[47:32] must be AC-coupled. Use a 0.22 µF capacitor.		
PEX_REFCLKn	W2	HCSLn	No	–
		Negative Half of 100-MHz PCI Express Constant Frequency Reference Clock Input Signal Pair An internal coupling capacitor is provided (an external capacitor is not needed).		
PEX_REFCLKp	W3	HCSLp	No	–
		Positive Half of 100-MHz PCI Express Constant Frequency Reference Clock Input Signal Pair An internal coupling capacitor is provided (an external capacitor is not needed).		

3.5.2 Serial EEPROM Signals – 19 x 21 mm² Package

The PEX 8747 includes four signals for interfacing to a serial EEPROM, defined in [Table 3-15](#). The serial EEPROM is used to load register values immediately following Reset (PEX_PERST# or Hot Reset/DL_Down). Most registers can be programmed by serial EEPROM, as indicated in the register descriptions.

For information regarding serial EEPROM use, refer to [Chapter 6, “Serial EEPROM Controller.”](#)

Table 3-15. Serial EEPROM Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
EE_CS#	K19	I/O, PU	No	–
		Active-Low Serial EEPROM Chip Select Output <i>Note:</i> Although this is an I/O signal, its logical operation is output.		
EE_DI	F19	I/O, TS	No	–
		PEX 8747 Output to Serial EEPROM Data Input <i>Note:</i> Although this is an I/O signal with tri-statable output, its logical operation is output that is always driven.		
EE_DO	R18	I/O, PU	No	–
		PEX 8747 Input from Serial EEPROM Data Output Should be pulled High to VDD18 . <i>Note:</i> Although this is an I/O signal, its logical operation is input.		
EE_SK	F22	I/O, PU	No	–
		Serial EEPROM Clock Frequency Output Programmable, by way of the Serial EEPROM Clock Frequency register EepFreq[2:0] field (Port 0, offset 268h[2:0]), to the following: <ul style="list-style-type: none"> • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz <i>Note:</i> Although this is an I/O signal, its logical operation is output.		

3.5.3 Strapping Signals – 19 x 21 mm² Package

Note: Table 4-1 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.

The PEX 8747 Strapping signals, described in Table 3-16, define the configuration of Upstream Port assignment, Link width, and various setup and test modes.

Many of the Strapping signals are I/O 3-state inputs (indicated in Table 3-16 as “I/O, 3-state input”), which can be High (1), Low (0), or High-Impedance (Z; not connected/floating).

Strapping signals that have 2-state inputs (rather than 3-state inputs) use internal pull-up and pull-down resistors to define the default configuration; if the PEX 8747 configuration must be changed from the default, external pull-up and/or pull-down resistors can be connected. External resistors are not required unless the Strapping signals:

- Must be changed from the default logic state, –or–
- Are connected to circuit traces (the internal resistors are relatively weak, and may not be sufficiently strong, to hold circuit traces to the default input states)

After a Fundamental Reset, the **Link Capability**, **Port Configuration**, and **Upstream Port** registers (offsets 74h, 300h, and 360h, respectively) capture Strapping ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the serial EEPROM. I²C/SMBus can also change Strapping ball Configuration data; however, the STRAP_I2C_SMBUS_CFG_EN# input should be Low, to prevent linkup and Host enumeration. Then, when I²C programming is complete, I²C/SMBus should lastly Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]), to enable linkup and allow subsequent Host enumeration.

Table 3-16. Strapping Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State										
		Description												
STRAP_I2C_SMBUS_CFG_EN#	Y3	I/O, PU	No	—										
		I²C Bus Configuration Enable Enables or disables the I ² C/SMBus for initial device configuration prior to initial Link training. Must be pulled or tied High to VDD18 or Low to VSS (Ground). L = Enables I ² C/SMBus for initial device configuration. The serial EEPROM can also be used in this mode. After I ² C and/or the serial EEPROM Sets the Configuration Release register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]), all Ports start Link training. H = Disables I ² C/SMBus for initial device configuration. The <i>Initiate Configuration</i> bit is Set by hardware, immediately after the PEX 8747 comes out of reset. After the serial EEPROM load finishes, all Ports start Link training (assuming that the serial EEPROM does not Clear the <i>Initiate Configuration</i> bit). <i>Notes: The Delayed Linkup option might require software support to delay Host enumeration until I²C/SMBus completes switch initialization (by Setting the Initiate Configuration bit; otherwise system software could miss detection of the PCI Express hierarchy (precluding device enumeration)).</i> <i>Although this is an I/O signal, its logical operation is input.</i>												
STRAP_I2C_SMBUS_EN	F4	I/O, 3-state input	No	—										
		I²C/SMBus Protocol Select Enable Selects the I ² C or SMBus protocol, and defines the default SMBus Configuration register <i>SMBus Enable</i> and <i>ARP Disable</i> bit (Port 0, offset 2C8h[0 and 8], respectively) values, as listed below. <table><tr><th>STRAP_I2C_SMBUS_EN Input State</th><th>SMBus Enable Value</th><th>ARP Disable Value</th></tr><tr><td>0</td><td>0</td><td>—</td></tr><tr><td>Z</td><td>1</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table> 0 = Enables I ² C Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus Z, 1 = Enables SMBus with ARP, on the I2C_SCL0 and I2C_SDA0 2-wire bus			STRAP_I2C_SMBUS_EN Input State	SMBus Enable Value	ARP Disable Value	0	0	—	Z	1	0	1
STRAP_I2C_SMBUS_EN Input State	SMBus Enable Value	ARP Disable Value												
0	0	—												
Z	1	0												
1	1	1												
STRAP_PLL_BYPASS#	V17	I, PU	No	—										
		Factory Test Only Must be pulled or tied High to VDD18 .												
STRAP_RESERVED[21:20], STRAP_RESERVED19#, STRAP_RESERVED[16:14, 9, 7, 5, 0]	AD3, AD6, B12, V14, W14, AD12, B18, K3, AD9, V18	I	No	—										
		Factory Test Only (10 Balls) Reserved for future use Refer to Table 3-17 for specific pull-up/pull-down resistor requirements.												

Table 3-16. Strapping Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
STRAP_STN1_PORTCFG0	H10	I/O, 3-state input	No	—
		Strapping Signal to Select Port Configuration for Station 1 (Quantity of Enabled Ports (1 or 2), and Maximum Quantity of Lanes for Each Specific Port) Defines the enabled Port Numbers and their Link widths, for Station 1. Programs the Port Configuration register <i>Port Configuration for Station 1</i> field (Port 0, offset 300h[5:3]) default value. 0 = 0 = <i>Reserved</i> Z = 1 = x16 1 = 2 = x8x8		
STRAP_STN2_PORTCFG0	N19	I/O, 3-state input	No	—
		Strapping Signal to Select Port Configuration for Station 2 (Quantity of Enabled Ports (1 or 2), and Maximum Quantity of Lanes for Each Specific Port) Defines the enabled Port Numbers and their Link widths, for Station 2. Programs the Port Configuration register <i>Port Configuration for Station 2</i> field (Port 0, offset 300h[8:6]) default value. 0 = 0 = <i>Reserved</i> Z = 1 = x16 1 = 2 = x8x8		

Table 3-16. Strapping Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
STRAP_TESTMODE0	V13	I/O, 3-state input	No	—
		Test Mode Select The STRAP_TESTMODE0 input state (first value listed below) indicates the test mode (second value listed below), which defines the default functionality of the PORT_GOODx# and GPIOx signals. 0 = 0 = PORT_GOOD[9:8, 5:4, 0]# functionality defaults to PORT_GOOD for Ports 17, 16, 9, 8, and 0, respectively Z = 1 = <i>Factory Test Only</i> 1 = 2 = PORT_GOOD[9:8, 5:4, 0]# and GPIO[10, 7:6, 3:1] functionality defaults to GPIO input		
STRAP_UPSTRM_PORTS EL[1:0]	M18, H18	I/O, 3-state input	No	—
		Select Upstream Port (2 Balls) Select any Port as the Upstream Port. These inputs map to the Upstream Port register <i>Upstream Port</i> field (Port 0, offset 360h[4:0]). If I ² C/SMBus is used to configure the PEX 8747, the STRAP_I2C_SMBUS_CFG_EN# input can be pulled or tied Low, to delay linkup until I ² C/SMBus initialization is complete. After I ² C initialization is complete, I ² C/SMBus must then Set the Configuration Release register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]).		
		STRAP_UPSTRM_PORTSEL[1:0] Input States^a	Offset 360h[4:0] Value	Port Number
		00	0_0000b	0
		11	0_1000b	8
		—	0_1001b	9
		—	1_0000b	16
		—	1_0001b	17
		<i>a. The STRAP_UPSTRM_PORTSEL[1:0] inputs select either Port 0 or Port 8 as the Upstream Port; if Port 9, 16, or 17 is needed as the Upstream Port, use the serial EEPROM (if present) and/or I²C/SMBus (when STRAP_I2C_SMBUS_CFG_EN# is asserted) to program the Upstream Port field accordingly.</i>		

Table 3-17. Factory Test Only STRAP_RESERVED[21:20], STRAP_RESERVED19#, STRAP_RESERVED[16:14, 9, 7, 5, 0] Input External Pull-Up/Pull-Down Resistor Requirements

Ball/Signal Name	Location	PU/PD	Pull-Up/Pull-Down Requirement
STRAP_RESERVED21	AD3	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED20	AD6	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED19#	B12	PU	Pull High to VDD18 ; can optionally remain unconnected, due to its internal pull-up resistor.
STRAP_RESERVED16	V14	–	Must be tied directly to VSS (Ground).
STRAP_RESERVED15	W14	–	Must be pulled High to VDD18 .
STRAP_RESERVED14	AD12	–	Must be pulled High to VDD18 .
STRAP_RESERVED9	B18	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED7	K3	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED5	AD9	–	Must be pulled or tied Low to VSS (Ground).
STRAP_RESERVED0	V18	PU	Pull or tie High to VDD18 ; can optionally remain unconnected, due to its internal pull-up resistor.

3.5.4 JTAG Interface Signals – 19 x 21 mm² Package

The PEX 8747 includes five signals for performing JTAG boundary scan, defined in [Table 3-18](#). The JTAG interface is described in [Section 12.6, “JTAG Interface.”](#)

Table 3-18. JTAG Interface Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
JTAG_TCK	G11	I, PD	No	–
		JTAG Test Clock Input JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 15 MHz.		
JTAG_TDI	J6	I, PD	No	–
		JTAG Test Data Input Serial input to the JTAG TAP Controller, for test instructions and data.		
JTAG_TDO	F11	I/O, TS	No	–
		JTAG Test Data Output Serial output from the JTAG TAP Controller test instructions and data. <i>Note: Although this is an I/O signal with tri-statable output, its logical operation is output that is driven when the TAP Controller is being used; otherwise, the output is High-Impedance.</i>		
JTAG_TMS	H11	I, PD	No	–
		JTAG Test Mode Select Input decoded by the JTAG TAP Controller, to control test operations.		
JTAG_TRST#	F3	I, PD	No	–
		JTAG Test Reset Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the JTAG_TRST# input should be driven Low, or pulled Low to VSS (Ground) through a 1.5K Ω resistor, to place the JTAG TAP Controller into the <i>Test-Logic-Reset</i> state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the <i>Test-Logic-Reset</i> state by initializing the JTAG TAP Controller's Instruction register to contain the <i>IDCODE</i> instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.		

3.5.5 I²C/SMBus Slave Interface Signals – 19 x 21 mm² Package

Table 3-19 defines the three I²C/SMBus Slave interface signals. The I²C/SMBus Slave interface provides access to the PEX 8747 registers. Most registers that can be programmed by serial EEPROM (including registers that are Read Only to PCI Express), can be also programmed by I²C/SMBus. However, I²C/SMBus cannot replace the serial EEPROM programming of some registers, *such as* SerDes- and Hot Plug-related registers that (generally) must be configured prior to automatic link training, immediately following Reset. I²C/SMBus can also be used to program the serial EEPROM.

The I²C/SMBus Slave interface used with PLX software is a powerful debugging tool that enables register access, regardless of whether the PCI Express Link is Up. Figure 3-1 illustrates the suggested Header pin layout on 0.1-inch centers, for direct connection to the Total Phase Aardvark I²C-USB converter (as used with PLX Rapid Development Kits (RDKs)).

For further details, refer to Chapter 7, “I²C/SMBus Slave Interface Operation.”

Figure 3-2. Suggested I²C Header Pin Layout on 0.1-Inch Centers

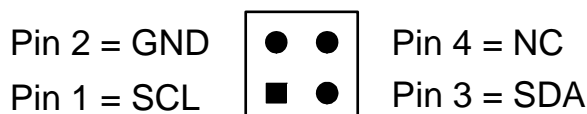


Table 3-19. I²C/SMBus Slave Interface Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State								
		Description										
I2C_ADDR0	F5	I/O, 3-state input	No	–								
		I²C Slave/SMBus Device Address Bit										
		Used to define the default value of the two least significant bits of the PEX 8747 I ² C/SMBus 7-bit Slave Address, which is programmable in both the I²C Configuration register <i>Slave Address</i> and SMBus Configuration register <i>SMBus Device Address</i> fields (Port 0, offsets 294h[6:0] and 2C8h[7:1], respectively). If I ² C or SMBus configuration is used, I2C_ADDR0 should be strapped to a unique address, to avoid an address conflict with any other I ² C/SMBus devices (on the same I ² C Bus/SMBus segment).										
		The three possible default I ² C Slave/SMBus Device Address values are listed below.										
		<table><tr><th>I2C_ADDR0 Input State</th><th>I²C Slave/SMBus Device Address</th></tr><tr><td>0</td><td>0111_000b (default)</td></tr><tr><td>Z</td><td>0111_001b</td></tr><tr><td>1</td><td>0111_010b</td></tr></table>			I2C_ADDR0 Input State	I ² C Slave/SMBus Device Address	0	0111_000b (default)	Z	0111_001b	1	0111_010b
		I2C_ADDR0 Input State	I ² C Slave/SMBus Device Address									
0	0111_000b (default)											
Z	0111_001b											
1	0111_010b											

Table 3-19. I²C/SMBus Slave Interface Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
I2C_SCL0	F7	OD	No	–
		I²C/SMBus Serial Clock Line I ² C/SMBus bidirectional Clock line. Data on the I ² C Bus can be transferred at rates of up to 100 kbit/s (Standard mode). Because the 1.8V signaling is less than the voltage defined by the I ² C Bus v2.1 (5V, 3.3V), external voltage translation circuitry might be required. I2C_SCL0 requires an external pull-up resistor. <i>Note: The PEX 8747 I²C/SMBus Slave Interface can stretch the Low period of the I²C/SMBus clock while a simultaneous in-band Request that also targets PEX 8747 registers is being processed.</i>		
I2C_SDA0	F2	OD	No	–
		I²C/SMBus Serial Data Line Transmits and receives I ² C/SMBus data during I ² C/SMBus accesses to PEX 8747 registers. Because the 1.8V signaling is less than the voltage defined by the I ² C Bus v2.1 (5V, 3.3V), external voltage translation circuitry might be required. I2C_SDA0 requires an external pull-up resistor.		

3.5.6 Device-Specific Signals – 19 x 21 mm² Package

Table 3-20 defines the Device-Specific signals – signals that are unique to the PEX 8747.

Table 3-20. Device-Specific Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
FATAL_ERR#	F14	I/O, TS	No	–
		<p>Fatal Error Output</p> <p>FATAL_ERR# is asserted Low when a Fatal error is detected in the PEX 8747 and the following conditions are met (all the same conditions that are required to send a Fatal Error Message to the Host).</p> <p>For <i>PCI Express Base r3.0</i> errors:</p> <ul style="list-style-type: none"> Specific error is defined as <i>Fatal</i> in the Uncorrectable Error Severity register (offset FC0h), and Reporting of the specific error condition is enabled (not masked) by the Uncorrectable Error Mask register's (offset FBCh) corresponding <i>Interrupt Mask</i> bit, and Device Control register <i>Fatal Error Reporting Enable</i> bit (offset 70h[2]) –or– PCI Command register <i>SERR# Enable</i> bit (offset 04h[8]) is Set <p>Device-Specific (RAM ECC) errors can be reported as a PCI Express Uncorrectable Error, and/or by interrupt (INTx, MSI, or PEX_INTA#) signaling, by the FATAL_ERR# output:</p> <ul style="list-style-type: none"> Reporting of the specific error condition in the Device-Specific Error Status x Mask x register bit(s), if not masked in their corresponding Device-Specific Error Mask x register bit(s) (Port 0, 8, or 16, offsets 700h, 708h, 710h, and/or 718h (Status) and offsets 704h, 70Ch, 714h, and/or 71Ch (Mask)). Uncorrectable Internal error in the Uncorrectable Error Status register <i>Uncorrectable Internal Error Status</i> bit (Port 0, 8, or 16, offset FB8h[22]) is defined as <i>Fatal</i> in the Uncorrectable Error Severity register <i>Uncorrectable Internal Error Severity</i> bit (Port 0, 8, or 16, offset FC0h[22]), and Reporting of Uncorrectable Internal errors is enabled (not masked) by the Uncorrectable Error Mask register <i>Uncorrectable Internal Error Mask</i> bit (Port 0, 8, or 16, offset FBCh[22]), and Device Control register <i>Fatal Error Reporting Enable</i> bit (offset 70h[2]) –or– PCI Command register <i>SERR# Enable</i> bit (offset 04h[8]) is Set <p>The Device Status register <i>Fatal Error Detected</i> bit (offset 70h[18]) is Set, and the specific error is flagged in the Uncorrectable Error Status register (offset FB8h).</p> <p>Continued...</p>		

Table 3-20. Device-Specific Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
FATAL_ERR#	F14	I/O, TS	No	–
		<p>Continued...</p> <p>Software can be used to de-assert FATAL_ERR#, with the following procedure:</p> <ol style="list-style-type: none"> 1. Set the ECC Error Check Disable register <i>Software Force Error Enable</i> bit (Downstream Ports, offset 720h[2]). 2. Write 5h to bits [11:8] of the Uncorrectable Error Status register (offset FB8h), in addition to Clearing <i>Status</i> bits that are Set, using a Read-Modify-Write operation. When the <i>Software Force Error Enable</i> bit is Set, writing 1 to an <i>Error Status</i> bit that is Cleared causes that bit to be Set, and generates the corresponding ERR_FATAL or ERR_NONFATAL Message, if enabled and not masked. Therefore, software should not, <i>for example</i>, write all 1s to this register while the <i>Software Force Error Enable</i> bit is Set. 3. Clear the Port's <i>Software Force Error Enable</i> bit. <p>If FATAL_ERR# output is not used, this signal can remain unconnected.</p> <p><i>Notes: Although this is an I/O signal with tri-statable output, its logical operation is output that is always driven.</i></p> <p><i>Device-Specific errors (RAM ECC errors) are reported in the lowest numbered enabled Port within the Station.</i></p>		
GPIO[10, 7:6, 3:1]	Y4, M6, Y6, V11, Y5, N3	GPIO7 – I/O, PD, GPIO[10, 6, 3:1] – I/O, PU	No	–
		<p>General-Purpose I/O (6 Balls)</p> <p>GPIO[10, 7:6, 3:1] provide GPIO functionality, determined according to the GPIO registers associated with each GPIO (Port 0, offsets 600h through 63Ch). GPIO interrupts are described in Section 9.5, “General-Purpose Input/Output.”</p>		

Table 3-20. Device-Specific Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PEX_INTA#	B6	OD	No	—
		<p>Interrupt Output</p> <p>PEX_INTA# Interrupt output is enabled if:</p> <ul style="list-style-type: none"> INT_x Messages are enabled (PCI Command register <i>Interrupt Disable</i> bit, offset 04h[10] is Cleared), and MSIs are disabled (MSI Control register <i>MSI Enable</i> bit, offset 48h[16] is Cleared) PEX_INTA# output (ECC Error Check Disable register <i>Enable PEX_INTA# Interrupt Output(s) for x Interrupt</i> bit(s) (Port 0, 8, or 16, offset 720h[6 and/or 4])) is enabled <p>Device-Specific (RAM ECC) errors can be signaled by interrupt, and/or as an Uncorrectable Internal error that is fatal (Uncorrectable Error Status register <i>Uncorrectable Internal Error Status</i> and Uncorrectable Error Severity register <i>Uncorrectable Internal Error Severity</i> bits (offsets FB8h[22] and FC0h[22], respectively, are Set).</p> <p>The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:</p> <ul style="list-style-type: none"> Conventional PCI INT_x Message generation Native MSI transaction generation Device-Specific PEX_INTA# assertion <p>PEX_INTA# assertion (Low) indicates that one or more of the following events and/or errors (if not masked) were detected:</p> <ul style="list-style-type: none"> Link State events PCI Express Hot Plug events General-Purpose Input Interrupt events Device-Specific Error conditions <p>Refer to Section 9.1.1, “Interrupt Sources or Events,” for details.</p> <p>If used, PEX_INTA# output requires an external pull-up resistor; otherwise, this output can remain unconnected.</p>		

Table 3-20. Device-Specific Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PORT_GOOD[9:8, 5:4, 0]#	W5, T3, W6, T2, B3	PORT_GOOD8# – I/O, PD, PORT_GOOD[9, 5:4, 0]# – I/O, PU	No	Refer to STRAP_TESTMODE0
		<p>Active-Low PCI Express Port Linkup Status Indicator Outputs –or– Programmable General-Purpose I/O (5 Balls)</p> <p>PORT_GOODx# signals can function as PORT_GOODx# outputs or General-Purpose input/output (I/O) signals. Default functionality for all PORT_GOODx# signals is selected according to the STRAP_TESTMODE0 input (sampled at Fundamental Reset (PEX_PERST#) de-assertion), and the functionality of each signal can be programmed by the serial EEPROM, I²C/SMBus, and/or software.</p> <p>The General-Purpose Input/Output (GPIO) signals can function independently, as General Purpose inputs (default functionality), General-Purpose outputs, or Interrupt inputs (that can trigger interrupt outputs using MSI Writes, INTx Messages, or PEX_INTA# signaling).</p> <p>Notes: Table 4-1 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p> <p>PORT_GOOD[9:8, 5:4, 0]# signals that are enabled to function as PORT_GOODx# outputs correspond to Ports 17, 16, 9, 8, and 0, respectively, by default.</p> <p>PORT_GOODx# signals that are enabled to function as PORT_GOODx# outputs can be re-assigned to any Port, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h.</p> <p>PORT_GOODx# signals that are enabled to function as GPIO are always mapped to Port 0 registers.</p> <p style="text-align: right;">Continued...</p>		

Table 3-20. Device-Specific Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PORT_GOOD[9:8, 5:4, 0]#	W5, T3, W6, T2, B3	PORT_GOOD8# – I/O, PD, PORT_GOOD[9, 5:4, 0]# – I/O, PU	No	Refer to STRAP_TESTMODE0
		<p>Continued...</p> <p>PORT_GOOD Output Function</p> <p>For PORT_GOODx# signals that are assigned to enabled Ports (according to the Port Good Selector x register(s), Port 0), offset(s) 6A0h through 6A8h) and are configured for PORT_GOOD output functionality (by the STRAP_TESTMODE0 input state, sampled at Fundamental Reset), or by subsequent programming (by serial EEPROM, I²C, and/or software) of the appropriate GPIO 0_x Direction Control register (Port 0, offset(s) 600h and/or 604h) values. The output states are not directly available from a single register (due to encoded, possibly blinking output); however, software can determine LANE_GOOD status (Physical Layer Link status for each Lane) from the Station x Lane Status register(s) <i>Lane x Up Status</i> bits (Port 0, offset(s) 330h[31:0] and 334h[15:0]). Software can also determine the Port's Maximum Link Width and Maximum Link Speed, from the Port's Link Capability register (offset 74h[9:4 and 3:0], respectively), as well as the Port's Negotiated Link Width and Current Link Speed, from the Port's Link Status register (offset 78h[25:20 and 19:16], respectively).</p> <p>If PORT_GOOD output functionality is enabled, but some Ports are not enabled due to the STRAP_STNx_PORTCFG0 input states, the PORT_GOODx# signals associated with non-enabled Ports function as GPIOx signals.</p> <p>LED behavior when connected to PORT_GOODx# signals:</p> <ul style="list-style-type: none"> • Off – Link is Down • Blinking, 512 ms On, 512 ms Off (1 Hz) – Link is Up, 2.5 GT/s, any negotiated width • Blinking, 256 ms On, 256 ms Off (2 Hz) – Link is Up, 5.0 GT/s, any negotiated width • On – Link is Up, 8.0 GT/s, any negotiated width <p>The PORT_GOODx#/GPIOx I/Os operate from the VDD18 supply, and maximum input voltage is 2.5V. Because LED forward voltage drop is typically greater than 1.8V, the LED voltage source will likely be higher than 2.5V. In this case, if the LED is connected directly to the PORT_GOODx# input, the input voltage level (while the LED is turned Off) would exceed the specification. Therefore, a PORT_GOODx# signal typically cannot drive an LED directly; however, it can be used to gate a transistor that switches the LED On and Off.</p> <p>For further details regarding LED behavior, refer to Section 12.7, “Port Good Status LEDs.”</p> <p>Continued...</p>		

Table 3-20. Device-Specific Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
PORT_GOOD[9:8, 5:4, 0]#	W5, T3, W6, T2, B3	PORT_GOOD8# – I/O, PD, PORT_GOOD[9, 5:4, 0]# – I/O, PU	No	Refer to STRAP_TESTMODE0
		<p>Continued...</p> <p>General-Purpose Inputs</p> <p>For PORT_GOODx# signals that are configured as General-Purpose inputs (by the STRAP_TESTMODE0 input state, sampled at Fundamental Reset), or by subsequent programming (by serial EEPROM, I²C, and/or software) of the appropriate GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and 604h) value(s), input states are reflected in the GPIO 0_10 Input Data register (Port 0, offset 61Ch).</p> <p>Inputs can be internally de-bounced, by Setting the corresponding GPIO 0_10 Input De-Bounce register (Port 0, offset 614h) bits. De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched.</p> <p>General-Purpose Outputs</p> <p>For PORT_GOODx# signals that are configured as General-Purpose outputs in the GPIO 0_9 Direction Control and/or GPIO 10 Direction Control register <i>Direction Control</i> bit(s) (Port 0, offsets 600h and 604h, respectively), output states are controlled by the corresponding GPIO 0_10 Output Data register (Port 0, offset 624h) bit values.</p> <p>Interrupt Inputs</p> <p>For PORT_GOODx# signals that are configured as Interrupt inputs in the GPIO 0_x Direction Control register <i>Direction Control</i> bit(s), input states are reflected in the GPIO 0_10 Interrupt Status register (Port 0, offset 634h).</p> <p>Inputs can be internally de-bounced, by Setting the corresponding GPIO 0_10 Input De-Bounce register (Port 0, offset 614h) bits. De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched.</p> <p>Interrupt polarity (Active-High or Active-Low) is individually programmable in the GPIO 0_10 Interrupt Polarity register (Port 0, offset 62Ch).</p> <p>Interrupt generation can be selectively masked in the GPIO 0_10 Interrupt Mask register (Port 0, offset 63Ch). If a GPIO 0_10 Interrupt Mask register bit is Set, a read of the corresponding GPIO 0_10 Interrupt Status register <i>Status</i> bit returns a value of 0.</p>		

3.5.7 External Resistor Signals – 19 x 21 mm² Package

Table 3-21. External Resistor Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
REXT_A[11:0]	G13, G14, K22, T21, F10, F8, G7, N2, W16, Y14, Y11, W11	A	No	–
		External Bias Resistor Balls (12 Balls) One REXT_Ax ball is provided for each SerDes quad, per Station. An external resistor (3.00KΩ, 1%) must be connected between each REXT_Ax ball and VSS (Ground). Each resistor should be placed close to the PEX 8747, for minimal noise injection. Bypass capacitors must not be connected to these balls. <i>Note: A 3.01K 0.1% resistor can be used, because that value is within the 3.00K \pm1% specification.</i>		
REXT_B[11:0]	H13, G16, G17, T22, G10, G8, L6, W7, W15, Y13, V10, Y10	A	No	–
		External Bias Resistor Balls (12 Balls) One REXT_Bx ball is provided for each SerDes quad, per Station. An external resistor (3.00KΩ, 1%) must be connected between each REXT_Bx ball and VSS (Ground). Each resistor should be placed close to the PEX 8747, for minimal noise injection. Bypass capacitors must not be connected to these balls. <i>Note: A 3.01K 0.1% resistor can be used, because that value is within the 3.00K \pm1% specification.</i>		
REXT_CMU	W10	A	No	–
		Clock Management Unit for SerDes An external resistor (3.00KΩ, 1%) must be attached between REXT_CMU and VSS (Ground). <i>Note: A 3.01K 0.1% resistor can be used, because that value is within the 3.00K \pm1% specification.</i>		

3.5.8 No Connect Signals – 19 x 21 mm² Package

Caution: *Do not connect these balls to board electrical paths.
These balls are internally connected to the device.*

Table 3-22. No Connect Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
N/C	B9, B15, B21, F13, F16, F17, F20, F21, F23, H14, N22, P6, P7, P17, P18, T19, V8, W8, W13, Y16, Y17, Y19, Y20, Y22, AA18, AA21, AD18, AD21	<i>Reserved</i>	No	–
		No Connect (28 Balls) Do not connect these balls to board electrical paths.		
SPARE3	K2	I/O, PD	No	–
		Spare 3 <i>Reserved for future use</i> Note: Normally, this I/O should be pulled Low to <i>VSS</i> (Ground). Optionally, this I/O can remain unconnected, because the internal pull-down resistor holds the input Low.		
SPARE2	U6	I/O, PU	No	–
		Compatibility Enable for Non-Compliant Gen 1 Endpoints When SPARE2 is Low and the Link training sequence fails during either the LTSSM <i>Polling</i> or <i>Configuration</i> state, the next time the LTSSM exits the <i>Detect</i> state, TS Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support. When SPARE2 is High, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 3 data rate and Autonomous Change. Note: This feature should be enabled only if a non-compliant Gen 1 device will not linkup if these Data Rate Identifier bits are Set. Normally, this I/O should be pulled High to <i>VDD18</i> . Although this is an I/O signal, its logical operation is input. Optionally, this I/O can remain unconnected, because the internal pull-up resistor holds the input High.		
SPARE1	Y2	I/O, PU	No	–
		Spare 1 <i>Reserved for future use</i> Note: Normally, this I/O should be pulled High to <i>VDD18</i> . Optionally, this I/O can remain unconnected, because the internal pull-up resistor holds the input High.		

Table 3-22. No Connect Signals – 19 x 21 mm² Package (Cont.)

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
SPARE0	F1	I/O, PU	No	–
		Spare 0 <i>Reserved for future use</i> <i>Note: Normally, this I/O should be pulled High to VDD18. Optionally, this I/O can remain unconnected, because the internal pull-up resistor holds the input High.</i>		

3.5.9 Power and Ground Signals – 19 x 21 mm² Package

In general, each power ball should connect to one de-coupling capacitor. Use a mix of values, *such as* 0.1 and 0.01 μ F.

Due to VDD09 in-rush current at the moment [PEX_PERST#](#) input is de-asserted, bulk capacitance is needed, to prevent the voltage rail from falling below minimum voltage requirements. *For example*, the PEX 8747 RDK uses three 680 μ F capacitors for this. This particular capacitance value is not required; however, it is best to use multiple capacitors in parallel. Inductance must be low.

Table 3-23. Power and Ground Signals – 19 x 21 mm² Package

Signal Name	Location	Type	Multiplexed Y/N	STRAP_TESTMODE0 Input State
		Description		
VDD09	K8, K10, K12, K14, K16, L9, L11, L13, L15, M8, M10, M12, M14, M16, N9, N11, N13, N15, P8, P10, P12, P14, P16, R9, R11, R13, R15, T8, T10, T12, T14, T16	CPWR	No	–
		0.9V -5%, +5.55% Power for Core and SerDes Digital Logic (32 Balls)		
VDD09A	H6, H7, H8, H9, H12, H15, H16, H17, J7, J8, J9, J11, J13, J15, J16, J18, K6, K17, K18, L18, M7, M17, N7, N17, R6, R7, T6, T18, U8, U9, U11, U14, U15, U16, U17, U18, V12, V15, V16	APWR	No	–
		0.9V -5%, +5.55% Power for SerDes Analog Circuits (39 Balls)		
VDD18	J12, J17, K7, N6, N18, T7, T17, U12	I/OPWR	No	–
		1.8V -5%, +10% Power for I/O Logic Functions (8 Balls)		
VDD18A	J10, J14, L7, L17, R17, U7, U10, U13	PLL PWR	No	–
		1.8V -5%, +10% Power for PLL Circuits (8 Balls)		
VSS	A3, A6, A9, A12, A15, A18, A21, C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, D3, D6, D9, D12, D15, D18, D21, E3, E6, E9, E12, E15, E18, E21, F6, F9, F12, F15, F18, G1, G2, G3, G4, G5, G6, G9, G12, G15, G18, G19, G20, G21, G22, G23, H3, H21, J3, J21, K1, K4, K5, K9, K11, K13, K15, K20, K21, K23, L3, L8, L10, L12, L14, L16, L21, M3, M9, M11, M13, M15, M21, N1, N4, N5, N8, N10, N12, N14, N16, N20, N21, N23, P3, P9, P11, P13, P15, P21, R3, R8, R10, R12, R14, R16, R21, T1, T4, T5, T9, T11, T13, T15, T20, T23, U3, U21, V3, V6, V9, V21, W1, W4, W9, W12, W17, W18, W19, W20, W21, W22, W23, Y1, Y7, Y8, Y9, Y12, Y15, Y18, Y21, Y23, AA3, AA6, AA9, AA12, AA15, AB3, AB6, AB9, AB12, AB15, AB18, AB21, AC1, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD15, AE3, AE6, AE9, AE12, AE15, AE18, AE21	GND	No	–
		Ground Connections (193 Balls)		

3.6 Physical Layout

Figure 3-3. Physical Ball Assignment (See-Through Top View) – 27 x 27 mm² Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		
A	VSS	STRAP_R ESERVED 11	REXT_A6	VSS	PEX_PETn 24	PEX_PETn 25	PEX_PETn 26	PEX_PETn 27	N/C	PEX_PETn 28	PEX_PETn 29	PEX_PETn 30	PEX_PETn 31	PEX_PETn 47	PEX_PETn 46	PEX_PETn 45	PEX_PETn 44	N/C	PEX_PETn 43	PEX_PETn 42	PEX_PETn 41	PEX_PETn 40	VSS	N/C	VSS	VSS	A	
B	JTAG_TMS	JTAG_TCK	STRAP_R ESERVED 19#	VSS	PEX_PETp 24	PEX_PETp 25	PEX_PETp 26	PEX_PETp 27	N/C	PEX_PETp 28	PEX_PETp 29	PEX_PETp 30	PEX_PETp 31	PEX_PETp 47	PEX_PETp 46	PEX_PETp 45	PEX_PETp 44	N/C	PEX_PETp 43	PEX_PETp 42	PEX_PETp 41	PEX_PETp 40	VSS	N/C	N/C	N/C	B	
C	REXT_B6	JTAG_TRST#	JTAG_TDI	STRAP_ST N1_PORT CFG0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	STRAP_ST N2_PORT CFG0	FATAL_ER#	N/C	STRAP_R ESERVED 9	C	
D	PEX_INTA#	SPARE0	PORT_GO OD0#	VSS	PEX_PERn 24	PEX_PERn 25	PEX_PERn 26	PEX_PERn 27	REXT_A7	PEX_PERn 28	PEX_PERn 29	PEX_PERn 30	PEX_PERn 31	PEX_PERn 47	PEX_PERn 46	PEX_PERn 45	PEX_PERn 44	REXT_A11	PEX_PERn 43	PEX_PERn 42	PEX_PERn 41	PEX_PERn 40	VSS	N/C	N/C	N/C	D	
E	N/C	I2C_ADDR0	I2C_SDA0	VSS	PEX_PERp 24	PEX_PERp 25	PEX_PERp 26	PEX_PERp 27	REXT_B7	PEX_PERp 28	PEX_PERp 29	PEX_PERp 30	PEX_PERp 31	PEX_PERp 47	PEX_PERp 46	PEX_PERp 45	PEX_PERp 44	REXT_B11	PEX_PERp 43	PEX_PERp 42	PEX_PERp 41	PEX_PERp 40	VSS	REXT_A10	EE_SK	EE_CS#	E	
F	N/C	STRAP_I2C SMBUS _EN	STRAP_R ESERVED 4	VSS	VSS	VSS	VSS	VSS	N/C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	REXT_B10	VSS	VSS	VSS	VSS	VSS	N/C	N/C	EE_DO	F	
G	STRAP_R ESERVED 7	STRAP_R ESERVED 18	REXT_B5	I2C_SCL0	JTAG_TDO	STRAP_R ESERVED 12	VDD18	VSS	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VSS	VDD18	N/C	N/C	EE_DI	STRAP_U PSTRM_P ORTSEL1	STRAP_U PSTRM_P ORTSEL0	STRAP_U PSTRM_P ORTSEL2	G	
H	VSS	VSS	REXT_A5	VSS	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD18	VSS	VSS	VSS	VSS	STRAP_G EN1_GEN 2	VSS	VSS	H	
J	PEX_PETn 23	PEX_PETp 23	VSS	PEX_PERn 23	PEX_PERp 23	VSS	VDD09A	VSS	VDD18	VSS	VDD09A	VSS	VDD09A	VDD09A	VSS	VDD09A	VSS	VDD18	VSS	VDD09A	VSS	PEX_PERp 39	PEX_PERn 39	VSS	PEX_PETp 39	PEX_PETn 39	J	
K	PEX_PETn 22	PEX_PETp 22	VSS	PEX_PERn 22	PEX_PERp 22	VSS	VDD09A	VSS	VSS	VDD18	VSS	VDD18A	VSS	VSS	VDD18A	VSS	VDD18	VSS	VSS	VDD09A	VSS	PEX_PERp 38	PEX_PERn 38	VSS	PEX_PETp 38	PEX_PETn 38	K	
L	PEX_PETn 21	PEX_PETp 21	VSS	PEX_PERn 21	PEX_PERp 21	VSS	VDD09A	VSS	VDD09A	VSS	VDD09	VSS	VDD09	VSS	VDD09	VSS	VDD09A	VSS	VDD09A	VSS	PEX_PERp 37	PEX_PERn 37	VSS	PEX_PETp 37	PEX_PETn 37	L		
M	PEX_PETn 20	PEX_PETp 20	VSS	PEX_PERn 20	PEX_PERp 20	VSS	VDD09A	VSS	VDD09A	VSS	VSS	VDD09	VSS	VDD09	VSS	VDD09	VSS	VDD09A	VSS	VDD09A	VSS	PEX_PERp 36	PEX_PERn 36	VSS	PEX_PETp 36	PEX_PETn 36	M	
N	N/C	N/C	VSS	REXT_A4	REXT_B4	STRAP_R ESERVED 1	VDD09A	VSS	VSS	VDD18A	VDD09	VSS	VDD09	VSS	VDD09	VSS	VDD18A	VSS	VSS	VDD09A	VSS	STRAP_R ESERVED 2	REXT_B9	REXT_A9	VSS	N/C	N/C	N
P	PEX_PETn 19	PEX_PETp 19	VSS	PEX_PERn 19	PEX_PERp 19	VSS	VDD09A	VSS	VDD09A	VSS	VSS	VDD09	VSS	VDD09	VSS	VDD09	VSS	VDD09A	VSS	VDD09A	VSS	PEX_PERp 35	PEX_PERn 35	VSS	PEX_PETp 35	PEX_PETn 35	P	
R	PEX_PETn 18	PEX_PETp 18	VSS	PEX_PERn 18	PEX_PERp 18	VSS	VDD09A	VSS	VSS	VDD09A	VDD09	VSS	VDD09	VSS	VDD09	VSS	VDD09A	VSS	VSS	VDD09A	VSS	PEX_PERp 34	PEX_PERn 34	VSS	PEX_PETp 34	PEX_PETn 34	R	
T	PEX_PETn 17	PEX_PETp 17	VSS	PEX_PERn 17	PEX_PERp 17	VSS	VDD09A	VSS	VDD09A	VSS	VSS	VDD09	VSS	VDD09	VSS	VDD09	VSS	VDD09A	VSS	VDD09A	VSS	PEX_PERp 33	PEX_PERn 33	VSS	PEX_PETp 33	PEX_PETn 33	T	
U	PEX_PETn 16	PEX_PETp 16	VSS	PEX_PERn 16	PEX_PERp 16	VSS	VDD09A	VSS	VSS	VDD18	VSS	VDD18A	VSS	VSS	VDD18A	VSS	VDD18	VSS	VSS	VDD09A	VSS	PEX_PERp 32	PEX_PERn 32	VSS	PEX_PETp 32	PEX_PETn 32	U	
V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD18	VDD18	VSS	VDD09A	VSS	VDD09A	VDD09A	VSS	VDD09A	VSS	VDD18	VDD18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	V	
W	N/C	N/C	STRAP_R ESERVED 3	N/C	GPIO6	STRAP_I2C SMBUS CFG_EN#	VDD18	VDD18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD18	VDD18	N/C	N/C	REXT_B8	N/C	N/C	STRAP_S ERDES_M ODE_EN#	W	
Y	REXT_CMU	N/C	GPIO7	REXT_A0	REXT_B0	STRAP_I2C SMBUS STMODE0	VDD18	VSS	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VDD09A	VSS	VDD18	STRAP_P ROBE_MO DE#	REXT_B3	N/C	N/C	REXT_A8	STRAP_PL L_BYPASS#	Y	
AA	SPARE3	SPARE2	SPARE1	VSS	VSS	VSS	VSS	VSS	N/C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	STRAP_R ESERVED 10	VSS	VSS	VSS	VSS	VSS	N/C	N/C	N/C	AA	
AB	GPIO1	PORT_GO OD4#	GPIO2	VSS	PEX_PERp 0	PEX_PERp 1	PEX_PERp 2	PEX_PERp 3	REXT_B1	PEX_PERp 4	PEX_PERp 5	PEX_PERp 6	PEX_PERp 7	PEX_PERp 8	PEX_PERp 9	PEX_PERp 10	PEX_PERp 11	REXT_B2	PEX_PERp 12	PEX_PERp 13	PEX_PERp 14	PEX_PERp 15	VSS	REXT_A3	N/C	N/C	AB	
AC	PEX_PER ST#	PORT_GO OD8#	PORT_GO OD9#	VSS	PEX_PERn 0	PEX_PERn 1	PEX_PERn 2	PEX_PERn 3	REXT_A1	PEX_PERn 4	PEX_PERn 5	PEX_PERn 6	PEX_PERn 7	PEX_PERn 8	PEX_PERn 9	PEX_PERn 10	PEX_PERn 11	REXT_A2	PEX_PERn 12	PEX_PERn 13	PEX_PERn 14	PEX_PERn 15	VSS	THERMAL _DIODE#	STRAP_R ESERVED 14	N/C	AC	
AD	PORT_GO OD5#	GPIO10	STRAP_R ESERVED 20	STRAP_R ESERVED 21	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	N/C	STRAP_R ESERVED 0	N/C	AD	
AE	GPIO3	N/C	N/C	VSS	PEX_PETp 0	PEX_PETp 1	PEX_PETp 2	PEX_PETp 3	PEX_REF CLKp	PEX_PETp 4	PEX_PETp 5	PEX_PETp 6	PEX_PETp 7	PEX_PETp 8	PEX_PETp 9	PEX_PETp 10	PEX_PETp 11	N/C	PEX_PETp 12	PEX_PETp 13	PEX_PETp 14	PEX_PETp 15	VSS	STRAP_R ESERVED 16	STRAP_R ESERVED 15	N/C	AE	
AF	VSS	N/C	N/C	VSS	PEX_PETn 0	PEX_PETn 1	PEX_PETn 2	PEX_PETn 3	PEX_REF CLKn	PEX_PETn 4	PEX_PETn 5	PEX_PETn 6	PEX_PETn 7	PEX_PETn 8	PEX_PETn 9	PEX_PETn 10	PEX_PETn 11	N/C	PEX_PETn 12	PEX_PETn 13	PEX_PETn 14	PEX_PETn 15	VSS	STRAP_R ESERVED 5	THERMAL _DIODEp	VSS	AF	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26		

Figure 3-4. Physical Ball Assignment (See-Through Top View) – 19 x 21 mm² Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	PEX_PET42	PEX_PET43	VSS	PEX_PET406	PEX_PET427	VSS	PEX_PET428	PEX_PET429	VSS	PEX_PET430	PEX_PET431	VSS	PEX_PET432	PEX_PET433	VSS	PEX_PET434	PEX_PET435	VSS	PEX_PET436	PEX_PET437	VSS	PEX_PET438	PEX_PET439
B	PEX_PET44	PEX_PET45	PORT_GOOD#	PEX_PET407	PEX_PET428	PEX_PET429	PEX_PET430	PEX_PET431	PEX_PET432	PEX_PET433	PEX_PET434	PEX_PET435	PEX_PET436	PEX_PET437	PEX_PET438	PEX_PET439	PEX_PET440	PEX_PET441	PEX_PET442	PEX_PET443	PEX_PET444	PEX_PET445	PEX_PET446
C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
D	PEX_PET46	PEX_PET47	VSS	PEX_PET408	PEX_PET429	VSS	PEX_PET430	PEX_PET431	PEX_PET432	PEX_PET433	PEX_PET434	PEX_PET435	PEX_PET436	PEX_PET437	PEX_PET438	PEX_PET439	PEX_PET440	PEX_PET441	PEX_PET442	PEX_PET443	PEX_PET444	PEX_PET445	PEX_PET446
E	PEX_PET48	PEX_PET49	VSS	PEX_PET410	PEX_PET431	VSS	PEX_PET432	PEX_PET433	PEX_PET434	PEX_PET435	PEX_PET436	PEX_PET437	PEX_PET438	PEX_PET439	PEX_PET440	PEX_PET441	PEX_PET442	PEX_PET443	PEX_PET444	PEX_PET445	PEX_PET446	PEX_PET447	PEX_PET448
F	SPARE0	DC_SD40	JTAG_TRST#	STRAP_RESE#	DC_ADD0	VSS	DC_SD0	REXT_A6	VSS	REXT_A7	JTAG_TDO	VSS	NC	FATALERR#	VSS	NC	REXT_B9	VSS	EE_DI	NC	NC	EE_SK	NC
G	VSS	VSS	VSS	VSS	VSS	VSS	REXT_A5	REXT_A6	VSS	REXT_A7	JTAG_TCK	VSS	REXT_A11	REXT_A10	VSS	REXT_B10	REXT_B9	VSS	VSS	VSS	VSS	VSS	VSS
H	PEX_PET43	PEX_PET44	VSS	PEX_PET423	PEX_PET424	VSS	PEX_PET425	PEX_PET426	VSS	PEX_PET427	JTAG_TMS	PEX_PET428	PEX_PET429	PEX_PET430	PEX_PET431	PEX_PET432	PEX_PET433	PEX_PET434	PEX_PET435	PEX_PET436	PEX_PET437	PEX_PET438	PEX_PET439
J	PEX_PET42	PEX_PET43	VSS	PEX_PET422	PEX_PET423	VSS	PEX_PET424	PEX_PET425	VSS	PEX_PET426	JTAG_TDI	PEX_PET427	PEX_PET428	PEX_PET429	PEX_PET430	PEX_PET431	PEX_PET432	PEX_PET433	PEX_PET434	PEX_PET435	PEX_PET436	PEX_PET437	PEX_PET438
K	VSS	SPARE3	STRAP_RESE#	STRAP_RESE#	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
L	PEX_PET41	PEX_PET42	VSS	PEX_PET421	PEX_PET422	VSS	PEX_PET423	PEX_PET424	VSS	PEX_PET425	PEX_PET426	VSS	PEX_PET427	PEX_PET428	VSS	PEX_PET429	PEX_PET430	VSS	PEX_PET431	PEX_PET432	PEX_PET433	PEX_PET434	PEX_PET435
M	PEX_PET40	PEX_PET41	VSS	PEX_PET420	PEX_PET421	VSS	PEX_PET422	PEX_PET423	VSS	PEX_PET424	PEX_PET425	VSS	PEX_PET426	PEX_PET427	VSS	PEX_PET428	PEX_PET429	VSS	PEX_PET430	PEX_PET431	PEX_PET432	PEX_PET433	PEX_PET434
N	VSS	REXT_A4	GPO1	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
P	PEX_PET19	PEX_PET18	VSS	PEX_PET16	PEX_PET15	VSS	PEX_PET14	PEX_PET13	VSS	PEX_PET12	PEX_PET11	VSS	PEX_PET10	PEX_PET09	VSS	PEX_PET08	PEX_PET07	VSS	PEX_PET06	PEX_PET05	PEX_PET04	PEX_PET03	PEX_PET02
R	PEX_PET14	PEX_PET15	VSS	PEX_PET18	PEX_PET17	VSS	PEX_PET16	PEX_PET15	VSS	PEX_PET14	PEX_PET13	VSS	PEX_PET12	PEX_PET11	VSS	PEX_PET10	PEX_PET09	VSS	PEX_PET08	PEX_PET07	PEX_PET06	PEX_PET05	PEX_PET04
T	VSS	PORT_GOOD#	PORT_GOOD#	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
U	PEX_PET17	PEX_PET18	VSS	PEX_PET16	PEX_PET15	VSS	PEX_PET14	PEX_PET13	VSS	PEX_PET12	PEX_PET11	VSS	PEX_PET10	PEX_PET09	VSS	PEX_PET08	PEX_PET07	VSS	PEX_PET06	PEX_PET05	PEX_PET04	PEX_PET03	PEX_PET02
V	PEX_PET16	PEX_PET17	VSS	PEX_PET18	PEX_PET19	VSS	PEX_PET20	PEX_PET21	VSS	PEX_PET22	PEX_PET23	VSS	PEX_PET24	PEX_PET25	VSS	PEX_PET26	PEX_PET27	VSS	PEX_PET28	PEX_PET29	PEX_PET30	PEX_PET31	PEX_PET32
W	VSS	PEX_PET19	PEX_PET20	VSS	PEX_PET21	VSS	PEX_PET22	PEX_PET23	VSS	PEX_PET24	PEX_PET25	VSS	PEX_PET26	PEX_PET27	VSS	PEX_PET28	PEX_PET29	VSS	PEX_PET30	PEX_PET31	PEX_PET32	PEX_PET33	PEX_PET34
Y	VSS	SPARE1	STRAP_RESE#	STRAP_RESE#	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AA	PEX_PET20	PEX_PET21	VSS	PEX_PET22	PEX_PET23	VSS	PEX_PET24	PEX_PET25	VSS	PEX_PET26	PEX_PET27	VSS	PEX_PET28	PEX_PET29	VSS	PEX_PET30	PEX_PET31	VSS	PEX_PET32	PEX_PET33	PEX_PET34	PEX_PET35	PEX_PET36
AB	PEX_PET20	PEX_PET21	VSS	PEX_PET22	PEX_PET23	VSS	PEX_PET24	PEX_PET25	VSS	PEX_PET26	PEX_PET27	VSS	PEX_PET28	PEX_PET29	VSS	PEX_PET30	PEX_PET31	VSS	PEX_PET32	PEX_PET33	PEX_PET34	PEX_PET35	PEX_PET36
AC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AD	PEX_PET20	PEX_PET21	VSS	PEX_PET22	PEX_PET23	VSS	PEX_PET24	PEX_PET25	VSS	PEX_PET26	PEX_PET27	VSS	PEX_PET28	PEX_PET29	VSS	PEX_PET30	PEX_PET31	VSS	PEX_PET32	PEX_PET33	PEX_PET34	PEX_PET35	PEX_PET36
AE	PEX_PET20	PEX_PET21	VSS	PEX_PET22	PEX_PET23	VSS	PEX_PET24	PEX_PET25	VSS	PEX_PET26	PEX_PET27	VSS	PEX_PET28	PEX_PET29	VSS	PEX_PET30	PEX_PET31	VSS	PEX_PET32	PEX_PET33	PEX_PET34	PEX_PET35	PEX_PET36

Note: Figure 3-4 is rotated 90° counterclockwise, for ease of viewing.

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Chapter 4 Functional Overview

4.1 Introduction

The PEX 8747 is designed with a flexible, modular architecture. This chapter provides an overview of the PEX 8747's major functions:

- [Mode of Operation](#)
- [Software Architecture](#)
- [Hardware Architecture](#)
- [PCI Express Station Functional Description](#)
- [Physical Layer](#)
- [Transaction Layer](#)

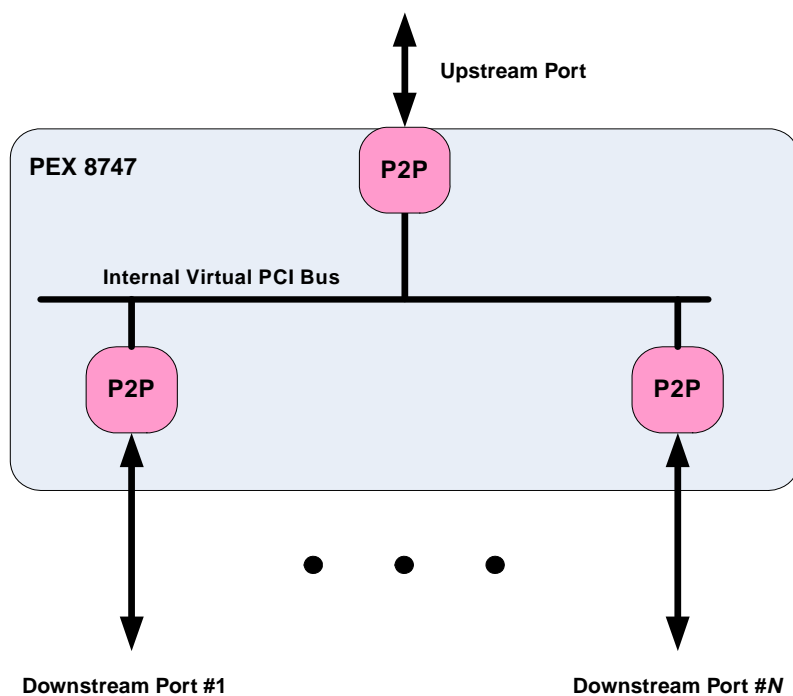
Subsequent chapters go into further detail.

4.2 Mode of Operation

The PEX 8747 is a 48-Lane, 5-Port switch. [Figure 4-1](#) illustrates the PEX 8747, from a software point of view. The PEX 8747 supports one Upstream Port and up to four Downstream Ports.

Note: The PCI-to-PCI (P2P) blocks in [Figure 4-1](#) are a logical representation of how a Port presents itself to software. Each P2P block is a Type 1 PCI function, which is a PCI-to-PCI bridge.

Figure 4-1. Software Point-of-View



4.3 Software Architecture

4.3.1 PCI-Compatible Software Model

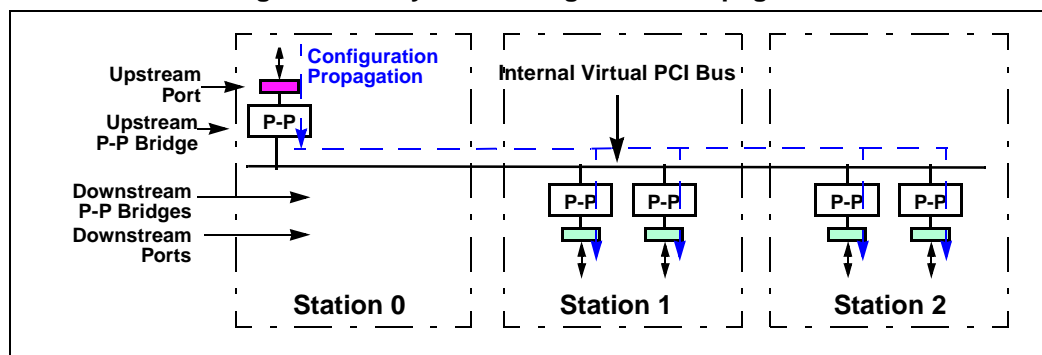
The PEX 8747 can be thought of as a hierarchy of PCI-to-PCI bridges, with one Upstream PCI-to-PCI bridge and one or more Downstream PCI-to-PCI bridges connected by an internal Virtual PCI Bus. (Refer to [Figure 4-2](#).) PCI-to-PCI bridges are compliant with the PCI and PCI Express system models, allowing software written for Conventional PCI devices to work on the latest PCI Express switches.

The Upstream Port has the lowest Bus Number in a PCI Express switch. From the point of view of the PCI-to-PCI bridge, there is a:

- Primary Bus Number (the Upstream Bus Number),
- Secondary Bus Number (the Downstream Bus Number), and
- Subordinate Bus Number (highest Bus Number below the bridge).

The Secondary and Subordinate Bus Numbers form a range, within which all Downstream devices must fit. This can cause problems for systems that might allow hot-insertion of additional devices, unless planned for in advance, and a gap is created within in the Bus Number range, to allow for new device(s). Typically, system BIOS scans the PCI Bus and assigns Bus Numbers; therefore, support for hot insertion can depend upon the BIOS used.

Figure 4-2. System Configuration Propagation



Note: [Table 4-1](#) indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.

The Configuration Space registers (CSRs) in the Upstream PCI-to-PCI bridge are accessible by Type 0 Configuration Requests that target the Upstream bus interface. The Upstream Port captures the Type 0 Configuration Write Target Bus Number and Device Number. The Upstream Port then uses this Captured Bus Number and Captured Device Number, as part of the Requester ID and Completer ID for the Requests and Completions generated by the Upstream Port.

The CSRs in the Downstream Port PCI-to-PCI bridges are accessible by Type 1 Configuration Requests received at the Upstream Port that target the internal virtual PCI Bus, by having a Bus Number value that matches the Upstream bridge's Secondary Bus Number value. Each Downstream bridge is associated with a unique Device Number, as explained in [Section 4.4.1.2](#).

The CSRs of Downstream devices are hit in two ways. If the Configuration Request matches the PEX 8747 Downstream Port Secondary Bus Number, the PEX 8747 converts the Type 1 Configuration Request into a Type 0 Configuration Request. However, if the Bus Number does *not* match the Secondary Bus Number, but falls within the Subordinate Bus Number range, the Type 1 Configuration Request is forwarded out of the PEX 8747, unchanged. A Type 1 Configuration Request that targets a Bus Number that is not within range is invalid, and is terminated by the PEX 8747 Upstream Port as an Unsupported Request (UR).

After all PCI devices have been located and assigned Bus and Device Numbers, software can assign a Memory map and I/O map. In the PEX 8747, each Downstream bridge has its own Base and Limit. Software will Set the Upstream PCI-to-PCI bridge Base and Limit to include all Downstream Base and Limit ranges. As a result, all Downstream devices are contiguous in the Memory map. Requests (Memory or I/O) go Downstream if they fall within a bridge's Base and Limit range. Alternatively, Requests (Memory or I/O) go Upstream if they do not target anything within the Upstream bridge's Base and Limit range.

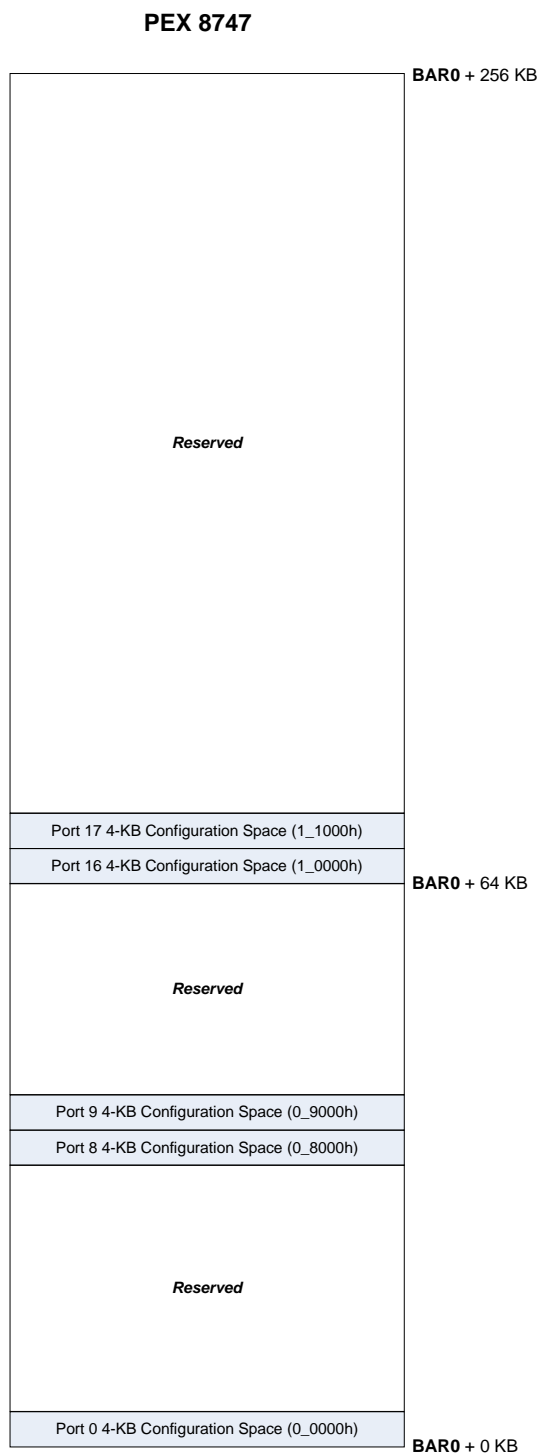
Completions are routed by the Bus Number established in the Configuration registers. If the Bus Number is in the Secondary or Subordinate range, the packet goes Downstream; otherwise, the packet goes Upstream.

PLX has enhanced the basic PCI-to-PCI bridge with PCI Express-defined capabilities, Device-Specific capabilities, and additional functions.

4.3.2 PCI Express Memory-Mapped Configuration Space

The Configuration space is also mapped into Memory space that is seen by **Base Address Register 0 (BAR0)** of the PCI-to-PCI bridges, which is termed *Memory-Mapped Configuration space*. All PEX 8747 Ports, fit into a single, flattened Memory space, as illustrated in [Figure 4-3](#).

Each Port Configuration space occupies 4 KB of the CSR Memory map. Port 0 is located at offset 0 KB, Port 8 is located at offset 32 KB, and so forth, for all enabled Ports, up to 256 KB. 4-KB register blocks that correspond to non-enabled Ports are *Reserved*.

Figure 4-3. PCI Express Memory-Mapped Configuration Space

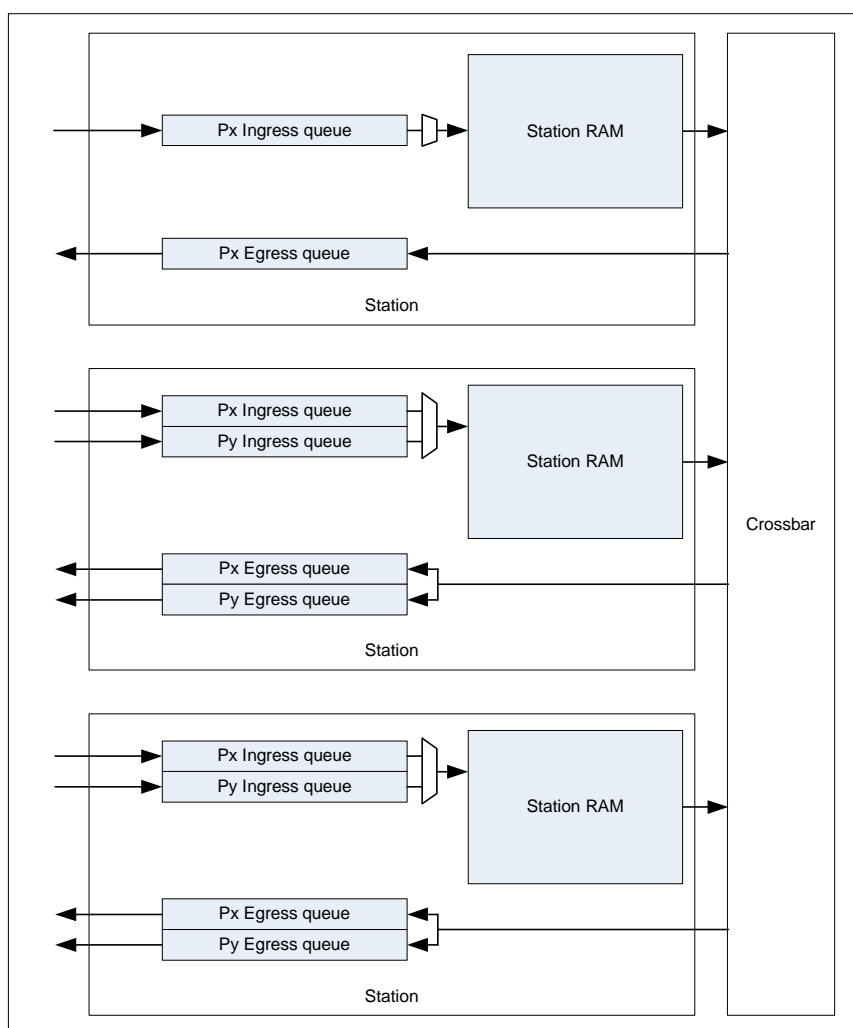
Note: *Table 4-1 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.*

4.4 Hardware Architecture

The PEX 8747 has 48 PCI Express Lanes, implemented as 16 Lanes across three Stations (refer to [Section 4.4.1.1](#)). The Stations are connected to one another by the internal non-blocking fabric. [Figure 4-4](#) illustrates a block diagram of the PEX 8747.

Station 0 has only one Port; however, Station 1 and Station 2 can have one or two Ports associated with it. The quantity of enabled Ports, and Link widths associated with those Ports, are configurable, on a Station-by-Station basis. Each Port has its own Ingress and Egress queue. Ports within a Station share the same Station RAM, but are otherwise completely independent of one another. Each Port implements the *PCI Express Base r3.0* Physical, Data Link, and Transaction Layers (PHY, DLL, and TL, respectively).

Figure 4-4. PEX 8747 Block Diagram



Notes: *Px* represents the first Port Number within the Station. *Py* represents the last enabled Port Number within the Station.

[Table 4-1](#) indicates which Ports are enabled/used, and when, based upon the *STRAP_STNx_PORTCFG0* input states and/or serial EEPROM programming.

4.4.1 Station and Port Functions

4.4.1.1 Port Configurations

[Table 4-1](#) defines the PEX 8747 Port configurations, as well as the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes. The Lanes are assigned to each enabled Port, in sequence.

The Upstream and Downstream Ports' maximum Link widths are initially defined by the STRAP_STNx_PORTCFG0 3-state inputs, which can be pulled or tied High (1) to **VDD18**, Low (0) to **VSS** (Ground), or left floating (Z, not connected). The serial EEPROM option can be used to re-configure the Ports, with the options defined in [Table 4-1](#). Serial EEPROM configuration occurs following a Fundamental Reset, and overrides the configuration defined by the STRAP_STNx_PORTCFG0 3-state inputs at that time. Port configuration can also be changed through the I²C Slave interface, if programmed prior to the I²C/SMBus Write sequence that Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset **3ACh[0]**) when **STRAP_I2C_SMBUS_CFG_EN#** is strapped Low. The final Link width can be automatically negotiated down from the programmed width, through Link-width negotiation for linkup to a device with fewer Lanes. The narrowest Port on one end of the Link determines the maximum Link width. Additionally, if a connection is broken on one of the Lanes, the training sequence removes the broken Lane and negotiates to a narrower Link width. *For example*, a x16 Port can negotiate down to x8, x4, x2, or x1.

If the Port cannot train to x1 (Lane 0 is broken), the Port reverses its Lanes and attempts to retrain. *For example*, a x16 Port that cannot train to x16 attempts to negotiate down to x8, x4, x2, or x1; if x1 linkup fails, the Port reverses its Lanes and re-attempts linkup negotiation. Either the lowest Lane (Lane 0) or highest Lane (if Lanes are reversed) of the programmed Link width must connect to the other device's Lane 0.

Each Port can run independently at Gen 1, Gen 2, or Gen 3 (2.5, 5.0, or 8.0 GT/s, respectively) Link speed.

Each Station's Port configurations are independent of the other Stations' Port configurations. Ports that are not configured or enabled are invisible to software.

Table 4-1. Port Configurations

# ^a	Fixed x16 Link Width	Port Configuration Register Value Port 0, Offset 300h[2:0]	Station 0 [Lanes/SerDes]/Port	
			Port 0 ^b	—
1	Station 0, Port 0 is always x16	001b	x16 [0-15]	
# ^a	Port Configuration Strapping Input States STRAP_STN1_PORTCFG0 ^c	Port Configuration Register Value Port 0, Offset 300h[5:3]	Station 1 [Lanes/SerDes]/Port	
			Port 8 ^b	Port 9
1	Z	001b	x16 [16-31]	
2	1	010b	x8 [16-23]	x8 [24-31]
# ^a	Port Configuration Strapping Input States STRAP_STN2_PORTCFG0 ^c	Port Configuration Register Value Port 0, Offset 300h[8:6]	Station 2 [Lanes/SerDes]/Port	
			Port 16 ^b	Port 17
1	Z	001b	x16 [32-47]	
2	1	010b	x8 [32-39]	x8 [40-47]

- a. Port Configuration Number, which is the decimal equivalent of the **Port Configuration** register Port Configuration for Station x field(s)' (Port 0, offset 300h[8:6, 5:3, and/or 2:0]) binary value.
- b. Ports 0, 8, and 16 are also “Station Ports” within their respective Stations. Station Ports are used to control the Station-specific registers.
- c. “Z” means “floating.” Z is used for the 3-state inputs that have three functions, depending upon whether the input is pulled or tied High to **VDD18**, pulled or tied Low to **VSS** (Ground), or left floating (not connected). Each one of these three input states (1, 0, or Z, respectively) results in a different function for that input.

4.4.1.2 Port Numbering

Available Port Numbers that can be used by the PEX 8747 are as follows (refer to [Table 4-1](#) and [Figure 4-5](#)):

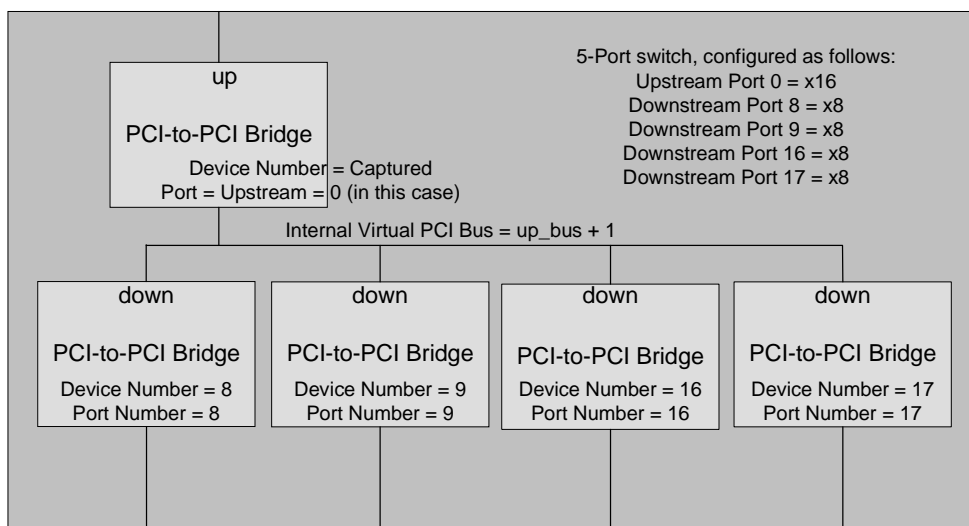
- **Station 0** – Port 0
- **Station 1** – Ports 8 and 9
- **Station 2** – Ports 16 and 17

All Downstream Device Numbers match their corresponding Port Number. *For example*, if Port 9 is a Downstream Port, the PCI-to-PCI bridge associated with that Port is Device Number 9.

Any Port can be configured as, or dynamically changed to be, the Upstream Port. The PCI-to-PCI bridge implemented on the Upstream Port does not assume a Device Number – it accepts the Device Number assigned by the Upstream device. Generally, the Upstream device assigns Device Number 0, according to the *PCI Express Base r3.0*.

[Figure 4-5](#) illustrates a sample configuration, with the PEX 8747 configured as a 5-Port switch with Upstream x16 on Port 0, and Downstream Ports as follows – Ports 8, 9, 16, and 17 (x8). The Device Numbers for the PCI-to-PCI bridges implemented on the Downstream Ports match the Port Numbers.

Figure 4-5. Sample Port and Device Numbering for a 5-Port Configuration



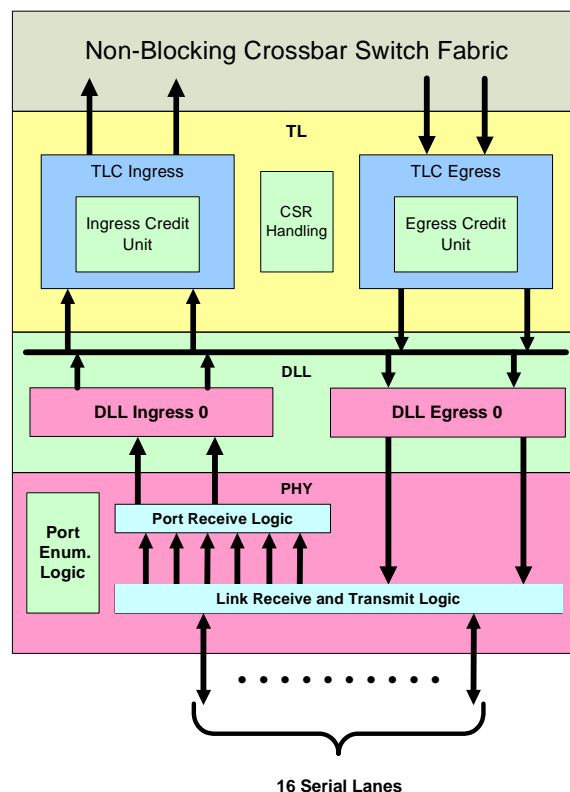
4.5 PCI Express Station Functional Description

The PEX 8747 groups 16 SerDes together into a Station, as listed in [Table 4-1](#). Station 0 has one Port, and Stations 1 and 2 can have one to two Ports each, depending upon the Station's Port configuration, with each Port having its own SerDes assignments.

Each Station implements the PCI Express PHY and DLL functions for each of its Ports, and aggregates traffic from these Ports onto a transaction-based, non-blocking internal crossbar fabric. The PCI Express Station also performs many TL functions, while the packet queuing and ordering aspects of this layer are handled by the Crossbar Switch Control blocks. During system initialization, software initiates Configuration Requests that set up the PCI Express interfaces, Device Numbers, and Address maps across the various Ports. These maps are used to direct traffic between Ports during standard system operation. Traffic flow between Ports within the same Station, or Ports on different Stations, is supported through the internal crossbar fabric.

At the top level, each Station has a layered organization consisting of the PHY, DLL, and TL blocks, as illustrated in [Figure 4-6](#). The PHY and DLL blocks have Port-specific data paths (one per PCI Express Port) that operate independently of one another. The Transaction Layer Control (TLC) ingress section of the TL block aggregates traffic for all ingress Ports within the Station, then sends the traffic to the internal crossbar fabric. The TLC egress section of the TL block accepts packets, by way of the internal crossbar fabric, from all ingress Ports, and schedules them to be sent out the appropriate egress Port.

Figure 4-6. PCI Express Station Block Diagram (Station 0)



4.6 Physical Layer

The Physical Layer (PHY) converts information received from the DLL into an appropriate serialized format and transmits it across the PCI Express Link. The PHY also receives the serialized input from the Serializer/De-Serializer (SerDes), converts it to parallel data (internal Data Bus), then writes it to the Transaction Layer Control (TLC) Ingress buffer.

The PHY includes all circuitry for PCI Express Link interface operation, including:

- Driver and input buffers
- Parallel-to-serial and serial-to-parallel conversion
- Phase-Locked Loops (PLLs) and clock circuitry
- Impedance matching circuitry
- Interface initialization and maintenance functions
- Programmable pre-emphasis
- Decision Feedback Equalization (DFE)
- Constant Time Linear Equalization (CTLE)

4.6.1 Physical Layer Features

- 48 SerDes, implemented across three Stations, as 16 Lanes, per Station (refer to [Section 4.4.1.1](#))
- One Port in Station 0, and one or two Ports each in Stations 1 and 2
-
- Hardware Link training and initialization
- Hardware detection of polarity inversion
- Hardware detection of Lane reversal
- User-configurable Link widths, per Port (refer to [Table 4-1](#))
- Supported Link widths – x8¹ or x16, depending upon Port configuration; x1, x2, and x4 Link widths are also supported for auto-negotiation
- Supported Link speeds – 2.5, 5.0, and 8.0 GT/s
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Hardware insertion of Sequence Number, STP, SDP, END, and EDB symbols
- Hardware Autonomous Speed Control supported
- Dynamic Link speed control supported
- Dynamic Link width supported
- Data scrambling and 8b/10b (Gen 1 and Gen 2 Link speeds) or 128b/130b (Gen 3 Link speed) encode/decode
- Receiver Error checking (Elastic buffer over/underflow, disparity and symbol encoding, Gen 3 framing)
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Link state Power Management – supported power states are as follows:
 - L0
 - L0s
 - L1
 - L2/L3 Ready (condition before L2 or L3)
 - L3 (no Vaux)
- Upstream Port can operate as Link Negotiation Master (Upstream cross-link)
- Downstream Port(s) can operate as Link Negotiation Slave (Downstream cross-link)
- Checks and removes Data Link Layer Packet (DLLP) framing symbols/tokens
- Checks and removes DLLP Link Cyclic Redundancy Check (LCRC)

1. x8 is valid only for Stations 1 and 2.

4.6.2 Physical Layer Status and Command Registers

The PHY operating conditions are defined in:

- [Section 11.16.4, “Device-Specific Registers – Physical Layer \(Offsets 200h – 25Ch\)”](#)
- [Section 11.18.2, “Device-Specific Registers – Physical Layer \(Offsets B80h – C88h\)”](#)

The Link side Host can track the Link operating status and re-configure Link parameters, by way of these registers.

4.6.3 Hardware Link Interface Configuration

The PHY can include up to 16 integrated SerDes modules, on each Station. The SerDes modules are distributed among four SerDes quads (Quads 0, 1, 2, and 3) and provide the PCI Express hardware interface Lanes. The SerDes modules also provide all physical communication controls and functions required by the *PCI Express Base r3.0*, as well as the Links (clustered into Ports) that connect the PEX 8747 to other PCI Express devices.

The quantity of Ports, quantity of Lanes per Port, and SerDes connected to those Ports, are configurable, as defined in [Table 4-1](#). Initial Port configuration is determined by Strapped inputs, serial EEPROM, or auto Link-width negotiation. After the Ports are configured using the auto-negotiation process, the Link widths can narrow or widen (by combining multiple adjacent Lanes within the Station).

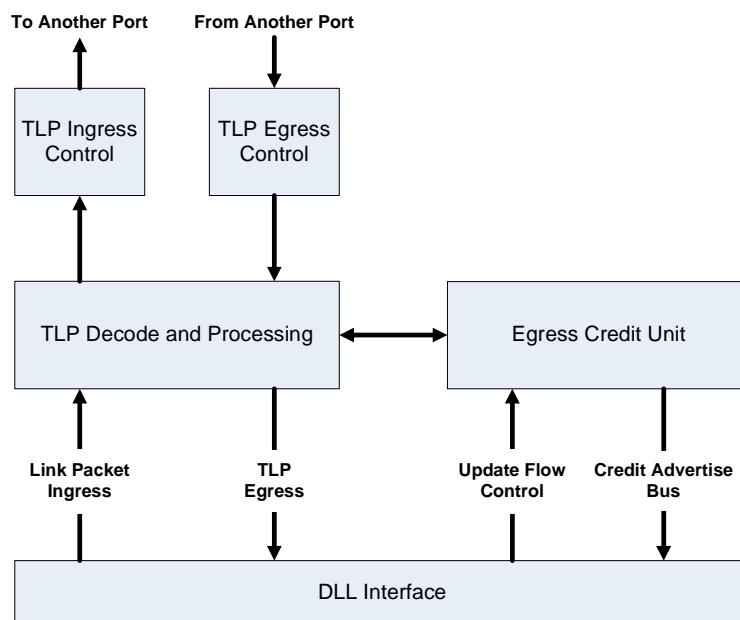
4.7 Transaction Layer

Transaction Layer (TL) functions include:

- Decoding and checking rules for the incoming TLP
- Memory-Mapped CSR access
- Checking incoming packets for malformed or unsupported packets
- Data Poisoning and end-to-end data integrity detection
- End-to-end Cyclic Redundancy Check (ECRC) of incoming packets
- Error logging and reporting for incoming packets
- TLP dispatching
- Write control to the packet RAM and packet Link List RAM
- Destination lookup and TC-VC mapping
- Credit-based scheduling
- Pipelined full Split Transaction protocol
- PCI/PCI-X-compatible ordering
- Interrupt handling (INTx or Message Signaled Interrupts (MSIs))
- Power Management (PM) support
- PCI Express Hot Plug event support
- Link State event support
- QoS support
- Ordering
- Ingress and Egress credit management

The hardware functions provided by the PEX 8747 to implement the *PCI Express Base r3.0* TL requirements are illustrated in [Figure 4-7](#). The blocks provide a combination of ingress and egress control, as well as the data management at each stage within the flow sequence.

Figure 4-7. TL Controller



4.7.1 Locked Transactions

The PEX 8747 forwards Locked transactions that are destined across the switch (that is, the PEX 8747 cannot be a target of a Locked Request; however, it can pass along the Request). Locked transactions that target PEX 8747 Memory space are terminated with an Unsupported Request (UR) error.

While the PEX 8747 understands Locked transactions, it does not lock the resources. This is consistent with limitations for Locked transaction use, as outlined in the *PCI r3.0* (Appendix F, “Exclusive Accesses”), and prevents potential deadlock, as well as serious performance degradation, that could occur with Locked transaction use.

4.7.2 Relaxed Ordering

The PEX 8747 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled, by Setting the **Station-Based Control** register *No Special Treatment for Relaxed Ordering Traffic* bit (Port 0, 8, or 16, offset 760h[29]), in each Station.

4.7.3 TL Transmit/Egress Protocol – End-to-End Cyclic Redundancy Check

End-to-End Cyclic Redundancy Check (ECRC) is an optional 32-bit field appended to the end of the outgoing packet. ECRC is calculated over the entire packet, starting with the Header and including the Data Payload, except for the *EP* bit and bit 0 of the *Type* field, which are always considered to be a value of 1 for ECRC calculations. The *ECRC* field is transmitted, unchanged, as it moves through the fabric to the Completer device. The PEX 8747 checks the ECRC on all incoming TLPs, if enabled (**Advanced Error Capabilities and Control** register *ECRC Check Enable* bit (offset FCCh[8]) is Set, in each Port), and can optionally report detected errors. (When the ECRC is detected, the **Uncorrectable Error Status** register *ECRC Error Status* bit (offset FB8h[19]) can be used to log ECRC errors.)

Additionally, the PEX 8747 can optionally append ECRC to the end of internally generated TLPs, *such as* Interrupt and Error Messages, if enabled (**Advanced Error Capabilities and Control** register *ECRC Generation Enable* bit (offset FCCh[6]) is Set, in each Port).

4.7.4 TL Receive/Ingress Protocol

The ingress side TL collects and stores inbound TLP traffic in the packet RAM. The incoming TLP is checked for LCRC error, valid type field, length matching the Header *Transfer Size* field, and other TLP-specific errors defined by the *PCI Express Base r3.0*.

Header and Data Payload information is forwarded to the Source Scheduler, to be routed across the internal fabric, to the egress Port. When ECRC errors are detected, the packet is discarded.

4.7.5 Flow Control Credit Initialization

The initial quantity of VC0 Flow Control (FC) credits is advertised as programmed for each type of Header and Payload. After VC0 FC initialization is complete, the FC credits received are transferred to the TL egress. The TL ingress must schedule an UpdateFC Data Link Layer Packet (DLLP) for transmission, to increase the quantity of advertised credits.

4.7.6 Flow Control Protocol

The PEX 8747 implements FC protocol that ensures that the switch:

- Does not transmit a TLP over a Link to a remote Receiver, unless the receiving device has sufficient VC Buffer space to accommodate the packet
- Generates FC credit updates to the remote Transmitter, to replace credits used to send TLPs to the PEX 8747

This FC is automatically managed by the hardware, and is transparent to software. Software is used only to enable additional Buffer space, to supplement the initial default buffer assignment.

The initial default FC credits, which are enabled after Link training, allow TLP traffic immediately after Link training completes. The Configuration transactions are the first transactions to use the default VC credits, to set up the initial device operating modes and capabilities.

The TL Ingress Credit Unit transmits DLLPs (referred to as *FC packets*) that update the FC to the remote Transmitter device, on a periodic basis. The DLLPs contain FC credit information that updates the Transmitter regarding the amount of available Buffer space in the PEX 8747.

The TL Egress Credit Unit receives DLLPs from the remote device, indicating the amount of Buffer space available in the remote Receiver. The unit uses this credit information to schedule the sending of TLPs to the remote device.



Chapter 5 Reset and Initialization

5.1 Reset

This section describes the resets supported by the PEX 8747.

Reset is a mechanism that returns a device to its initial state. Reset is propagated from Upstream to Downstream. Hardware or software mechanisms can trigger three different levels of reset – Fundamental, Hot, or Secondary Bus (each is described in the sections that follow). The re-initialized states following a reset vary, depending upon the reset type.

Table 5-1 summarizes each type of reset.

Table 5-1. Reset Summary

PCI Express Definition	Reset Source	Impact to Different Internal Components (upon De-Assertion)	Impact to Internal Registers
Fundamental Reset <ul style="list-style-type: none"> Cold Reset Warm Reset 	PEX_PERST# input assertion	<ul style="list-style-type: none"> Initializes everything Serial EEPROM contents are loaded HwInit types are evaluated 	All registers are initialized
Hot Reset	<ul style="list-style-type: none"> TS Ordered-Set <i>Hot Reset</i> bit is Set, at the Upstream Port Upstream Port enters the <i>DL_Down</i> state 	<ul style="list-style-type: none"> Initializes all Station Ports Initializes internal credits and queues Selectively reloads serial EEPROM contents 	All registers, except: <ul style="list-style-type: none"> Port Configuration registers All Sticky bits not affected by Hot Reset (HwInit, ROS, RW1CS, RWS)
Secondary Bus Reset	Downstream Port's Bridge Control register <i>Secondary Bus Reset</i> bit (offset 3Ch[22]) is Set	<ul style="list-style-type: none"> Downstream Port PHY generates a Hot Reset Downstream Port Data Link Layer (DLL) is down Downstream Port Transaction Layer (TL) is initialized, exhibits DL_Down behavior, and TLP Requests to that Port are dropped Upstream Port and Downstream Ports drain traffic, corresponding to the DL_Down condition on the Downstream Port, and initialize credits corresponding to that Downstream Port 	Does not affect registers (other than to initialize credits)
	Upstream Port's Bridge Control register <i>Secondary Bus Reset</i> bit (offset 3Ch[22]) is Set	<ul style="list-style-type: none"> All Downstream Ports propagate a Hot Reset DLL of each Downstream Port is down TL of each Downstream Port is initialized, exhibits DL_Down behavior, and drops TLP Requests that target Downstream Ports Upstream Port TL exhibits DL_Up behavior 	Initializes Downstream Ports registers to default values

5.1.1 Fundamental Reset

Fundamental Reset is a hardware mechanism defined by the *PCI Express Base r3.0*, Section 6.6. Fundamental Reset input, through the `PEX_PERST#` signal, resets all Port states and Configuration registers to default conditions.

5.1.2 Hot Reset

Hot Reset is an in-band Reset that propagates from an Upstream PCI Express Link to all its Downstream Ports, through the Physical Layer (PHY) mechanism. The PHY mechanism communicates a reset to Downstream devices through a training sequence (TS1/TS2 Ordered-Set, in which the *Hot Reset Training Control Bit* is Set). Hot Reset is also referred to as a *Soft Reset*.

A Hot Reset initializes all Ports, resets registers that are not defined as Sticky, and resets the serial EEPROM logic to reload registers from serial EEPROM, if present. Hot Reset does not reset the Clock logic, and can be caused by any of the following:

- Upstream Port PHY receives two consecutive TS1 Ordered-Sets in which the *Hot Reset Training Control bit* is Set. Hot Reset is generated from an Upstream device, *such as* by Setting its **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
- Upstream Port unexpectedly enters the *DL_Down* state.
Exception – If the Upstream Port Link is in the L2 Link PM state and the Link goes down, the Downstream Ports do *not* generate Hot Reset.
- Upstream Port PHY enters either the *Loopback* or *Disabled* state, upon receiving two consecutive TS1 or TS2 Ordered-Sets in which either the *Loopback* or *Disable Link Training Control bit* is Set, respectively. An Upstream device can generate the *Disable Link* sequence, by Setting its **Link Control** register *Link Disable* bit (offset 78h[4]).

5.1.3 Secondary Bus Reset

Any virtual Upstream or Downstream PCI-to-PCI bridge within the PEX 8747 can reset its Downstream hierarchy, by Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).

When the *Secondary Bus Reset* bit is Set on the Upstream Port, all the Downstream Ports are initialized to their default states, as defined by the *PCI Express Base r3.0*. Each of the Downstream Ports generates an in-band Hot Reset onto its Downstream Links. In addition, writable registers defined by the *PCI Express Base r3.0*, in all Downstream Ports, are initialized to default values (Upstream Port registers are not reset, and the serial EEPROM does not reload registers).

When the *Secondary Bus Reset* bit is Set on a Downstream Port, that Port is reset to its default state as defined by the *PCI Express Base r3.0*, and generates an in-band Hot Reset onto its Downstream Link. The registers of that Downstream Port are not affected.

5.1.4 Register Bits that Affect Hot Reset

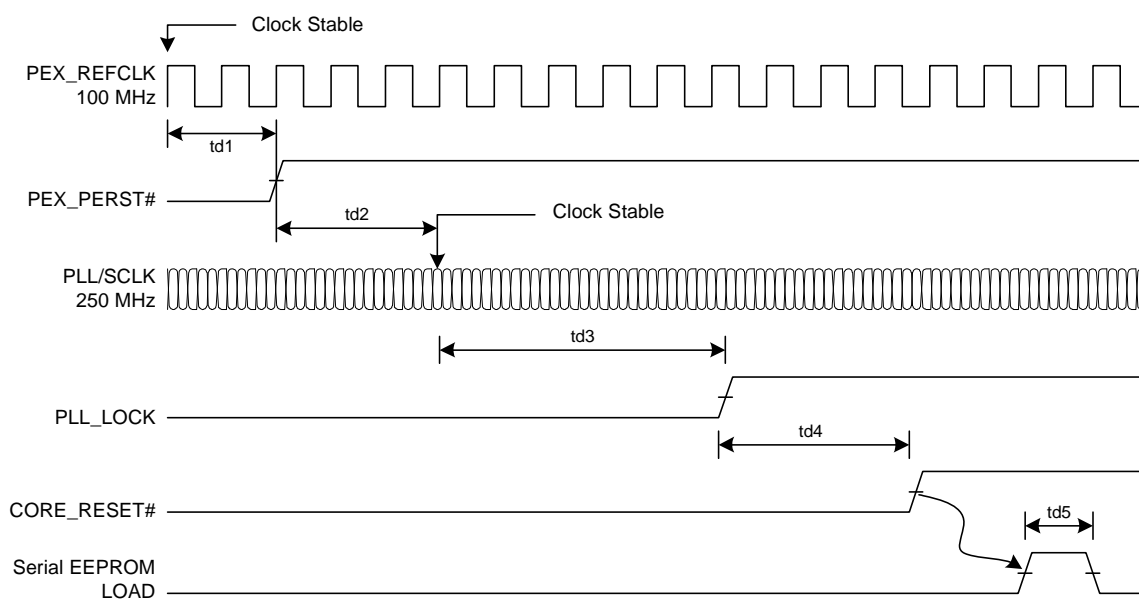
Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) generates a Hot Reset to Downstream Ports and Downstream devices.

5.1.5 Reset and Clock Initialization Timing

Table 5-2. Reset and Clock Initialization Timing

Symbol	Description	Typical Delay
td1	REFCLK stable to PEX_Reset release time	100 μ s
td2	PEX_Reset release to Reset de-bounce	1.32 ms
td3	Reset de-bounce to Phase-Locked Loop (PLL) Lock	105 μ s
td4	Reset de-bounce to Core Reset release	2.63 ms
td5	Serial EEPROM load time with no serial EEPROM present	17 μ s

Figure 5-1. Reset and Clock Initialization Timing



5.2 Initialization

The PEX 8747 initialization process starts upon exit from a Fundamental Reset. The serial EEPROM and/or I²C can be used to program initial register values, prior to BIOS/OS enumeration. If the [STRAP_I2C_SMBUS_CFG_EN#](#) input is Low, linkup of all Ports is delayed, until I²C software Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]).

Serial EEPROM download operates much faster than I²C access. I²C is relatively slow. Consequently, I²C initialization might not complete prior to the first BIOS/OS Configuration access, unless the system is designed to delay BIOS/OS Configuration access until the PCI Express subsystem is ready. If I²C is used to program the initial register values, and the PHY or DLL register values that affect SerDes parameters or Link initialization need to be changed, those registers must be programmed by serial EEPROM, so that the values are loaded prior to initial Link training.

5.2.1 Serial EEPROM Load Time

Serial EEPROM initialization loads only the Configuration register data that is specifically programmed into the serial EEPROM. Registers that are not included in the serial EEPROM data are initialized to default register values.

Each register entry in the serial EEPROM consists of two Address bytes and four Data bytes (refer to [Section 6.4, “Serial EEPROM Data Format”](#)); therefore, each register entry (6 bytes, or 48 bits) requires 48 serial EEPROM clocks to download. Thus, at the serial EEPROM clock default frequency of 1 MHz, after initial overhead to read the **Serial EEPROM Status** register (Port 0, offset 260h) (16 serial EEPROM clocks, or 16 μ s), plus another 40 serial EEPROM clocks (40 μ s) to begin reading the register data, each register entry in the serial EEPROM requires 48 μ s to download. A serial EEPROM containing 50 register entries (typical configuration, assuming the serial EEPROM is programmed only with non-default register values) and clocked at 1 MHz, takes approximately 5.2 ms to load ((16 + 40 + 48) x 50 μ s = 5,200 μ s).

To reduce the serial EEPROM initialization time, the first register entry in the serial EEPROM can increase the clock frequency, by programming the **Serial EEPROM Clock Frequency** register (Port 0, offset 268h), to a value of 2h (5 MHz), or 3h (9.62 MHz), if the serial EEPROM supports the higher frequency at the serial EEPROM supply voltage (typically 1.8 to 2.5V). At 5-MHz clocking, the serial EEPROM load time for 50 register entries can be reduced to approximately 575 μ s. Because the *PCI Express Base r3.0* allows a 20-ms budget for system hardware initialization, the default 1-MHz serial EEPROM clock is often sufficient when the quantity of Ports and registers programmed by serial EEPROM is relatively small.

5.2.2 I²C Load Time

Initialization using I²C is slower than serial EEPROM initialization, because the I²C Slave interface operates at a lower clock frequency (100 KHz maximum) and the quantity of bits per Register access is increased (because the Device address is included in the bit stream). Writing one register using 100-KHz clocking takes approximately 830 μ s (83 clock periods).

For further details, refer to [Section 7.2, “I2C Slave Interface.”](#)

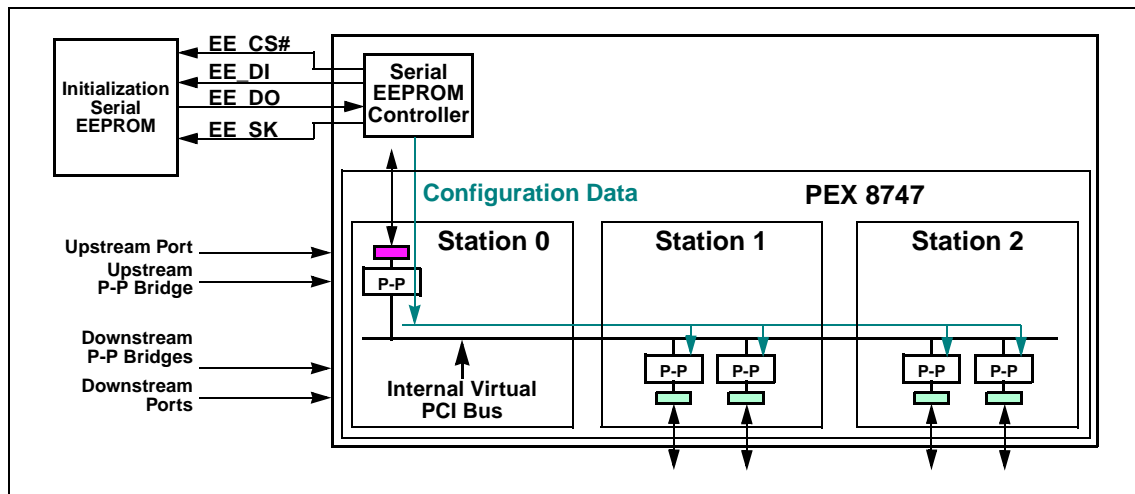
6.1 Overview

The PEX 8747 provides a Serial EEPROM Controller and interface to Serial Peripheral Interface (SPI)-compatible serial EEPROMs. (Refer to [Figure 6-1](#).) This interface consists of a Chip Select, Clock, Serial Data In, and Serial Data Out signals, and operates at a programmable frequency of up to 17.86 MHz. The PEX 8747 supports serial EEPROMs that use 1-, 2-, or 3-byte addressing; the PEX 8747 automatically determines the appropriate addressing mode.

The controller provides access to non-volatile memory. This external memory can be used for two different purposes:

- The serial EEPROM can be used to store register data, for switch configuration and initialization. When a serial EEPROM device is connected to the PEX 8747, immediately after reset, the Serial EEPROM Controller reads data from the serial EEPROM that is used to update the PEX 8747 register default values.
- System or application data can be stored into, and read from, the serial EEPROM, by software, I²C and/or SMBus, initiating random-access Read or Write Requests to the serial EEPROM.

Figure 6-1. Serial EEPROM Connections



Note: [Table 4-1](#) indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.

6.2 Features

- Detection of whether a serial EEPROM is present/not present
- Supports high-speed serial EEPROMs with Serial Peripheral Interface (SPI) interface
- Non-volatile storage for register default values loaded during Power-On Reset
- Cyclic Redundancy Check (CRC) compared on each download, to ensure data integrity prior to loading registers
- 4-byte Write/Read access to the serial EEPROM, through the Upstream Port and/or I²C/SMBus
- Serial EEPROM data format allows for loading registers by Station/Port/Address location
- Required serial EEPROM size is dependent upon the quantity of registers being changed
- Automatic support for 1-, 2-, or 3-byte-addressable serial EEPROMs
- Manual override for quantity of serial EEPROM Address bytes
- Programmable serial EEPROM clock frequency
- Programmable serial EEPROM clock-to-chip select timings

6.3 Serial EEPROM Load

The Serial EEPROM Controller performs a serial EEPROM download when the following conditions are met:

- Serial EEPROM is present^a, and
- Validation signature (first byte read from the serial EEPROM) value is [5Ah](#), and
- One of the following events occurs:
 - [PEX_PERST#](#) is returned High, following a Fundamental Reset (*such as* a Cold or Warm Reset to the entire PEX 8747)
 - Hot Reset is received at the Upstream Port (downloading upon this event can be optionally disabled, by Setting the **Debug** register [Disable Serial EEPROM Load on Hot Reset](#) and/or [Upstream Hot Reset Control](#) bit (Upstream Port, offset [A30h\[3\]](#) and/or [2](#)], respectively))
 - Upstream Port exits a *DL_Down* state (downloading upon this event can be optionally disabled, by Setting the **Debug** register [Upstream Port DL_Down Reset Propagation Disable](#) and/or [Upstream Hot Reset Control](#) bit (Upstream Port, offset [A30h\[4\]](#) and/or [2](#)], respectively))

a. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the [Status Data from Serial EEPROM](#) register bits (Port 0, offset [260h\[31:24\]](#)). Serial EEPROM presence is reported in the register's [EepPrsnt\[1:0\]](#) field (field [\[17:16\]](#)); a value of 01b or 11b indicates that the serial EEPROM is present.

6.4 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the format defined in [Table 6-1](#). The [Validation Signature](#) byte is located in the first address. The Serial EEPROM Controller reads this byte to determine whether a valid serial EEPROM image exists versus a blank image. REG_BYTE_COUNT[15:0] contains the quantity of bytes of serial EEPROM data to be loaded. It is equal to the quantity of registers to be loaded times 6 (6 serial EEPROM bytes, per register). If the REG_BYTE_COUNT[15:0] value is not a multiple of 6, the last incomplete register entry is ignored.

For the remaining register-related locations, data is written into a 2-byte address that represents the Configuration register offset and Port Number, and the 4 bytes following are the data loaded for that Configuration register. Only Configuration register data specifically programmed into the serial EEPROM is loaded after the PEX 8747 exits reset.

[Table 6-2](#) defines the Configuration register Address format (REGADDR[15:0] from [Table 6-1](#)):

- Bits [9:0] represent bits [11:2] of the Register address
- Bits [15:10] represent the Port Number of the register selected to be programmed by serial EEPROM

Because the PEX 8747 Serial EEPROM Controller always accesses 4 bytes of serial EEPROM data (for DWord-aligned Register addresses), register offsets are stored in the serial EEPROM as DWord address values.

To determine the 2-byte serial EEPROM value that represents the PEX 8747 Port and register offset, shift the register offset 2 bits to the right (divide by 4), then OR the resulting value with the appropriate Port Identifier value from [Table 6-2](#).

For example, to load Port 16 register offset FA8h, shift the address to the right by 2 bits (this becomes 07Eh) and concatenate 1000_00b. The resulting DWord address in the serial EEPROM will be 1000_0000_0111_1110b (807Eh).

6.4.1 Serial EEPROM Cyclic Redundancy Check

A Cyclic Redundancy Check (CRC) value is always calculated for serial EEPROM data stored in serial EEPROM addresses 2h through BYTE COUNT +3. If the value of “REG BYTE COUNT plus 2” is not a multiple of 4, the final data is still put into a CRC calculation, with unread byte(s) of the final DWord equal to 00h. Expansion ROM code (if present in the serial EEPROM content) is not included in the CRC calculation. The constant value used for CRC calculation is DB71_0641h. The calculated CRC value is always placed into the **Serial EEPROM CRC Value** register (Port 0, offset 270h), after serial EEPROM auto load.

There is an optional CRC checking at the end of serial EEPROM auto load. If bit 7 of the second byte (address 01h, following the **Validation Signature**) is Set, CRC checking is enabled. When CRC checking is performed, the calculated CRC value is compared to a stored CRC value read from serial EEPROM addresses [BYTE_COUNT+4] through [BYTE_COUNT+7]. If the calculated CRC value does not match the stored CRC value, the **Serial EEPROM Status** register *EepCRCErr* bit (Port 0, offset 260h[19]) is Set, and an Uncorrectable Internal Error is triggered in Port 0 of Station 0 (**Uncorrectable Error Status** register *Uncorrectable Internal Error Status* bit (Port 0, offset FB8h[22])). The serial EEPROM loading of registers is not aborted.

When programming the serial EEPROM, it is not necessary for software to calculate the CRC value that is to be stored within the serial EEPROM. Instead, CRC Checking can be initially disabled, then after the system is re-booted or reset (forcing EEPROM reload), the calculated CRC (from the Serial EEPROM CRC Value register) can be written to serial EEPROM addresses [BYTE_COUNT+4] through [BYTE_COUNT+7], and then CRC Checking can be enabled (by programming serial EEPROM address 01h to value 80h).

Table 6-1. Serial EEPROM Data Format

Location	Value	Description
0h	5Ah	Validation Signature
1h	–	Bit 7 = CRC checking enable ^a
2h	REG BYTE COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG BYTE COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1 st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1 st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1 st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1 st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1 st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1 st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2 nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2 nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2 nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2 nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2 nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2 nd Configuration Register Data (Byte 3)
...
End of Serial EEPROM data (BYTE COUNT +3)	REGDATA (Byte 3)	Last Configuration Register Data (Byte 3)
BYTE COUNT +4	Stored CRC Byte 0	Optional, used when CRC is enabled ^a
BYTE COUNT +5	Stored CRC Byte 1	
BYTE COUNT +6	Stored CRC Byte 2	
BYTE COUNT +7	Stored CRC Byte 3	

- a. *There is an optional CRC checking at the end of serial EEPROM auto load. Bit 7 of the second byte (after the 5Ah Validation Signature) determines whether CRC checking is to be performed. The CRC value is calculated for serial EEPROM addresses REG BYTE COUNT (LSB) (that is, 2h) through BYTE COUNT + 3. If the “REG BYTE COUNT (LSB)” value is not a multiple of 4, two additional bytes (of value 0h) are included in the calculation, so that CRC polynomial is always applied to DWord data.*

*The calculated CRC value is always placed into the **Serial EEPROM CRC Value** register (Port 0, offset 270h) after serial EEPROM auto load. If CRC checking is enabled, and the stored 32-bit CRC value read from the end of the serial EEPROM content does **not** match the calculated value:*

1. *The **Serial EEPROM Status** register **EepCRCErr** bit (Port 0, offset 260h[19]) is Set, and,*
2. *An Uncorrectable Internal error is triggered at Port 0 of Station 0 (**Uncorrectable Error Status** register **Uncorrectable Internal Error Status** bit (Port 0, offset FB8h[22]) is Set). The severity for Internal errors is Fatal, by default (**Uncorrectable Error Severity** register **Uncorrectable Internal Error Severity** bit (Port 0, offset FC0h[22]) is Set).*

*Serial EEPROM CRC errors do **not** inhibit serial EEPROM auto load of registers.*

Table 6-2. Configuration Register Address Format

Port Number ^a	REGADDR Bits [15:10] Value ^{b, c}	Port Identifier
Port 0	0000_00b	0000h
Port 8	0010_00b	2000h
Port 9	0010_01b	2400h
Port 16	0100_00b	4000h
Port 17	0100_01b	4400h

- a. Refer to [Table 4-1](#) for the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes. The table also indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.
- b. Encodings not listed are **Reserved**.
- c. REGADDR bits [15:13] indicate the Station Number. REGADDR bits [12:10] indicate the relative Port Number (0 or 1) within the Station.

6.5 Serial EEPROM Initialization

After the device Reset is de-asserted, the PEX 8747 determines whether a serial EEPROM is present. The serial EEPROM is considered to be present if it returns a value other than FFh in response to an initial Read Status command of its **Status** register, in which case this value is copied to the **Status Data from Serial EEPROM** register bits (Port 0, offset 260h[31:24]). Serial EEPROM presence is reported in the **Serial EEPROM Status** register *EepPrsnt[1:0]* field (Port 0, offset 260h[17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.

If a serial EEPROM is detected, the first byte (**Validation Signature**) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8747. The serial EEPROM address width is determined while the first byte is read. If the first byte's value is not 5Ah, the serial EEPROM is blank or programmed with invalid data. In this case, no more data is read from the serial EEPROM, and the **Serial EEPROM Status** register *EepAddrWidth* field (offset 260h[23:22]) reports a value of 00b (undetermined width).

If the *EepAddrWidth* field reports a value of 00b, any subsequent accesses to the serial EEPROM (through the PEX 8747 Serial EEPROM registers) default to a serial EEPROM address width of 1 byte, unless the **Serial EEPROM Status** register *EepAddrWidth Override* bit (offset 260h[21]) is Set. The *EepAddrWidth* field is usually Read-Only (RO); however, it is writable if the *EepAddrWidth Override* bit is Set (both can be programmed by a single Write instruction).

If the serial EEPROM contains valid data, the REG_BYTE_COUNT values in Bytes 2 and 3 determine the quantity of serial EEPROM locations that contain Configuration register addresses and data. Each Configuration register entry consists of 2 bytes of register Address and 4 bytes of register Write data. The REG_BYTE_COUNT must be a multiple of 6.

The **EE_SK** output clock frequency is determined by the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Port 0, offset 268h[2:0]). The default clock frequency is 1 MHz. At this clock rate, it takes approximately 48 μ s per DWORD during Configuration register initialization. For faster loading of large serial EEPROMs that support a faster clock, the first Configuration register load from the serial EEPROM could be to the **Serial EEPROM Clock Frequency** register.

There is an optional CRC checking at the end of serial EEPROM auto load. Bit 7 of the second byte (after the 5Ah **Validation Signature**) determines whether CRC checking is to be performed. The CRC value is calculated for serial EEPROM addresses 2h through BYTE COUNT +3. The calculated CRC value is always placed into the **Serial EEPROM CRC Value** register (Port 0, offset 270h) after serial EEPROM auto load. If CRC checking is enabled, and the stored 32-bit CRC value read from the end of the serial EEPROM content does not match the calculated value, an Uncorrectable Internal error is triggered at Port 0 of Station 0.

6.6 Serial EEPROM Registers

The Serial EEPROM register (Port 0, offsets 260h through 270h) parameters defined in [Section 11.16.5, "Device-Specific Registers – Serial EEPROM \(Offsets 260h – 270h\),"](#) can be changed, using the serial EEPROM. It is recommended that the first serial EEPROM entry be used to change the **Serial EEPROM Clock Frequency** register (offset 268h) value, to increase the clock frequency, and thereby reduce the time needed for the remainder of the serial EEPROM load. At the last serial EEPROM entry, the **Serial EEPROM Status and Control** register (offset 260h) can be programmed to issue a Write Status Register (WRSR) command, to enable the Write Protection feature(s) within the serial EEPROM data, if needed.

6.7 Serial EEPROM Random Write/Read Access

To access the serial EEPROM, a PCI Express, I²C, or SMBus Master uses the following Port 0 registers:

- **Serial EEPROM Status and Control** (offset 260h)
- **Serial EEPROM Buffer** (offset 264h)
- **Serial EEPROM 3rd Address Byte** (offset 26Ch)

***Note:** To help streamline the text in the following subsections, the specific Port location/access of each register offset is not repeated – only the offset location is mentioned.*

The Master can only access the serial EEPROM on a DWord basis (4 bytes aligned to one DWord address).

6.7.1 Writing to Serial EEPROM

To write a DWord to the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Write the 32-bit data into the **Serial EEPROM Buffer** register (offset 264h).
3. Issue a Write Enable instruction to the serial EEPROM (Command = 110b, Set Write Enable Latch), by writing the value 0000_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
4. Calculate and write the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Write Data instruction (value 010b) as the *EepCmd[2:0]* field [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into the register's *EepBlkAddr* field [12:0], and serial EEPROM Address bit 15 must be programmed into the **Serial EEPROM Status** register *EepBlkAddr Upper Bit* bit (*that is*, Set offset 260h[20] if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM). The data in the **Serial EEPROM Buffer** register is written to the serial EEPROM when the **Serial EEPROM Status and Control** register is written.
5. The serial EEPROM Write operation is complete when a subsequent read of the **Serial EEPROM Status** register *EepCmdStatus* bit (offset 260h[18]) returns a value of 0. At this time, another serial EEPROM access can be started.

Because each PEX 8747 Port and Register address value (REGADDR; refer to [Section 6.5](#)), and its corresponding Data value (REGDATA), require 6 bytes of serial EEPROM memory, and the PEX 8747 serial EEPROM interface accesses 4 bytes at a time, two serial EEPROM Writes may be needed to store each set of REGADDR (one word) and REGDATA (1 DWord) entries into the serial EEPROM. To avoid overwriting a word of another set of 6-byte REGADDR and REGDATA values, one of the two Serial EEPROM Writes might need to be a Read-Modify-Write type of operation (preserving one word read from the serial EEPROM, and writing the value back along with a new word value).

6.7.2 Reading from Serial EEPROM

To read a DWord from the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Calculate the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Read Data instruction (value 011b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM).
3. Poll the **Serial EEPROM Status** register until the *EepCmdStatus* bit (offset 260h[18]) is Cleared, which signals that the transaction is complete.
4. Read the four bytes of serial EEPROM data from the **Serial EEPROM Buffer** register (offset 264h).

For example, to read the first DWord in the serial EEPROM, write the value 0000_6000h to Port 0, register offset 260h, and then read Port 0, register offset 264h.

6.7.3 Programming a Blank Serial EEPROM

The PEX 8747 supports 1-, 2-, or 3-byte serial EEPROM addressing. 8-Kbit to 512-Kbit SPI EEPROMs use 2-byte addressing. The PEX 8747 requires that the first byte in the serial EEPROM must be the value 5Ah (ASCII Z), as a **Validation Signature**.

The 2nd and 3rd bytes contain the quantity of bytes within the serial EEPROM image, beginning with the first register entry at serial EEPROM address 04h. If this Byte Count value exceeds the actual quantity of register entries times 6 (*for example*, if the first DWord is programmed to the value 5A00_FFFFh), the system could hang. To simplify programming of a blank EEPROM (*such as* in a typical production build), the serial EEPROM could be pre-programmed with the first DWord, 0000_005Ah.

A 2-byte address serial EEPROM that is blank (or corrupted) can be programmed according to the following procedure (when the PEX 8747 is in 1-Byte Address mode).

To program a blank serial EEPROM:

1. Write the value 0000_005Ah into the **Serial EEPROM Buffer** register at address [Upstream Port **BAR0** + 264h].
2. Issue a Write Enable instruction (Command = 110b, Set Write Enable Latch, and enable 2-byte addressing, by writing the value 00A0_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
3. Copy this data value to serial EEPROM location 0, by writing the value 00A0_4000h into the **Serial EEPROM Status and Control** register. At this point, the first four bytes in the serial EEPROM now contain the value 0000_005Ah.
4. Reboot the system, to reset the PEX 8747 so that it re-detects the serial EEPROM.

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Chapter 7 I²C/SMBus Slave Interface Operation

7.1 Introduction

This chapter discusses the [I²C Slave Interface](#) and [SMBus Slave Interface](#).

7.2 I²C Slave Interface

7.2.1 I²C Support Overview

Note: This section applies to the I²C Slave interface, which uses the [I2C_ADDR0](#), [I2C_SCL0](#), and [I2C_SDA0](#) signals for PEX 8747 register access by an I²C Master.

Inter-Integrated Circuit (I²C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I²C Bus, and I²C devices that have I²C mastering capability can initiate a Data transfer. I²C is used for Data transfers between ICs at relatively low rates (100 Kbps), and is used in a variety of applications. For further details regarding I²C Buses, refer to the [I2C Bus, v2.1](#).

The PEX 8747 is an I²C Slave. Slave operations allow the PEX 8747 Configuration registers to be read from or written to by an I²C Master, external from the device. I²C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express Upstream Link.

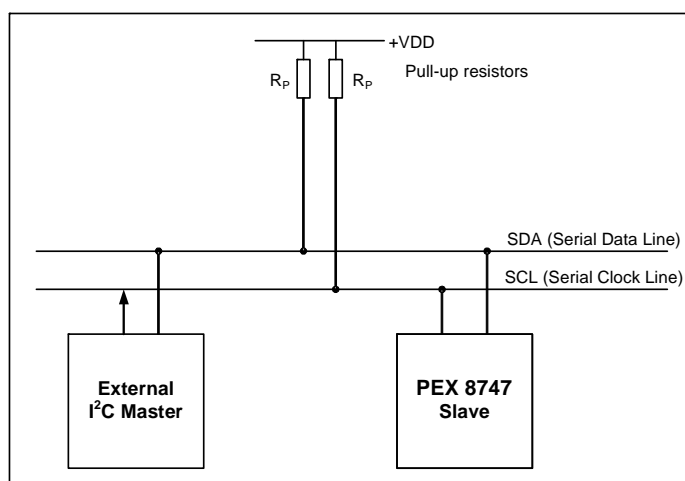
With I²C, users have the option of accessing all PEX 8747 registers through the I²C Slave interface. I²C provides an alternative to using a serial EEPROM, except the I²C/SMBus cannot access the registers (in time) prior to initial Link training (unless linkup is delayed by strapping the [STRAP_I2C_SMBUS_CFG_EN#](#) input Low, or by Clearing the [Configuration Release](#) register [Initiate Configuration](#) bit (Port 0, offset [3ACh\[0\]](#)) by serial EEPROM); therefore, the serial EEPROM is recommended for complete programmability options. I²C can also be used for debugging, such as if the PEX 8747 Upstream Port fails to linkup.

Accordingly, it is recommended that both I²C/SMBus access, and the serial EEPROM (or at least its footprint), be included in designs.

The I2C_SCL0 and I2C_SDA0 signals can be brought out to a 2x2 pin header on the board, to allow PLX software (*for example*, running on a laptop computer) to access the PEX 8747 registers, using an Aardvark USB-I²C adapter connected to this header. (Refer to the [PEX 8747 RDK Hardware Reference Manual](#) for the header pin design.)

Figure 7-1 provides a block diagram that illustrates how standard devices connect to the I²C Bus.

Figure 7-1. Standard Devices to I²C Bus Connection Block Diagram



7.2.2 I²C Addressing – Slave Mode Access

To access the PEX 8747 Configuration registers through the I²C Slave interface, the PEX 8747 I²C Slave address must be configured.

The PEX 8747 supports a 7-bit I²C Slave address, defined by the `I2C_ADDR0` 3-state input, which can be strapped Low (0), left floating (Z), or High (1), to select a different Slave address – `0111_000b`, `0111_001b`, or `0111_010b`, respectively.

Up to three PEX 8747 devices can share the same I²C Bus segment without conflict, provided that each PEX 8747 has its `I2C_ADDR0` 3-state input strapped to a unique state. More than three PEX 8747 devices can share the I²C Bus, however, if the upper Address bits are programmed in the serial EEPROM.

The Slave address can also be programmed by the serial EEPROM (if present; recommended, if the default address must be changed), or by a Memory Write, in the **I2C Configuration** register *Slave Address* field (Port 0, offset `294h[6:0]`). The bits of field [6:0] correspond to Address Byte bits [7:1], with bit 0 of the byte indicating a Write (0) or Read (1).

Note: *The I²C Slave address must not be changed by an I²C Write command.*

7.2.3 I²C Command Format

An I²C transfer starts as a packet with Address Phase bytes, followed by four Command Phase bytes, and one or more Data Phase bytes. The I²C packet Address Phase Byte format is illustrated in [Figure 7-2a](#). The I²C Command portion must include 4 bytes of data that contain the following:

- I²C Transfer type (Read/Write)
- PCI Express Configuration Register address
- PEX 8747 Port Number being accessed
- Byte Enable(s) of the register data being accessed

When the I²C Master is writing to the PEX 8747, the I²C Master must transmit the Data bytes to be written to that register within the same packet that contains the Command bytes. [Table 7-2](#) describes each I²C Command byte for Write access. [Figure 7-2b](#) illustrates the Command phase portion of an I²C Write packet.

When the I²C Master is reading from the PEX 8747, the I²C Master must separately transmit a Command Phase packet and Data Phase packet. [Table 7-6](#) describes each I²C Command byte for Read access. [Figure 7-4b](#) illustrates the Command phase portion of an I²C Read packet.

Each I²C packet must contain 4 bytes of data. Pad unused packet Data bytes with zeros (0) to meet this requirement.

7.2.4 I²C Register Write Access

The PEX 8747 Configuration registers can be read from and written to, based upon I²C register Read and Write operations, respectively. An I²C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I²C Data bytes. [Table 7-1](#) defines mapping of the I²C Data bytes to the Configuration register Data bytes. [Figure 7-2c](#) illustrates the I²C Data byte format.

The I²C packet starts with the *S* (START condition) bit. Data bytes are separated by the *A* (Acknowledge Control Packet (ACK)) or *N* (Negative Acknowledge (NAK)) bit. The packet ends with the *P* (STOP condition) bit.

If the Master generates an invalid command, the targeted PEX 8747 register is not modified.

The PEX 8747 considers the 1st Data byte of the 4-byte Data phase, following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively. Four Data bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I²C Master sends more than the four Data bytes (violating PEX 8747 protocol), the PEX 8747 returns a NAK for the extra Data byte(s). (For further details regarding I²C protocol, refer to the [I2C Bus, v2.1](#).)

[Table 7-2](#) describes each I²C Command byte for Write access. In the packet described in [Figure 7-2](#), Command Bytes 0 through 3 for Writes follow the format specified in [Table 7-2](#).

Table 7-1. I²C Register Write Access

I ² C Data Byte Order	PCI Express Configuration Register Bytes
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-2. I²C Command Format for Write Access

Field (Byte) On Bus	Bit(s)	Value/Description										
Command Byte 1	7:3	Reserved Should be Cleared.										
	2:0	Command 011b = Write register Do not use other encodings for Writes.										
Command Byte 2	7:6	Reserved Should be Cleared.										
	5:4	Access Mode Default is 00b. All other encodings are Reserved .										
	3:2	Station Select 00b = Station 0 01b = Station 1 10b = Station 2 11b = Reserved										
	1:0	Port Select, Bits [2:1]										
Command Byte 3	7	Port Select, Bit 0 <i>Port Select[2:0] selects the Port to access, as indicated by Station Select.</i> 000b = Port 0 of the Station 001b = Port 1 of the Station (Stations 1 and 2 Only) Note: If Port 1 of the Station is not enabled, 001b is Reserved . All other encodings are Reserved .										
	6	Reserved Should be Cleared.										
	5:2	Byte Enables <table><tr><th>Bit</th><th>Description</th></tr><tr><td>2</td><td>Byte Enable for Byte 0 (PEX 8747 register bits [7:0])</td></tr><tr><td>3</td><td>Byte Enable for Byte 1 (PEX 8747 register bits [15:8])</td></tr><tr><td>4</td><td>Byte Enable for Byte 2 (PEX 8747 register bits [23:16])</td></tr><tr><td>5</td><td>Byte Enable for Byte 3 (PEX 8747 register bits [31:24])</td></tr></table> 0 = Corresponding PEX 8747 register byte will not be modified 1 = Corresponding PEX 8747 register byte will be modified All 16 combinations are valid values.	Bit	Description	2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])	3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])	4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])	5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])
	Bit	Description										
2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])											
3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])											
4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])											
5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])											
1:0	PEX 8747 Register Address, Bits [11:10]											
Command Byte 4	7:0	PEX 8747 Register Address [9:2] Note: All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I ² C byte Writes.										

Figure 7-2. I²C Write Packet**Figure 7-2a I²C Write Packet Address Phase Bytes**

1 st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-2b I²C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

Figure 7-2c I²C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 (to selected register Byte 3)	A	Data Byte 1 (to selected register Byte 2)	A	Data Byte 2 (to selected register Byte 1)	A	Data Byte 3 (to selected register Byte 0)	A	P

7.2.4.1 I²C Register Write Example

The following tables illustrate a sample I²C packet for writing the PEX 8747 **MSI Upper Address** register (offset **50h**) for Port 9 (Port 1 of Station 1) with data 1234_5678h.

Note: The PEX 8747 has a default I²C Slave address value of **0111_000b**, **0111_001b**, or **0111_010b**, according to whether the **I2C_ADDR0** 3-state input is strapped Low (0), left floating (Z), or High (1), respectively. The actual address is reflected in the **I2C Configuration** register **Slave Address** field (Port 0, offset **294h**[6:0]).

The following example assumes the I²C Slave address is 0111_000b (I2C_ADDR0=0). The byte sequence on the I²C Bus, as listed in the following tables and figures, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Table 7-3. I²C Register Write Access Example – 1st Cycle

Phase	Value	Value/Description
Address	70h	Bits [7:1] for PEX 8747 I²C Slave Address (0111_000b) Last bit (bit 0) for Write = 0.

Table 7-4. I²C Register Write Access Example – Command Cycle

Byte	Value	Value/Description
0	03h	[7:3] Reserved Should be Cleared. [2:0] Command 011b = Write register
1	02h	[7:6] Reserved Should be Cleared. [5:4] Access Mode [3:2] Station Select [1:0] Port Select, Bits [2:1]
2	BCh	7 Port Select, Bit 0 6 Reserved Should be Cleared. [5:2] Byte Enables All active. [1:0] PEX 8747 Register Address, Bits [11:10]
3	14h	[7:0] PEX 8747 Register Address [9:2]

Table 7-5. I²C Register Write Access Example – Write Cycle

Byte	Value	Description
0	12h	Data to Write for Byte 3
1	34h	Data to Write for Byte 2
2	56h	Data to Write for Byte 1
3	78h	Data to Write for Byte 0

Figure 7-3. I²C Write Command Packet Example
Figure 7-3a I²C Write Packet Address Phase Bytes

1 st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 0 = Write	A

Figure 7-3b I²C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0 0000_0011b	A	Command Byte 1 0000_0010b	A	Command Byte 2 1011_1100b	A	Command Byte 3 0001_0100b	A

Figure 7-3c I²C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 0001_0010b	A	Data Byte 1 0011_0100b	A	Data Byte 2 0101_0110b	A	Data Byte 3 0111_1000b	A	P

7.2.5 I²C Register Read Access

When the I²C Master attempts to read a PEX 8747 register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the [I2C Bus, v2.1](#), a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I²C Read access occurs, the internal buffer value is transferred on to the I²C Bus, starting from Byte 3 (bits [31:24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I²C Master requests more than four bytes, the PEX 8747 re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I²C Read packets (illustrated in [Figure 7-4](#) and [Figure 7-5](#), respectively) perform the following functions:

- **1st packet** – Selects the register to read
- **2nd packet** – Reads the register (sample 2nd packet provided is for a 7-bit PEX 8747 I²C Slave address)

Although two packets are shown for the I²C Read, the I²C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

[Table 7-6](#) describes each I²C Command byte for Read access. In the packet described in [Figure 7-4](#), Command Bytes 0 through 3 for Reads follow the format specified in [Table 7-6](#).

Table 7-6. I²C Command Format for Read Access

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 1	7:3	Reserved Should be Cleared.
	2:0	Command 100b = Read register Do not use other encodings for Reads.
Command Byte 2	7:6	Reserved Should be Cleared.
	5:4	Access Mode Default is 00b. All other encodings are Reserved .
	3:2	Station Select 00b = Station 0 01b = Station 1 10b = Station 2 11b = Reserved
	1:0	Port Select, Bits [2:1]

Table 7-6. I²C Command Format for Read Access (Cont.)

Field (Byte) On Bus	Bit(s)	Value/Description										
Command Byte 3	7	Port Select, Bit 0 <i>Port Select[2:0]</i> selects the Port to access, as indicated by <i>Station Select</i> . 000b = Port 0 of the Station 001b = Port 1 of the Station (Stations 1 and 2 Only) Note: <i>If Port 1 of the Station is not enabled, 001b is Reserved.</i> All other encodings are Reserved .										
	6	Reserved Should be Cleared.										
	5:2	Byte Enables <table><thead><tr><th>Bit</th><th>Description</th></tr></thead><tbody><tr><td>2</td><td>Byte Enable for Byte 0 (PEX 8747 register bits [7:0])</td></tr><tr><td>3</td><td>Byte Enable for Byte 1 (PEX 8747 register bits [15:8])</td></tr><tr><td>4</td><td>Byte Enable for Byte 2 (PEX 8747 register bits [23:16])</td></tr><tr><td>5</td><td>Byte Enable for Byte 3 (PEX 8747 register bits [31:24])</td></tr></tbody></table> 0 = Corresponding PEX 8747 register byte will not be modified 1 = Corresponding PEX 8747 register byte will be modified All 16 combinations are valid values.	Bit	Description	2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])	3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])	4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])	5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])
	Bit	Description										
2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])											
3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])											
4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])											
5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])											
1:0	PEX 8747 Register Address, Bits [11:10]											
Command Byte 4	7:0	PEX 8747 Register Address [9:2] Note: <i>All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, for the I²C Read.</i>										

Figure 7-4. I²C Read Command Packet (1st Packet)**Figure 7-4a I²C Read Command Packet Address Phase Bytes**

1 st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-4b I²C Read Command Packet Command Phase Bytes

Command Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A	P

Figure 7-5. I²C Read Data Packet (2nd Packet)**Figure 7-5a I²C Read Data Packet Address Phase Bytes**

1 st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit, 1 = Read	A

Figure 7-5b I²C Read Data Packet Data Phase Bytes

Read Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

7.2.5.1 I²C Register Read Address Example – Phase and Command Packet

The following is a sample I²C packet for reading the PEX 8747 **MSI Upper Address** [63:32] register (offset **50h**) in Port 9 (Port 1 of Station 1), assuming the register value is ABCD_EF01h.

Note: The PEX 8747 has a default I²C Slave address value of **0111_000b**, **0111_001b**, or **0111_010b**, according to whether the **I2C_ADDR0** 3-state input is strapped Low (0), left floating (Z), or High (1), respectively. The actual address is reflected in the **I2C Configuration** register **Slave Address** field (Port 0, offset **294h**[6:0]).

The following example assumes the I²C Slave address is 0111_000b (I2C_ADDR0=0). The byte sequence on the I²C Bus, as listed in the following tables, occurs after the START and before the STOP bits, by which the I²C Master frames the transfer.

Table 7-7. I²C Register Read Access Example – 1st Packet

Phase	Value	Value/Description
Address	70h	Bits [7:1] for PEX 8747 I²C Slave Address (0111_000b) Last bit (bit 0) for Write = 0.

Table 7-8. I²C Register Read Access Example – Command Cycle

Byte	Value	Value/Description
0	04h	[7:3] Reserved Should be Cleared. [2:0] Command 100b = Read register
1	02h	[7:6] Reserved Should be Cleared. [5:4] Access Mode [3:2] Station Select [1:0] Port Select, Bits [2:1]
2	BCh	7 Port Select, Bit 0 6 Reserved Should be Cleared. [5:2] Byte Enables All active. [1:0] PEX 8747 Register Address, Bits [11:10]
3	14h	[7:0] PEX 8747 Register Address [9:2]

7.3 SMBus Slave Interface

7.3.1 SMBus Features

- Compliant to the *SMBus v2.0*
- Supports the SMBus Slave function only
- PEX 8747 internal registers can be read and written, through the SMBus Slave interface
- Supports Address Resolution Protocol (ARP-capable)
- [I2C_ADDR0](#) input state, serial EEPROM, software, and/or ARP define the SMBus Device address
- Supports Block Read, Block Write, and Block Write - Block Read Process Call commands to access the registers
- Supports Packet Error Checking
- 10 to 100 KHz Bus operation frequency range

7.3.2 SMBus Operation

Based upon I²C's principles of operation, SMBus is a two-wire bus used for communication between IC components and the remainder of the system. Electrically, I²C and SMBus devices are compatible, and both protocol devices can co-exist on the same bus. Multiple devices, both Masters and Slaves, can be connected to an SMBus segment. PCI Express cards have two optional SMBus pins defined on the connector – SMCLK and SMDAT.

The PEX 8747 implements an *SMBus v2.0*-compliant Slave device, and is used to read and write PEX 8747 registers, through SMBus commands. The PEX 8747 SMBus uses the same SDA Data and SCL Clock balls that are used for I²C. Additionally, the SMBus Device Address is the same value as the I²C Slave address, used by the I²C protocol (default addresses [0111_000b](#), [0111_001b](#), or [0111_010b](#), according to whether the [I2C_ADDR0](#) 3-state input is strapped Low (0), left floating (Z), or High (1), respectively). At any time, either the I²C or SMBus feature is enabled, dependent upon the **SMBus Configuration** register *SMBus Enable* bit (Port 0, offset [2C8h\[0\]](#)) state, which is latched (at Fundamental Reset) according to the [STRAP_I2C_SMBUS_EN](#) 3-state input, to one of the following protocols:

- 0 = I²C (*SMBus Enable* bit is Cleared)
- Z, 1 = SMBus with ARP (*SMBus Enable* bit is Set)

Software can toggle the *SMBus Enable* bit to change between I²C and SMBus functionality.

The PEX 8747 SMBus logic also supports the commands that are required to support ARP. ARP is a feature specific to *SMBus v2.0*, through which an SMBus ARP Master can dynamically assign a unique address to each of the SMBus Targets residing on the same bus. Although ARP is an optional feature of the *SMBus v2.0*, PCI and PCI Express cards are required to support ARP. The ARP feature is enabled when the **SMBus Configuration** register *ARP Disable* bit (Port 0, offset [2C8h\[8\]](#)) is Cleared; this bit is initially latched (at Fundamental Reset) according to the [STRAP_I2C_SMBUS_EN](#) input state, as described above.

The PEX 8747 also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the *SMBus v2.0*. The *SMBus v2.0* optional feature, *Notify ARP Master* (which requires Master capability on the SMBus) is *not* supported.

7.3.3 Supported SMBus Commands

For register access, the SMBus logic supports three commands:

- Block Write (command BEh) is used to write the registers
- Block Write (command BAh), followed by Block Read (command BDh), can be used to read the registers
- Block Write - Block Read Process Call (commands BAh, CDh) can also be used to read registers

Unsupported SMBus commands – Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read Word, and Process Call – are NACKed.

7.3.3.1 SMBus Block Write

The Block Write command is used to write to the PEX 8747 registers. General SMBus Block Writes are illustrated in [Figure 7-6](#) and [Figure 7-7](#). The sequence of Bytes include the following, in the sequence listed:

- 7-bit address,
- Command Code that indicates it is Block Write,
- *Byte Count* field with a value of 8h that indicates 4 bytes to set up the register to write (Port Number, register address, Command Byte Enable, and so forth), followed by
- 4 bytes of data to be written into the register

[Figure 7-8](#) explains the elements used in [Figure 7-6](#) and [Figure 7-7](#), and [Figure 7-9](#) indicates the Data Bytes written.

Figure 7-6. SMBus Block Write Command Format, to Write to a PEX 8747 Register without PEC

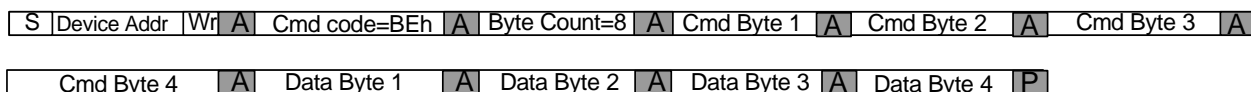


Figure 7-7. SMBus Block Write Command Format, to Write to a PEX 8747 Register with PEC

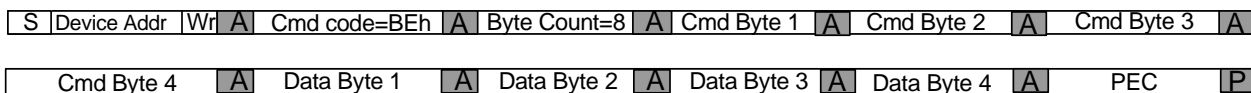


Figure 7-8. SMBus Packet Protocol Diagram Element Key

- S -> START condition
P -> STOP condition
- A -> Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)
- > Master to Slave
 -> Slave to Master

Figure 7-9. SMBus Block Write Bytes, as Written to Register

31:24	23:16	15:8	7:0
Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4

Note: In each byte, the Most Significant Byte (MSB) is transmitted first.

Table 7-9 provides a description of bytes for an SMBus Block Configuration Space register (CSR) Write.

Block Write transactions that are received with incorrect byte Settings are NACKed, starting from the wrong byte Setting, and including subsequent bytes in the packet. *For example*, if the Byte Count value is not 8, the PEX 8747 NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PEX 8747 drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Port 0, offset 2C8h[9]). The Byte Count value, by definition, does not include the PEC byte.

Table 7-9. Bytes for Block CSR Write on SMBus

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BEh for Block Write.
Byte Count	7:0	08h = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted.
Command Byte 1	7:3	Reserved Should be Cleared.
	2:0	Command 011b = Write register Do not use other encodings for Writes.
Command Byte 2	7:6	Reserved Should be Cleared.
	5:4	Access Mode Default is 00b. All other encodings are Reserved .
	3:2	Station Select 00b = Station 0 01b = Station 1 10b = Station 2 11b = Reserved
	1:0	Port Select, Bits [2:1]

Table 7-9. Bytes for Block CSR Write on SMBus (Cont.)

Field (Byte) On Bus	Bit(s)	Value/Description										
Command Byte 3	7	Port Select, Bit 0 <i>Port Select[2:0]</i> selects the Port to access, as indicated by <i>Station Select</i> . 000b = Port 0 of the Station 001b = Port 1 of the Station (Stations 1 and 2 Only) Note: If Port 1 of the Station is not enabled, 001b is Reserved . All other encodings are Reserved .										
	6	Reserved Should be Cleared.										
	5:2	Byte Enables <table><thead><tr><th>Bit</th><th>Description</th></tr></thead><tbody><tr><td>2</td><td>Byte Enable for Byte 0 (PEX 8747 register bits [7:0])</td></tr><tr><td>3</td><td>Byte Enable for Byte 1 (PEX 8747 register bits [15:8])</td></tr><tr><td>4</td><td>Byte Enable for Byte 2 (PEX 8747 register bits [23:16])</td></tr><tr><td>5</td><td>Byte Enable for Byte 3 (PEX 8747 register bits [31:24])</td></tr></tbody></table> 0 = Corresponding PEX 8747 register byte will not be modified 1 = Corresponding PEX 8747 register byte will be modified All 16 combinations are valid values.	Bit	Description	2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])	3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])	4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])	5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])
	Bit	Description										
2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])											
3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])											
4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])											
5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])											
1:0	PEX 8747 Register Address, Bits [11:10]											
Command Byte 4	7:0	PEX 8747 Register Address [9:2] Note: All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive SMBus byte Writes.										

7.3.3.2 SMBus Block Read

A Block Read command is used to read PEX 8747 registers. Similar to register Reads using I²C, an SMBus Write sequence must first be performed to select the register to read, followed by an SMBus Read of the corresponding register. There are two ways a PEX 8747 register can be read:

- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.
- Use a Block Write - Block Read Process Call. This command is defined by the *SMBus v2.0*, and performs a Block Write and Block Read, using a two-part message. The Block Write portion of the message sets up the register to be read, and then a repeated START followed by the Block Read portion of the message returns the register data specified by the Block Write.

Note: There is no STOP condition before the repeated START condition.

CSR Read, Using SMBus Block Write, Followed by SMBus Block Read

A general SMBus Block Write and Block Read sequence is illustrated in [Figure 7-10](#).

[Table 7-10](#) describes the Byte definitions for a Block Write bus protocol, to prepare for a subsequent Block Read of the PEX 8747 register.

The PEX 8747 always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command (listed in [Table 7-11](#)), the PEX 8747 returns a PEC to the Master if, after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PEX 8747 recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PEX 8747.

Figure 7-10. SMBus Block Write to Set up Read, and Resulting Read that Returns CSR Value

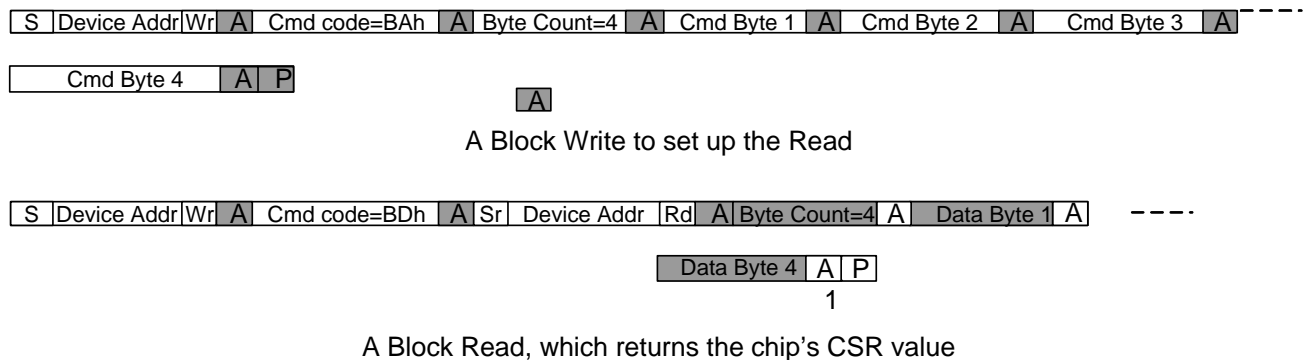


Table 7-10. SMBus Block Read Bytes

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BAh, to set up the Read, using Block Writes.
Byte Count	7:0	04h = 4 Command bytes.
Command Byte 1	7:3	Reserved Should be Cleared.
	2:0	Command 100b = Read register Do not use other encodings for Reads.
Command Byte 2	7:6	Reserved Should be Cleared.
	5:4	Access Mode Default is 00b. All other encodings are Reserved .
	3:2	Station Select 00b = Station 0 01b = Station 1 10b = Station 2 11b = Reserved
	1:0	Port Select, Bits [2:1]

Table 7-10. SMBus Block Read Bytes (Cont.)

Field (Byte) On Bus	Bit(s)	Value/Description										
Command Byte 3	7	Port Select, Bit 0 <i>Port Select[2:0] selects the Port to access, as indicated by Station Select.</i> 000b = Port 0 of the Station 001b = Port 1 of the Station (Stations 1 and 2 Only) <i>Note: If Port 1 of the Station is not enabled, 001b is Reserved.</i> All other encodings are Reserved .										
	6	Reserved Should be Cleared.										
	5:2	Byte Enables <table><thead><tr><th>Bit</th><th>Description</th></tr></thead><tbody><tr><td>2</td><td>Byte Enable for Byte 0 (PEX 8747 register bits [7:0])</td></tr><tr><td>3</td><td>Byte Enable for Byte 1 (PEX 8747 register bits [15:8])</td></tr><tr><td>4</td><td>Byte Enable for Byte 2 (PEX 8747 register bits [23:16])</td></tr><tr><td>5</td><td>Byte Enable for Byte 3 (PEX 8747 register bits [31:24])</td></tr></tbody></table> 0 = Corresponding PEX 8747 register byte will not be modified 1 = Corresponding PEX 8747 register byte will be modified All 16 combinations are valid values.	Bit	Description	2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])	3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])	4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])	5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])
	Bit	Description										
2	Byte Enable for Byte 0 (PEX 8747 register bits [7:0])											
3	Byte Enable for Byte 1 (PEX 8747 register bits [15:8])											
4	Byte Enable for Byte 2 (PEX 8747 register bits [23:16])											
5	Byte Enable for Byte 3 (PEX 8747 register bits [31:24])											
1:0	PEX 8747 Register Address, Bits [11:10]											
Command Byte 4	7:0	PEX 8747 Register Address [9:2] <i>Note: All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, for the SMBus Read.</i>										

Table 7-11. Command Format for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Cmd Code	7:0	CDh, for Block Read (Process Call Rea D).

7.3.3.3 CSR Read, Using SMBus Block Write - Block Read Process Call

A general SMBus Block Write - Block Read Process Call sequence is illustrated in [Figure 7-11](#). Alternatively, a general SMBus Block Write - Block Read Process Call with PEC sequence is illustrated in [Figure 7-12](#).

Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition.

[Table 7-11](#) lists the Command format for Block Read.

Figure 7-11. CSR Read Operation Using SMBus Block Write - Block Read Process Call

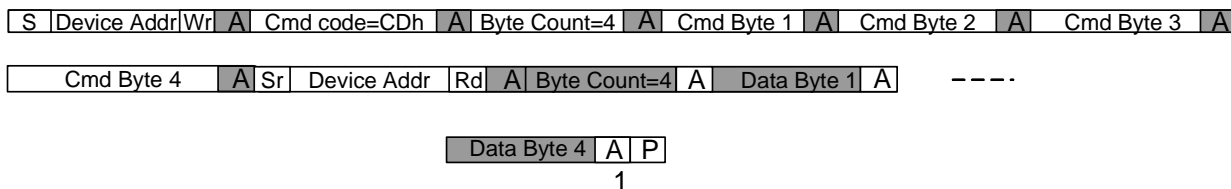
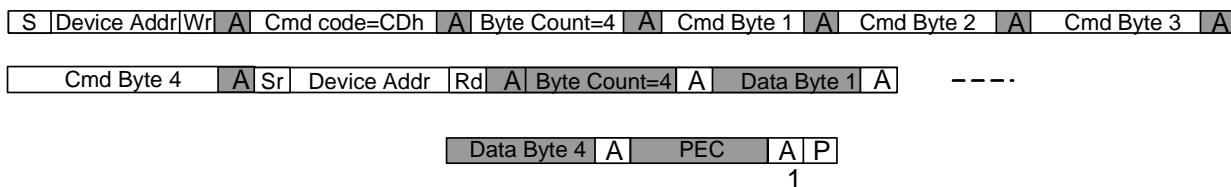


Figure 7-12. CSR Read Operation Using SMBus Block Write - Block Read Process Call with PEC



7.3.4 SMBus Address Resolution Protocol

Address Resolution Protocol (ARP) is a protocol by which SMBus devices that implement an assignable SMBus Device address feature are enumerated and dynamically assigned non-conflicting Device addresses, rather than using a fixed Device address. Although optional in the *SMBus v2.0*, it is mandatory per the *PCI r3.0* for add-in boards, to support ARP. This feature avoids conflicts with addresses used by other devices on a motherboard. ARP also allows multiple devices of the same type to co-exist on the same bus segment, without address conflicts.

To support this feature, a Slave device must implement a unique 128-bit ID, called *Unique Device Identifier (UDID)*. The fields of this ID are provided in [Figure 7-13](#). All ARP commands use the default Device Address, 1100_001b. There are also two flags that the SMBus devices must implement to support the ARP process:

- **Address Resolved flag (AR)** – A flag bit or device internal state that indicates whether the ARP Master has resolved the device's SMBus Device address
- **Address Valid flag (AV)** – A flag bit or device internal state that indicates whether the device's SMBus Device address is valid

The process of assigning an SMBus Device address starts with the ARP Master issuing a Reset Device or Prepare to ARP command, using the default Device Address. This Clears the AR flag in the Slave device (both flags are Cleared by a Reset Device command). The Master then issues a general Get UDID command. This causes all devices that support ARP to start driving their UDID onto the serial bus. A Target that loses the SMBus arbitration, backs off. Arbitration loss means that a device keeps the SMDAT line floating and it detects 0 driven by another device on the bus. Slave devices that lose arbitration issue NACK in response to further Bytes transmitted on the bus. After the ARP Master finishes the Get UDID sequence, it issues a Set Address command to the Slave device, using the Slave's UDID. All Slave devices on the bus monitor the UDID that is transmitted by the ARP Master, but only the particular device that has the matching UDID adopts the new SMBus Device address, and Sets its own AV and AR flags. After the Slave device sets its AR flag, that device no longer responds to a general Get UDID command, which allows other devices to participate in the ARP process. All ARP commands require PEC checking and generation.

7.3.4.1 SMBus UDID

The 128-bit UDID is comprised of the following fields, as illustrated in [Figure 7-13](#) (not to scale). Each UDID field and its default value implemented in the PEX 8747 and meaning are explained in the tables that follow.

Figure 7-13. 128-Bit SMBus UDID

8 bits	8 bits	16 bits	16 bits	16 bits	16 bits	16 bits	32 bits
127:120	119:112	111:96	95:80	79:64	63:48	47:32	31:0
Device Capability	Version/Revision	Vendor ID	Device ID	Interface	Subsystem Vendor ID	Subsystem Device ID	Vendor-Specific ID

Table 7-12. SMBus Vendor-Specific ID [31:0]

Field	Name	Default Value	Description
31:0	Vendor-Specific ID	Depends upon the I2C_ADDR0 input state, which provides the following ID values: 0 = 7000_0000h Z = B000_0000h 1 = D000_0000h	The Vendor-Specific ID is used to provide a unique ID for functionally equivalent devices. This is for devices that would otherwise return identical UDIDs for the purpose of dynamic address assignment. The I2C_ADDR0 3-state input produces three unique Vendor-Specific ID values, for a maximum of three SMBus-enabled PEX 8747 switches to co-exist on the same SMBus segment.

Table 7-13. SMBus Subsystem Device ID [47:32]

Field	Name	Default Value	Description
15:0	Subsystem Device ID	8747h	PLX part number for the PEX 8747.

Table 7-14. SMBus Subsystem Vendor ID [63:48]

Field	Name	Default Value	Description
15:0	Subsystem Vendor ID	10B5h	PLX Vendor ID.

Table 7-15. SMBus Interface [79:64]

Field	Name	Default Value	Description
3:0	SMBus Version	0100b	<i>SMBus</i> v2.0.
15:4	<i>Reserved</i>	000h	Supported protocols.

Table 7-16. SMBus Device ID [95:80]

Field	Name	Default Value	Description
15:0	Device ID	8747h	PEX 8747 default Device ID value.

Table 7-17. SMBus Vendor ID [111:96]

Field	Name	Default Value	Description
15:0	Vendor ID	10B5h	PLX Vendor ID.

Table 7-18. SMBus Version/Revision [119:112]

Field	Name	Default Value	Description
2:0	Silicon Revision ID	001b	PEX 8747, Silicon Revisions BA.
5:3	UDID Version	001b	UDID version defined for the <i>SMBus</i> v2.0.
7:6	<i>Reserved</i>	00b	

Table 7-19. SMBus Device Capability [127:120]

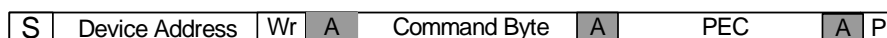
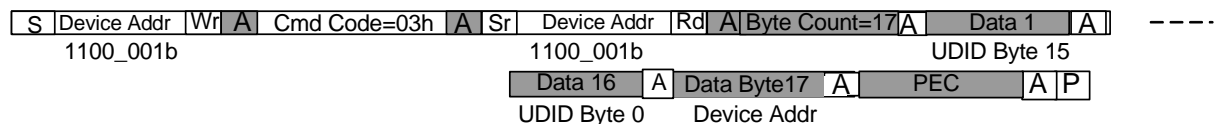
Field	Name	Default Value	Description
0	PEC Supported	1	By default, PEC generation and checking are enabled.
5:1	<i>Reserved</i>	00_000b	
7:6	Address Type	10b	The PEX 8747 SMBus Address Type is implemented as dynamic and volatile. 00b = Fixed address 01b = Dynamic and persistent 10b = Dynamic and volatile (default) 11b = Random number device

7.3.4.2 Supported SMBus ARP Commands

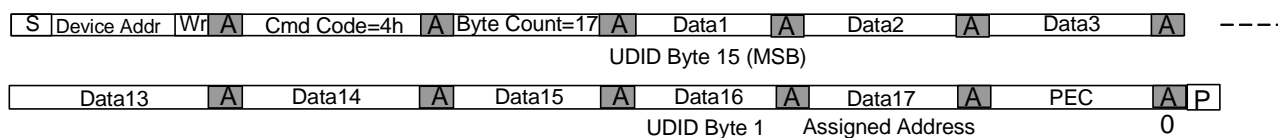
The PEX 8747 supports all ARP Slave commands. The Notify ARP Master command, which requires Master functionality, is *not* supported. Table 7-20 explains the PEX 8747 response to each received ARP command.

Table 7-20. Supported SMBus ARP Commands, Format, and Actions

ARP Command	SMBus Command Format	SMBus Device Address	Command Code	Action
Prepare to ARP (Only General)	Send Byte (Refer to Figure 7-14)	SMBus default Device Address 1100_001b	01h	Clear the <i>AR Flag</i> and prepare for the ARP process. <i>AV Flag</i> will have no change.
Reset Device (General)	Send Byte (Refer to Figure 7-14)	SMBus default Device Address 1100_001b	02h	Clear the <i>AR Flag</i> and <i>AV Flag</i> .
Reset Device (Directed)	Send Byte (Refer to Figure 7-14)	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 0	If the <i>AV Flag</i> is Set, Set ACK and Clear the <i>AR Flag</i> and <i>AV Flag</i> ; else, NACK/REJECT.
Get UDID (General)	Block Read (Refer to Figure 7-15)	SMBus default Device Address 1100_001b	03h	Respond only if the <i>AR Flag</i> is Cleared; else, NACK/REJECT. <i>AR Flag</i> and <i>AV Flag</i> are not changed. Address returned is all ones (1), if the <i>AV Flag</i> is Cleared.
Get UDID (Directed)	Block Read	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 1	<i>AR Flag</i> and <i>AV Flag</i> are not changed. ACK if <i>AV Flag</i> =1; else, NACK/REJECT. Data Byte 17 returned will be the SMBus Device address.
Assign Address ARP	Block Write (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	04h	Always ACK and Set the <i>AR Flag</i> and <i>AV Flag</i> , if the UDID matches.

Figure 7-14. Prepare SMBus ARP Command and SMBus Reset Device Command Format**Figure 7-15. Get SMBus UDID Command Format (General Get UDID Command with PEC)**

Note: If the **SMBus Configuration** register **AR Flag** bit (Port 0, offset 2C8h[11]) is Cleared, the device returns the register's **SMBus Device Address** field (Port 0, offset 2C8h[7:1]) as 1111_111b; otherwise, it returns the device **SMBus Device address**. Bit 0 (LSB) in the Data Byte 17 field should be 1.

Figure 7-16. Assign SMBus Address ARP Command Format

Note: Bit 0 (LSB) of the Data 17 field is ignored in the Assign Address command field.

7.3.5 SMBus PEC Handling

The PEX 8747 supports the optional *SMBus v2.0* PEC generation and checking feature. This feature is required for the ARP process; however, it is optional for standard data transfer operation. The PEX 8747 supports PEC Cyclic Redundancy Check (CRC) generation and checking during ARP, as well as during Read/Write transfers to the PEX 8747 registers. The CRC polynomial used for PEC calculation is:

$$C(x) = x^8 + x^2 + x + 1$$

An 8-bit parallel CRC is implemented. The PEC calculation does not include ACK, NACK, START, STOP, nor repeated START bits. An SMBus Master can determine whether a Slave device supports PEC, from the UDID value returned by the Slave device, in response to a Get UDID command.

As a Slave device, the PEX 8747 checks the PEC, if the Master transmits the additional PEC byte and the PEX 8747 PEC checking feature is enabled (default). PEC checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Port 0, offset 2C8h[9]).

Additionally, when PEC is enabled, packets received with an incorrect PEC value are dropped. If PEC checking is disabled and a received PEC byte value is incorrect, the PEX 8747 accepts the packet. During a register Read, if the Master requests the additional PEC byte, the PEX 8747 generates and transmits the PEC byte after the register data.

7.3.6 Addressing PEX 8747 SMBus Slave

By default, the PEX 8747 supports ARP when *STRAP_I2C_SMBUS_EN*=1, and expects the ARP Master to define the PEX 8747 SMBus Device Address. If ARP is disabled (*STRAP_I2C_SMBUS_EN*=0, and the default **SMBus Configuration** register *ARP Disable* bit (Port 0, offset 2C8h[8]) is Set), the default **SMBus Configuration** register *SMBus Device Address* bits [7:1] are 0111_000b, 0111_001b, or 0111_010b, according to whether the *I2C_ADDR0* 3-state input is strapped Low (0), left floating (Z), or High (1), respectively (Address bits [7:1] are 0111_000b, with Address bit [1:0] values loaded from *I2C_ADDR0*). The input state allows a maximum of three PEX 8747 SMBus Slaves to co-exist without address conflict on the SMBus, using SMBus Address byte values of 70h, 72h, and 74h. The *I2C_ADDR0* 3-state input is loaded immediately after Fundamental Reset, and any subsequent change of input state does not affect functionality.

If the register's *UDID Address Type* field is programmed as fixed address (Port 0, offset 2C8h[13:12], are both Cleared) without disabling ARP, the PEX 8747 still participates in ARP, but does not Set the Device Address after ARP successfully completes.

The SMBus Slave Address can be changed at any time, by using software to write to the register's *SMBus Device Address* field (offset 2C8h[7:1]). ARP can also be enabled or disabled at runtime, by writing to the register's *ARP Disable* bit. If ARP is disabled by software after initially being enabled, the default address (70h) is not used for subsequent transactions. In this case, software must program a Device address into the *SMBus Device Address* field. When software writes the Device Address, it must also Set the register's *AR Flag* and *AV Flag* bits (offset 2C8h[11:10], respectively), to indicate that the address is valid and resolved.

Whenever software changes the register's *AV Flag*, *ARP Disable*, and/or *SMBus Device Address* values, software must also Set the register's *SMBus Parameter Reload* bit (offset 2C8h[15]). Writes to this register bit take effect only when the register's *SMBus Command In-Progress* bit (offset 2C8h[28]) is Cleared, which indicates that the PEX 8747 SMBus interface is in the Idle state.

7.3.7 SMBus Timeout

Unlike I²C, where the Slave or Master can indefinitely hold the [I2C_SCL0](#) line Low, SMBus has a timeout condition. No device is allowed to hold the I2C_SCL0 line Low for more than 25 ms. When the PEX 8747, as a Slave-Transmitter, detects that it has pulled the I2C_SCL0 line Low for more than 25 ms, the PEX 8747 releases I2C_SCL0, and the logic returns to its default state and waits for another START condition. This can also occur when the Master pulls the I2C_SCL0 line Low for more than 25 ms during any single Clock Low interval within a transfer in progress, or during the ACK phase if the Master pulls the I2C_SCL0 line Low to process a task. Generally, the PEX 8747 pulls the I2C_SCL0 line Low if SMBus access to registers is delayed by internal arbitration for register access.

7.4 Switching between SMBus and I²C Bus Protocols

The PEX 8747's I²C implementation allows switching between the SMBus and I²C protocols, by toggling the [SMBus Configuration](#) register *SMBus Enable* bit (Port 0, offset [2C8h\[0\]](#)).

When operating in SMBus mode, Clearing this bit, using the SMBus Block Write protocol, enables I²C protocol for subsequent register accesses. This SMBus Block Write can be transmitted from an SMBus or I²C Master, provided that the Block Write Byte sequence conforms to the sequence explained in [Section 7.3.3.1](#). In I²C mode, writing 1 to the *SMBus Enable* bit turns On the SMBus protocol, immediately after the Write operation is complete.



Chapter 8 Performance Features

8.1 Introduction

This chapter discusses guidelines for programming on-chip registers, to boost performance beyond that provided by the general-purpose default values, specifically:

- [DLLP Policies](#)
- [Latency](#)
- [Queuing Options](#)
- [Read Pacing](#)
- [Multicast](#)

8.2 DLLP Policies

Data Link Layer Packet (DLLP) rates can vary from 0 to 2 or more DLLPs/TLP. The PEX 8747 allows programming to affect the DLLP rate. An increase in DLLPs reduces the total TLP throughput. Therefore, for designs that require high performance, it would be beneficial to minimize DLLP rates. Transmitting fewer DLLPs, however, can result in credit starvation or Replay buffer overfill, which can have a detrimental effect on TLP bandwidth. Care must be taken when changing the default PEX 8747 DLLP transmission rate.

Typically, TLPs have higher transmission priority on the wire than DLLPs. The PEX 8747, however, allows DLLPs to have higher priority under certain conditions, meaning that DLLPs can transmit before starting a new TLP. The decision to transmit a DLLP ahead of a TLP is referred to as *DLLP policy*.

The PEX 8747 can be programmed to alter its default DLLP policies, to emphasize improved TLP throughput, faster acknowledgement, more credit, or simplest behavior. The PEX 8747 default policies are designed to achieve optimal performance for most applications. Programmable choices for a DLLP policy, however, allow for further optimization.

8.2.1 ACK DLLP Policy

An *ACK DLLP* is a response indicating to the TLP Transmitter that the Receiver received a “good” copy of the TLP, meaning that it acknowledged receipt of the TLP. The simplest policy is to send 1 ACK for every received TLP, resulting in a 1 DLLP/TLP rate for ACK alone. What an ACK means to the TLP Transmitter is that the TLP Transmitter can remove any stored copy of that TLP, because it is unnecessary to resend the TLP. ACK DLLPs can be combined, so that one ACK DLLP can serve to acknowledge multiple TLPs. This collapsing of ACKs is the basis of the ACK DLLP policy choices. Less-frequent, more-collapsed ACKs have the least impact on TLP transmit bandwidth, meaning that less-frequent ACKs result in less than 1 DLLP/TLP.

The PEX 8747 ACK policy consists of two parts – a Timer and TLP Counter. The default ACK Timer policy/value varies according to the negotiated Link width, operating Link speed, and Maximum Packet Size, as recommended in the *PCI Express Base r1.1*, *PCI Express Base r2.1*, or *PCI Express Base r3.0*.

The ACK Transmission Latency Timer loads the appropriate value when a TLP is received and known to be good, meaning a few clocks after the END framing symbol is received. The Timer counts down each symbol time (every 4 ns (*PCI Express Base r1.1*) or 2 ns (*PCI Express Base r2.1*)). When the Timer reaches 0, an ACK DLLP takes higher priority over new TLPs (*that is*, an ACK DLLP is transmitted before a new TLP is started). The ACK DLLP transmitted acknowledges all TLPs, up to the most recently arrived good TLP.

The TLP Counter counts down on each TLP arrival until it reaches 0, then schedules a high-priority ACK DLLP. The default initialization value for the TLP Counter is 16, meaning a high-priority ACK is scheduled upon the arrival of 16 TLPs. The **Ingress Port-Based Control** register *ACK TLP Counter Timeout* field (All Ports, offset F48h[1:0]) value controls the ACK TLP Counter, as follows:

- 00b – Allows 16 TLPs before a high-priority ACK (default)
- 01b – Allows 8 TLPs before a high-priority ACK
- 10b – Allows 4 TLPs before a high-priority ACK
- 11b – Disables the Counter

Either the Latency Timer or TLP Counter mechanism can cause a high-priority ACK DLLP to be scheduled, and the first one to do so re-initializes both mechanisms to their starting parameters. *For example*, the time for 16 TLPs can be less than the ACK Timer above, in which case an ACK is sent earlier. The TLP Counter is useful for any system with a large programmed MPS (resulting in a large Timer value), that is capable of sending short TLPs (*such as* 12-byte Memory Reads). Rather than require the Transmitter to save possibly 100+ small TLPs, it need only save 16, plus whatever else arrives during the round-trip time.

If there is no TLP traffic being transmitted (*that is*, the Transmit Link is idle), an ACK DLLP can be transmitted immediately, before the Latency Timer expires. This is an opportunistic, low-priority ACK because it does not contend with a TLP in transmission. When an opportunistic, low-priority ACK is transmitted, both the Latency Timer and TLP Counter re-initialize, waiting for a new TLP to arrive to begin counting again.

The PEX 8747 allows a programmable override of the default Ack_Latency_Timer value, on a per-Port basis, by programming the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset FA8h[11:0]). The value in this register is loaded when a new TLP arrives and a high-priority ACK DLLP is attempted when the Timer reaches 0. For fastest ACK response, this Timer can be programmed to 000h, resulting in one DLLP ACK transmitted immediately per each TLP received. For less impact on Transmit TLP bandwidth, a larger value can be programmed, resulting in less-frequent ACKs.

In general, a slower ACK response does not impact the Receive TLP stream, and aids the TLP Transmit stream. Every PCI Express device contains storage (Retry buffer) for storing TLPs while waiting for ACKs. The amount of Retry buffer storage a device contains is vendor-dependent. The quantity of TLPs the PEX 8747 can store depends upon the type and size of TLPs received. The PEX 8747 holds TLPs in the Retry buffer while waiting for an ACK. At some point, if the Retry buffer storage fills, no new TLPs can be sent until a new received ACK frees up space. In this case, the ACK can become a performance bottleneck.

8.2.2 UpdateFC DLLP Policy

An *UpdateFC DLLP* is transmitted in response to a received TLP. The UpdateFC DLLP replenishes the connected device with additional credit, to allow the Transmitter to transmit more TLPs of that type. Each TLP that arrives consumes credit, and eventually, a stream of TLPs consume all the available credit, unless an UpdateFC DLLP provides additional credit. However, if the connected device has sufficient credit to transmit more TLPs, it is not necessary to transmit UpdateFC DLLPs to it. The UpdateFC policy determines how and when to transmit an UpdateFC DLLP.

There are two parts to the UpdateFC policy – frequency of transmitting the updates and credit amount. This section discusses only the frequency.

If the PEX 8747 is not transmitting TLPs (*that is*, the Transmit Link is idle), and credit to replenish the credit used becomes available, the PEX 8747 immediately transmits an UpdateFC DLLP to the connected device. This is an opportunistic, low-priority UpdateFC DLLP.

However, if the PEX 8747 is busy transmitting TLPs to the connected device, the PEX 8747 does not transmit an UpdateFC DLLP until a programmed threshold is crossed. The PEX 8747 provides four threshold options – 100%, 75% (default), 50%, and 25%. Whenever the remaining credit drops below the programmed threshold, an UpdateFC DLLP is given high priority, meaning that the UpdateFC DLLP is transmitted before a new TLP is started. There is a separate threshold for Header and Payload credits, for each TLP type – Posted, Non-Posted, and Completion – located in the **Ingress Credit Handler (INCH) Threshold** registers (Port 0, offsets [A00h](#) through [A08h](#)).

8.2.3 Unidirectional DLLP Policies

For unidirectional traffic, the PEX 8747 DLLP policies allow the most-frequent DLLPs, because DLLPs do not interfere with TLPs. (DLLPs flow in the opposite direction of TLPs.)

The PEX 8747 can transmit a DLLP ACK almost immediately upon receiving and verifying a TLP. A faster ACK results in fast Transmitter de-allocation of the TLP, and can therefore allow a shallow TLP Replay buffer. The default values can be overwritten, to increase or decrease the ACK DLLP rate. For unidirectional traffic, a small number, *such as* 1, is recommended.

The number programmed into the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset [FA8h](#)[11:0]) Sets the ACK Transmission Latency Timer, to count the quantity of symbol times after receiving a TLP, before transmitting an ACK.

Similar to the ACK programmability, the PEX 8747 can immediately transmit an UpdateFC after receiving only the TLP Header. By transmitting an UpdateFC earlier, the total credit advertised can be minimized. By programming fewer credits and having a fast UpdateFC policy, the system does not run out of credits and the PEX 8747 does not waste Buffer space on reservations that do not arrive. The following are the recommended Settings:

- Set the UpdateFC policy for unidirectional traffic to 100%
- Set the credits to be sufficient to allow 3 to 4 TLPs

8.3 Latency

Latency is the length of time it takes to proceed from one event to another. Latency can be measured in several different ways, but perhaps the most common measurement for a switch is *Start TLP-to-Start TLP (STP-to-STP) latency*. Figure 8-1 illustrates an STP-to-STP Latency Measurement. When the Egress Start TLP symbol is transmitted out of a switch before the Ingress Port End symbol arrives, the transfer is termed *Cut-Thru*. If an Egress Port queue is not already established, the PEX 8747 always cuts the packet through. The PEX 8747 has the same latency, regardless of whether the traffic is Upstream or peer-to-peer.

As expected with the PEX 8747 Cut-Thru architecture, STP-to-STP latency is basically constant for all Payload sizes. A faster Link can receive the Header for decode faster, with a slightly lower latency. There will generally be a constant latency for any ingress width to the same egress width, or any ingress width to a smaller egress width, operating at the same Link speed.

For cases in which the egress Port has a higher bandwidth than the ingress Port, then a fraction of the packet, given by the following formula:

$$F = (E - I) / E$$

must be buffered (to prevent under-run in the middle of the TLP), before the TLP can be forwarded to the egress Link.

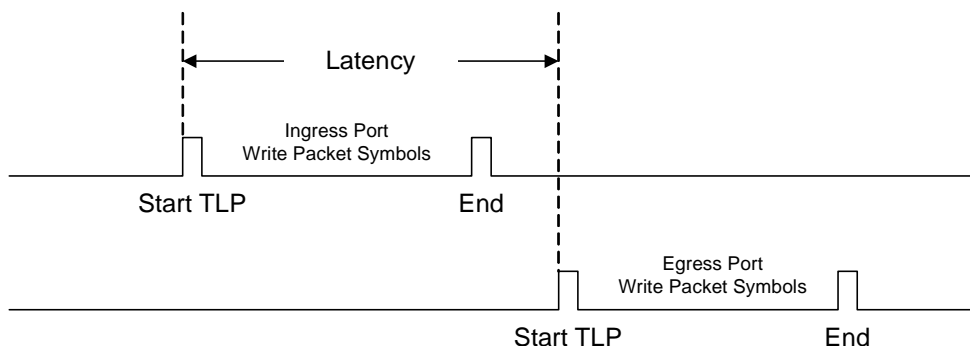
where

- F is the fraction sum
- E is egress bandwidth
- I is ingress bandwidth

For example, with an ingress x4 Port and egress x16 Port, $(16 - 4) / 16 = 3/4$ of the packet must be buffered before it can be forwarded. Moving in the opposite direction, with an ingress x16 Port and egress x4 Port, the ingress Port has more bandwidth than the egress Port; therefore, buffering is not needed, and the packet can immediately be cut through.

Latency is often important when a Downstream device is reading Main memory, Upstream, because the reader has a finite number of Reads that it can send. Often in this case, the Upstream Port is wider than the Downstream Port and, as a result, latency through the PEX 8747 is optimal in both directions. The Memory Read Request (MRd) that is transmitting Upstream is quite short (12 to 20 bytes); therefore, the buffering required for going from narrower to wider Link widths does not significantly increase latency. The resultant Completion with Data (CplD), with a Payload returning Downstream, is a significantly larger packet; however, the wider to narrower Link width rule applies, and therefore no buffering is needed before forwarding the packet.

Figure 8-1. Start TLP-to-Start TLP Latency Measurement



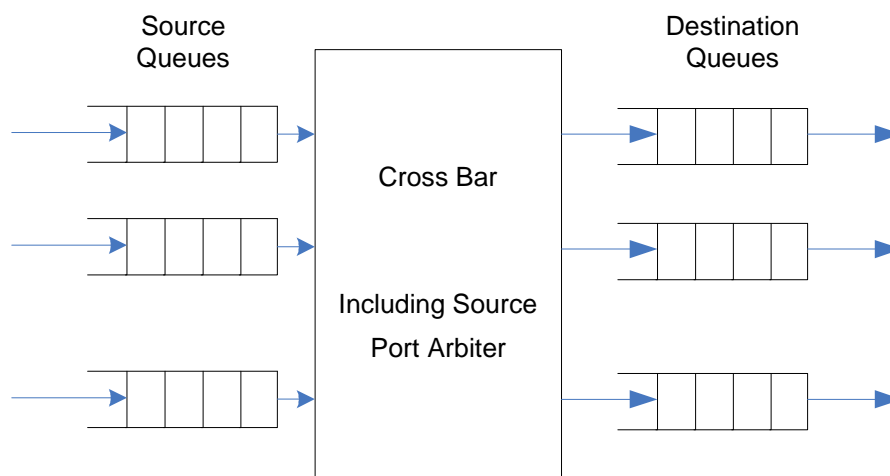
8.4 Queuing Options

On-chip queuing does not exist in balanced bandwidth scenarios, where the total ingress bandwidth is less than or equal to the egress bandwidth. In the common case, where the total ingress bandwidth is greater than the egress bandwidth, queues develop on the PEX 8747. The PEX 8747 provides two alternatives, as to where to locate such queuing (refer to [Figure 8-2](#)):

- **Destination queue** – Associated with a single destination Port. All the TLPs in a Destination queue will egress out the same Port.
- **Source queue** – Associated with a single ingress Port. All the TLPs in a Source queue come from the same Port.

Each queue is discussed in the sections that follow.

Figure 8-2. On-Chip Queuing



8.4.1 Destination Queuing

Note: For the queuing examples provided in this section, “Port 1” indicates “first Port,” not the Port physically identified as Port 1.

The default behavior is for all queues to develop at the destination Port. If TLPs are arriving from four sources to a common destination Port, the TLPs are scheduled according to First-In, First-Out (FIFO). The crossbar can forward a TLP every 4 ns, to each Destination queue; therefore, it is unlikely that a Source queue can develop or last very long.

A Destination queue develops whenever the *ingress rate* – the sum of all ingress Ports targeting a destination Port – exceeds the egress rate. A Destination queue might also develop in a credit-starved situation, where there is no credit available to forward TLPs.

For example, if TLPs arriving from four sources all go to a common destination Port, the TLPs are scheduled, based upon the order in which they arrive at the Destination queue FIFO^a. If all four flows are equally active, the TLPs naturally interleave as 1,2,3,4,1,2,3,4. If three of the Ports, however, have a head start before the fourth Port turns On, the output can be 1,2,3,1,2,3,1,2,3,1,2,3,1,2,3,4,1,2,3,4. In this case, all the new Port (Port 4) TLPs must wait for the earlier Port 1,2,3 traffic to be transferred before the Port 4 TLPs can be transferred. Therefore, the latency for Port 4 traffic to travel through the PEX 8747 can widely vary, based upon the traffic passing through the switch.

a. Conventional PCI Strong Ordering rules can override the FIFO. Conventional PCI requires Posted TLPs to be able to pass Non-Posted and Completion TLPs, to avoid deadlock.

8.4.2 Source Queuing

Caution: *Source Queuing and [Read Pacing](#) should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.*

Note: *For the queuing examples provided in this section, “Port 1” indicates “first Port,” not the Port physically identified as Port 1.*

Source queuing can be enabled for applications that require deterministic bounded latency for traffic that flows to a single Port.

Source queuing limits the Destination queue depth by applying an upper and lower threshold. When the Destination queue reaches the programmed upper threshold, any subsequent TLPs targeting that destination Port are not forwarded, but instead are queued up in a per-Source Port-based queue. The Source Port queue does not begin to forward TLPs again (to any Port), until its first entry’s destination Port’s queue drops to a programmed lower threshold.

Note: *A Source Port queue that cannot forward to a Destination queue blocks all subsequent TLPs arriving on that same Source Port, even if those subsequent TLPs target different destination Ports.*

The **Port Egress TLP Threshold** register (offset [F38h](#)) controls the upper and lower queue thresholds. [Table 8-1](#) summarizes the register bit Settings. The Port Lower TLP Counter is the quantity of TLPs that the Destination queue must reach after becoming saturated, before re-enabling TLP forwarding. The Port Upper TLP Counter is the quantity of TLPs that can be queued in the Destination queue.

In the Destination queue example provided in [Section 8.4.1](#), the early arriving Port 1,2,3 TLPs stalled Port 4’s TLP for an indeterminate length of time. By programming, with source queuing enabled and a Destination Port Lower TLP Counter programmed to 1 and Port Upper TLP Counter programmed to 3 (TLPs), the worst case is that Port 4 must wait for three TLPs (1,2,3) before getting its first turn. With these Settings, the example TLP output would be 1,2,3,4,1,2,3,4,1,2,3,4. The *turn to be forwarded* refers to a Port Arbitration wait, described in [Section 8.4.3](#).

To avoid unnecessary idles on the destination Link, program a Port Lower TLP Counter of 1, and a Port Upper TLP Counter of 2.

Table 8-1. Port Egress TLP Threshold Register Port Lower and Upper TLP Counters (Offset F38h)

Bit(s) ^a	Name	Description
11:0	Port Lower TLP Counter	When Source Scheduling is disabled due to Threshold, it is re-enabled when the Port TLP Counter goes below this Threshold value.
27:16	Port Upper TLP Counter	When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP scheduling to this egress Port.

a. Bits not identified in [Table 8-1](#) are **Reserved**.

8.4.3 Port Arbitration

Port Arbitration refers to the arbitration at an egress Port of a switch between other ingress Ports. In the PEX 8747, a different Port Arbiter connects all the Source queues to each Destination queue. The PEX 8747 supports, on a per-Port basis, either a hardware-fixed Round-Robin (RR) arbitration scheme or a 64-slot Weighted Round Robin (WRR) arbitration scheme, the assignment of which is a bit complicated and will be discussed at the end of this section.

The Port Arbiter has the most effect when source queuing is enabled (refer to [Section 8.4.2](#) for details), and TLPs from multiple ingress Ports are enqueued such that the Port Arbiter has choices about which TLP to forward. Every egress Port has its own independent Port Arbiter state machine.

Port arbitration in the PEX 8747 makes decisions on a per-TLP basis. As a consequence, the throughput may not look fair for two otherwise equal Ports if the average TLP size of each is different. *For example*, if two ingress Ports, PortA and PortB, target the same egress Port and both have the same weight, but PortA has short TLPs while PortB has long TLPs, PortB will appear to get a higher throughput. The seeming unfairness can be compensated for, by using the WRR Arbiter, and by adjusting the weights of the Ports to be in a ratio similar to the ratio of TLP size.

The RR Port Arbiter scheme decides which ingress Port to forward to a single egress Port, with all ingress Ports having the same weight. All Downstream Ports, by default, use an RR Port Arbiter.

The WRR Port Arbiter scheme also decides which ingress Port to forward to a single egress Port; however, the ingress Ports may have different weights. The initial weights are based upon the negotiated Link width. With 64 slots, the resolution of the weights goes down to a x1 Gen 3 Link (8 GT/s). Therefore, a x1 Gen 3 Link would have 1 slot, while a x8 Gen 3 Link would have 8 slots, and so forth. A x4 Gen 1 Link, x2 Gen 2 Link, and x1 Gen 3 Link all have the same weight, because each has the same throughput capability of approximately 8 GT/s.

Software can change the default WRR weights to any value. The WRR Port Arbiter uses the *PCI Express Base r3.0*-defined Port Arbitration Capability structure, as reflected in the Port's **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[2:0]), with the Port's **VC0 Resource Control** register *Port Arbitration Select* field (offset 15Ch[19:17]) programmed to 010b.

Software performs two steps to change the WRR weights.

In the first step, the weights are programmed in the **Port Arbitration Table Phase x** registers (offsets 178h through 1B4h). (Refer to the *PCI Express Base r3.0*, as well as [Section 11.15.1](#), “WRR Port Arbitration Table Registers (Offsets 178h – 1BCh),” for further details.)

The final step requires a write to the Port's **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]). When written, the weights programmed in the **Port Arbitration Table Phase x** registers in the first step are transferred to the WRR arbitration logic and take effect. Before writing the *Load Port Arbitration Table* bit, the **Port Arbitration Table Phase x** registers have no effect.

The selection of which egress Port gets a WRR Port Arbiter is limited, due to hardware constraints. The main constraint is that only one Port of a Port group can use the WRR. The Port groups are as follows:

- Group 0: Port 0
- Group 2: Port 8
- Group 3: Port 9
- Group 4: Port 16
- Group 5: Port 17

Each Port group has one WRR that is always enabled. As previously mentioned, the WRR defaults to weights based upon the negotiated Link width of each ingress Port.

8.4.4 Port Bandwidth Allocation

For applications that need to allocate a fixed bandwidth to each Port, the PEX 8747 can help enforce the relative bandwidth ratio between Ports in a congested scenario.

By combining source queuing, Port Arbitration, and initial credit, as well as some knowledge of average Payload size, many combinations of Port bandwidth allocation are possible.

8.5 Read Pacing

Note: Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.

The Read Pacing feature is supported on all Ports. The Read Pacing Configuration registers, however, are implemented as follows – Port 0, 8, or 16.

PCI Express has a weakness concerning the number of outstanding bytes requested by Reads. It is possible that a single device can overwhelm the system with a relatively small number of large Read Requests, thereby impacting the performance of other connected devices, by filling the ingress transaction queue in the Root Complex.

The Root Complex must handle the transactions in the order in which they are posted. Transactions posted from less aggressive reading devices, which may be more sensitive to latency, suffer performance reductions due to the unfairly weighted path (head of line blocking) in the transaction queue that the large reads represent.

Read Pacing attempts to apply some rules to Memory Read Requests, so that no one Port can overwhelm a system. There are two aspects to the PEX 8747's Read Pacing capability:

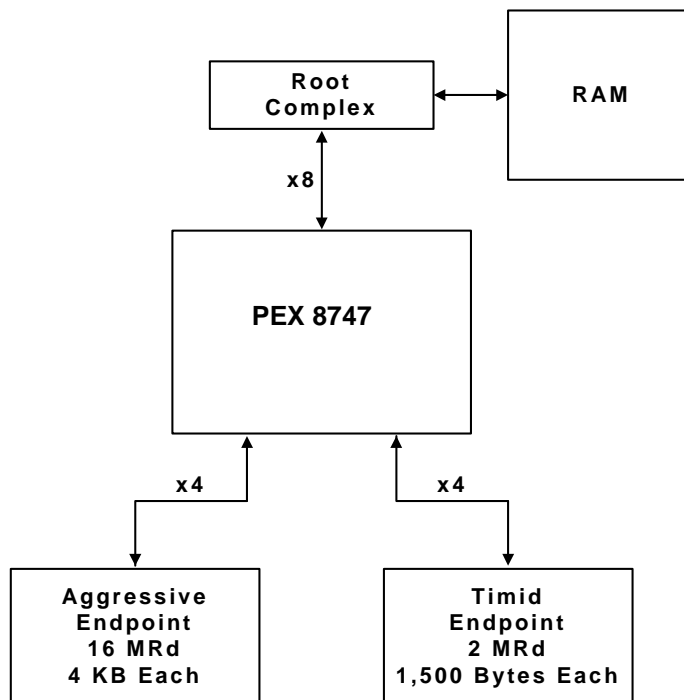
- Read spacing
- Read threshold

The following sections provide examples and further information regarding Read Pacing.

8.5.1 Read Pacing Example

Figure 8-3 illustrates an example of a system that benefits from Read Pacing.

Figure 8-3. Read Pacing Example



In a typical Host-centric application, endpoints have Direct Memory Access (DMA) engines that write to and read from Main memory. A performance bottleneck can occur during the Read to Main memory, through the Root Complex. For the example illustrated in [Figure 8-3](#), the aggressive endpoint sends many large (16, 4-KB) Memory Read Requests, while another endpoint, or Timid Endpoint (TEP), sends only two 1,500-byte Memory Read Requests. The TEP then waits for a response before sending additional Read Requests^a.

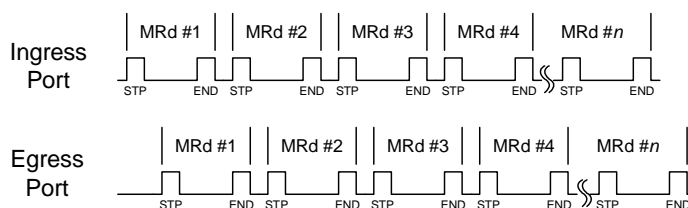
If either endpoint is running by itself, neither sees a problem. However, if both endpoints are concurrently active, the aggressive endpoint dominates the Root Complex Memory Controller. In addition, due to the bandwidth mismatch, Completions can queue up in the PEX 8747, creating too many Completions for the switch to store at one time. As a result, the PEX 8747 backpressures the Root Complex for Completions. The Root Complex can only forward Completions to the PEX 8747 at the aggressive endpoint's rate, which is significantly less than the Root Complex could otherwise handle.

The net impact is not to the aggressive endpoint, because there are a sufficient number of Completions queued up in the PEX 8747 to keep it busy. In fact, the aggressive endpoint experiences better performance with a switch, than connected directly to the Root Complex^b. Rather, the TEP experiences lower performance results. Its Memory Read Requests wait in line behind multiple aggressive endpoint Requests, and the Root Complex can drain Requests only at the same rate of the PEX 8747, not at the Upstream Link's capacity.

[Figure 8-4](#) illustrates how a PCI Express switch, without Read Pacing, forwards MRds.

Read Pacing solves the performance loss seen by the TEP, while improving the aggressive endpoint's performance. The following sections provide examples of the way in which the PEX 8747 functions when Read Pacing is enabled, and Read Spreading is enabled or disabled.

Figure 8-4. Read Pacing Off (Disabled)



a. This is based upon an actual setup in a third-party lab. Fibre Channel endpoints can easily send 16, 4-KB MRd at a time, while Gigabit Ethernet endpoints might send only one or two 1,500-byte endpoints at a time.

b. Without a switch, when the Root Complex has something else to do, the aggressive endpoint loses its data stream. With a switch, the buffering of multiple Completions hides the fact that the Root Complex is multitasking.

8.5.2 Read Spacing (Spreading) Logic

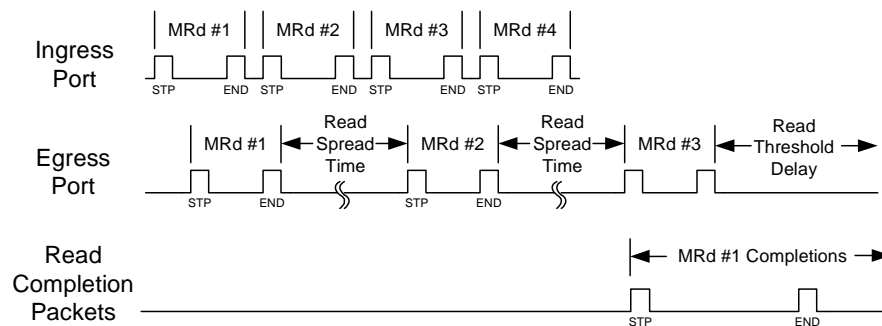
Read Spacing (also referred to as *Read Spreading*) spreads out Read Requests. The PEX 8747 Read Spacing logic looks at the Read Request size and the endpoint's bandwidth, to determine how often to forward subsequent Read Requests. *For example*, Read Requests arriving on a x4 Link can only sink data at a x4 rate. If a x4 endpoint submits multiple Read Requests to a x8 Link, the Read Spacing logic does not forward the subsequent Read Requests until the endpoint has sufficient time to sink a portion of the Completion data from the previous Read Requests.

Initially, a queue of Completions must build up to hide the time that it takes for the data to return. As a result, Reads are forwarded at 2x the endpoint's bandwidth. This 2x rate is maintained until a threshold of outstanding Read data is reached, at which time Reads are forwarded at 1x the endpoint's bandwidth.

Read Pacing must be enabled for Read Spreading to be enabled. That is, for a Port to have Read Spreading enabled, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* and *Port x Memory Read Spreading Disable* bits (Port 0, 8, or 16, offset 1D0h[0 and 16], respectively) must both be Cleared.

Figure 8-5 illustrates the way in which the PEX 8747 forwards Read Requests when the Read Pacing- and Read Spreading-related bits are enabled. (Refer to Section 8.5.5 for additional register/bit information.) The PEX 8747 continues to spread and forward the Read Requests, until the amount of Completion data for which it is waiting exceeds the value programmed in the **Read Pacing Threshold x** register(s) for that Link width (Port 0, 8, or 16, offsets 1D4h and 1D8h).

Figure 8-5. Read Pacing On (Enabled) and Read Spreading On (Enabled)

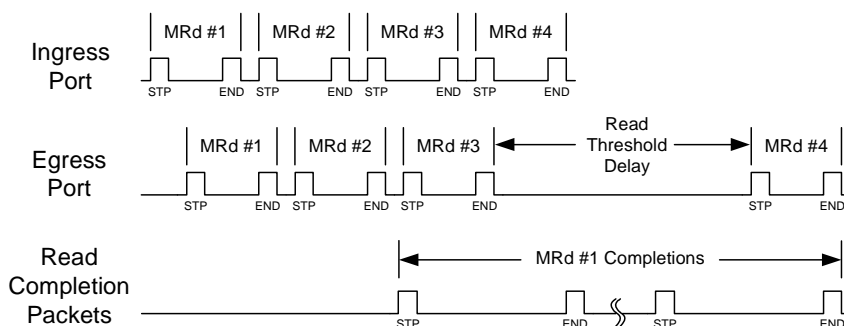


8.5.3 Read Threshold

The Read threshold is the maximum number of outstanding DWords (1 DWord = 4 bytes) that the endpoint Port requested to be read, but were not yet returned as Completion data. The threshold is related to the PEX 8747's buffering capacity – all outstanding Read data ought to be able to be buffered in the switch, to remain out of the way of other Completions for other endpoint's Read Requests.

After a Port reaches its Read threshold, subsequent Read Requests from that Port queue up in the PEX 8747, waiting for Completion data to reduce the outstanding count to below the threshold. If an overabundant number of Read Requests queue in the PEX 8747, no additional Read credit is allocated, which backpressures the Read Requester. Figure 8-6 illustrates the way in which the PEX 8747 forwards Read Requests when its Read Spacing logic is enabled and Read Spreading logic is disabled.

Figure 8-6. Read Pacing On (Enabled) and Read Spreading Off (Disabled)



8.5.4 Read Pacing Benefits

When Read Pacing logic is enabled, the PEX 8747 provides the follow benefits:

- Maximum Read latency that an endpoint may experience can be dramatically reduced.
By reducing the amount of queued Read Requests, and therefore pending Read Completion data at the Root Complex, new Read Requests from Ports that do not have pending Read Requests can be serviced with a predictable and/or reasonable amount of latency.
- Timid endpoint bandwidth is dramatically increased in busy applications.
Because queues of pending Read Requests in the Root Complex are limited, and congestion caused by a large amount of Completion data intended for a high-bandwidth, needy Port (or Ports) is avoided, the bandwidth needs of endpoints with smaller bandwidth requirements are met (*that is*, the endpoints are not starved).
- PEX 8747's Read Pacing Threshold logic allows all busy Ports to be equally serviced in congested scenarios, regardless of their individual Read requesting behavior.

For example, all Ports might simultaneously request data, some aggressively and some timidly. While unable to quickly drain their queued Completions, the Ports' Read Pacing Threshold logic forwards the additional Read Requests to the Root Complex, equally and fairly, while ensuring Completion data is available for each Port, when the Port is ready to accept it.

8.5.5 Enabling Read Pacing and Read Spreading

Read Pacing is disabled, by default. To enable Read Pacing, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* bit (Port 0, 8, or 16, offset 1D0h[0]) must be Cleared. A value of 0 enables Read Pacing, whereas a value of 1 (default) disables Read Pacing.

The Port's **Read Pacing Control** register *Port x Memory Read Spreading Disable* bit (Port 0, 8, or 16, offset 1D0h[16]) is used to enable or disable Read Spreading. A value of 1 disables Read Spreading. Read Spreading is enabled, by default (value of 0); however, it is overridden by the Port's *Port x Read Pacing Disable* bit, by default.

Both sets of Read Spreading and Pacing Control register bits are represented in Table 8-2. (For complete details, refer to the register offset 1D0h description provided in Section 11.16.1, "Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h).") Figure 8-4 through Figure 8-6 illustrate what occurs when the bits are enabled or disabled.

The Read Pacing thresholds are Set, based upon the Source Port's programmed Link width. The **Read Pacing Threshold 1** register controls the threshold values for x16 and x8 Link width threshold values, and the **Read Pacing Threshold 2** register controls the x4 and x2 Link width threshold values (Port 0, 8, or 16, offsets 1D4h and 1D8h, respectively). The thresholds are in DWords. Narrower Link widths have lower thresholds, because they must buffer smaller quantities.

Table 8-2. Read Pacing Control Register Read Pacing- and Memory Read Spreading Disable Bits (Offset 1D0h) (Ports 0, 8, and 16)

Bit(s)	Description	Default
0	Port x Read Pacing Disable 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	1
16	Port x Memory Read Spreading Disable 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	0

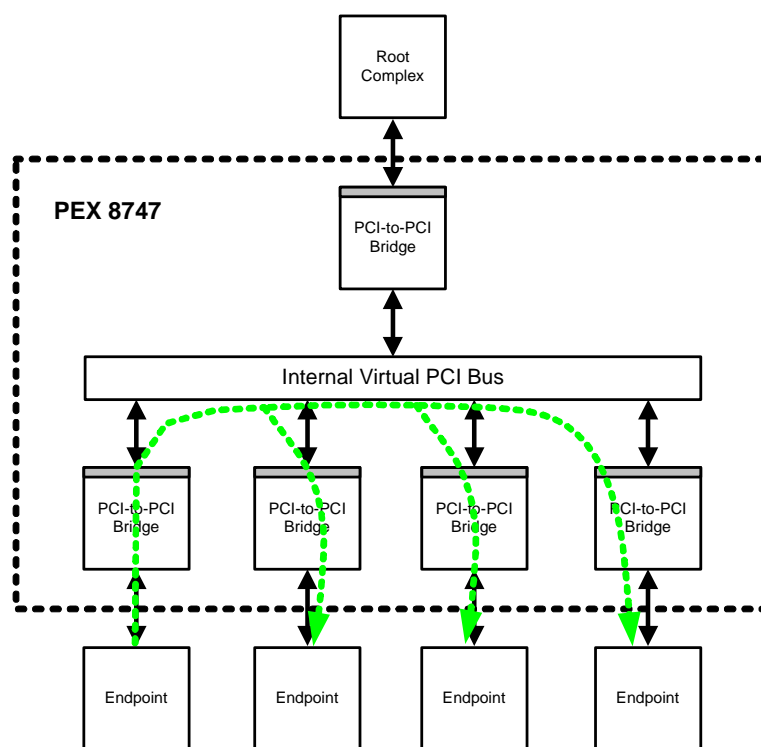
8.6 Multicast

This section describes the functions and registers of the Multicast (MC) feature.

Multicast allows software to concurrently write the same data to a group of multiple destinations. When a Posted Memory Write TLP entering the PEX 8747 is addressed to the MC Address Range (*MC BARs*), and Multicast is enabled, the PEX 8747 automatically generates and transmits a copy of the original TLP (referred to as the *MC Copy TLP*) to one or more destination Port(s). The MC Address Space is divided into *MC Groups (MCG)*, defined by using *MC Base Address* and *MC Index Position*. Each PEX 8747 Port can elect to receive an MC Copy TLP by belonging to an *MCG*, by Setting the corresponding *MC Receive* bit. An MC TLP can be blocked by using *MC Block All*, if required. *MC Overlay Bar* can be used to replace the original MC TLP's address to a Unicast address space, if the endpoint does not support MC.

Figure 8-7 illustrates an example of a Multicast operation on a peer-to-peer Write Request. An endpoint's Write Request is transmitted as copies to additional peer destination endpoints.

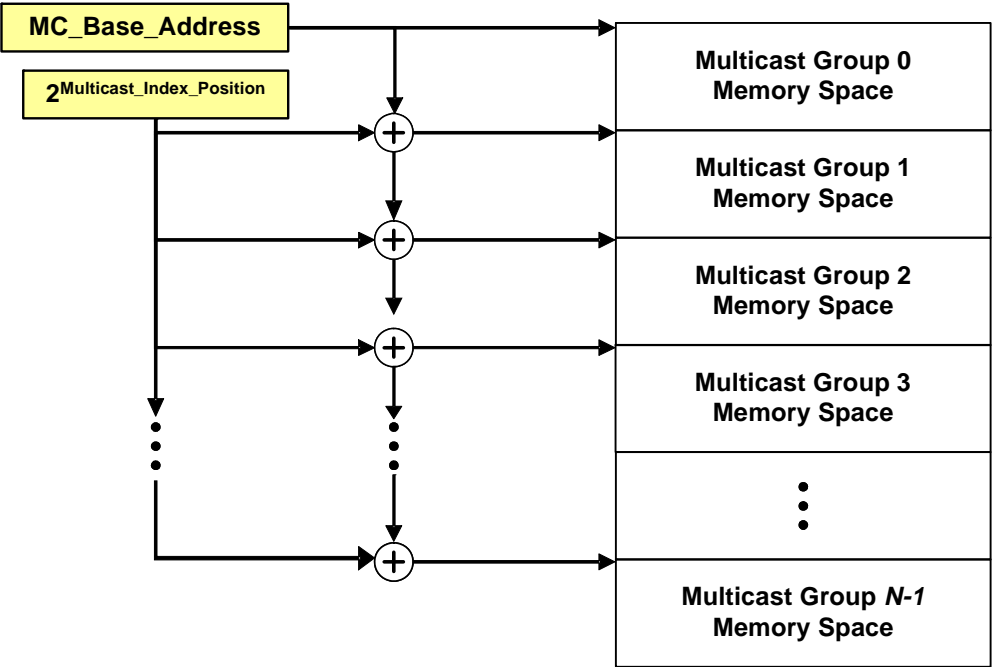
Figure 8-7. Peer-to-Peer Multicast



8.6.1 Multicast Address Range Segmentation

The **Multicast Extended Capability** structure defines an MC Address range, the segmentation of that range into a number, *N*, of equally sized MC windows, and the association of each MC window with an MCG, as illustrated in Figure 8-8. Each function that supports MC within a component implements a **Multicast Extended Capability** structure that provides routing directions and permission checking for each MCG for TLPs that pass through. The MCG is a field of up to 6 bits in width, which is embedded in the address, beginning at the MC_Index_Position.

Figure 8-8. Multicast Address Range Segmentation



8.6.2 Multicast TLP Processing

A TLP is processed as an MC TLP if an MC Hit occurs when all of the following conditions are true:

- MC_Enable is Set
- TLP is a Memory Write (Posted Request)
- TLP Address \geq MC_Base_Address
- TLP Address $< (MC_Base_Address + (MC_Index_Position^2) \times (MC_Num_Group + 1))$

While processing the TLP, each PEX 8747 ingress Port uses values of MC_Enable, MC_Base_Address, MC_Index_Position, and MC_Num_Group from its registers. The software is required to identically configure all these fields in all Ports. If this is not the case, results are indeterminate.

If an MC Hit occurs, standard address routing rules do not apply. Instead, the TLP is processed by first extracting the MCG from the address in the TLP, using the ingress Port's values for MC_Base_Address and MC_Index_Position. Specifically:

$$MCG = ((Address_{TLP} - MC_Base_Address) \gg MC_Index_Position) \& 3Fh$$

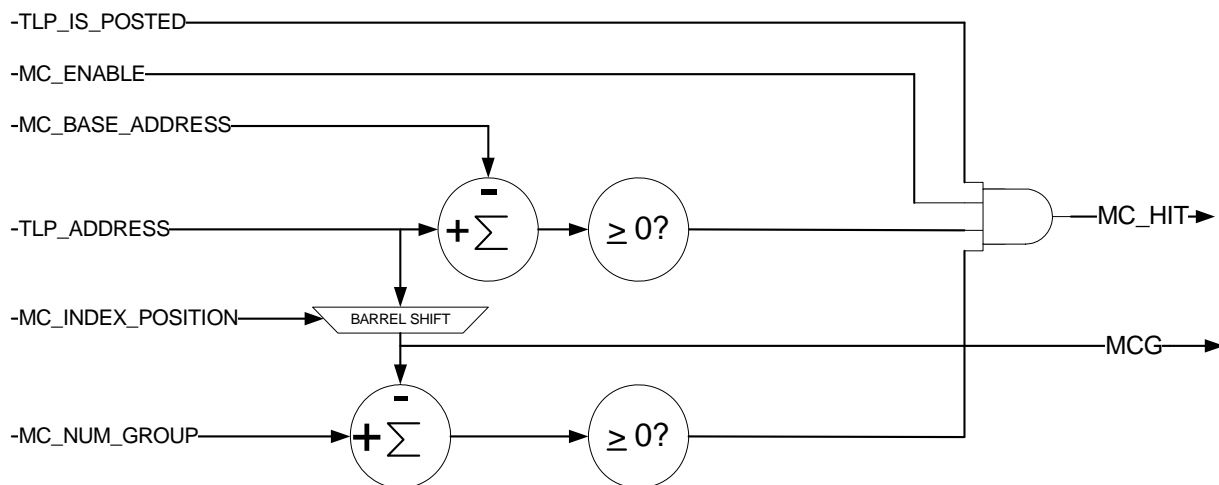
Next, the PEX 8747 checks the MC_Block_All and MC_Block_Untranslated bits corresponding to the extracted MCG, using the MC_Block_All and MC_Block_Untranslated registers associated with the ingress Port. If the MC_Block_All bit corresponding to the extracted MCG is Set, the TLP is handled as an MC Blocked TLP. If the MC_Block_Untranslated bit corresponding to the extracted MCG is Set, and the TLP contains an Untranslated Address, the TLP is also handled as an MC Blocked TLP.

If the TLP is not blocked in the PEX 8747, it is forwarded out of all the Ports, with the exception of its ingress Port, whose MC_Receive bit corresponding to the extracted MCG is Set. If no Ports forward the TLP, the TLP is silently dropped.

Figure 8-9 illustrates Multicast processes TLPs.

Note: To prevent loops, it is prohibited for a PEX 8747 Port to forward a TLP back out through its ingress Port, regardless of whether it is specified to do so, by the Port's MC_Receive register.

Figure 8-9. Multicast TLP Processing



An MC Hit suspends standard address routing, including default Upstream routing in the PEX 8747. When an MC Hit occurs, the TLP is forwarded out only through those egress Ports whose *MC_Receive* bit associated with the MCG extracted from the address in the TLP is Set. The PEX 8747 attempts to simultaneously broadcast the packets. However, if the Egress queues are not empty, the packet remains queued for each egress Port, because ordering must be maintained. Therefore, the MC packets could be transmitted at different times, depending upon the traffic flow.

If the address in the TLP does not decode to a Downstream Port using standard address decode, the TLP is copied to the Upstream Port, if specified to do so, by the Upstream Port's **MC_Receive** register.

If the address in a Non-Posted Memory Request hits in an MC window, no MC Hit occurs, and the TLP is processed as a Unicast.

If an MC Hit occurs, the only ACS access control that can apply is ACS Source Validation. In particular, neither ACS redirection nor the ACS Egress Control Vector affects operations during an MC Hit.

8.6.3 Multicast Ordering

No new ordering rules are defined for processing MC TLPs. All MC TLPs are Posted Requests and follow Posted Request ordering rules. MC TLPs are ordered per standard ordering rules, relative to other TLPs in a component's ingress stream, through the point of replication. Once copied into an egress stream, an MC TLP follows the same ordering as other Posted Requests in the stream.

8.6.4 Multicast Extended Capability Structure Field Updates

Certain fields of the **Multicast Extended Capability** structure can be changed at any time. Others cannot be changed with predictable results, unless the *MC_Enable* bit is Cleared in every component function. The latter group includes *MC_Base_Address* and *MC_Index_Position*. Fields that software can change at any time include *MC_Enable*, *MC_Num_Group*, *MC_Receive*, *MC_Block_All*, and *MC_Block_Untranslated*. Updates to these fields must be ordered.

For example, TLPs *A* and *B* arrive in that order, at the same ingress Port, and in the same TC. If *A* uses *X* for one of these fields, then *B* must use the same value or a newer value.

8.6.5 MC Blocked TLP Processing

When a TLP is blocked by the *MC_Block_All* or *MC_Block_Untranslated* mechanisms, the TLP is dropped. The ingress Port blocking the TLP serves as the Completer. The ingress Port logs and signals this MC Blocked TLP. In addition, the ingress Port Sets the **PCI Status** register *Signaled Target Abort* bit (offset 04h[27]) or **Secondary Status** register *Signaled Target Abort* bit (offset 1Ch[27]), as appropriate. If the error occurs with a TLP received by an ingress Port, the error is reported by that ingress Port.

8.6.6 MC_Overlay and ECRC Re-Generation

The MC Overlay mechanism is provided to allow a single BAR in an endpoint that does not contain a **Multicast Extended Capability** structure to be used for both MC and Unicast TLP reception. Software can configure the MC_Overlay mechanism to affect this, by Setting the MC_Overlay_BAR in a Downstream Port of the PEX 8747, so that the MC Address range, or a portion thereof, is re-mapped (overlaid) onto the Memory Space range accepted by the endpoint's BAR. At the Upstream Port, the mechanism can be used to overlay a portion of the MC Address range onto a Memory Space range associated with Host memory.

When enabled, the overlay operation specifies that MC TLP Address bits, whose bit numbers are greater than or equal to the MC_Overlay_Size field, be replaced by the corresponding MC_Overlay_BAR bits.

That is:

```

If (MC_Overlay_Size = 0)
Then:
    Egress_TLP_Addr = Ingress_TLP_Addr;
Otherwise:
    Egress_TLP_Addr =
        {MC_Overlay_BAR[63:MC_Overlay_Size], Ingress_TLP_Addr[MC_Overlay_Size-1:0]};

```

If the TLP with the modified address contains the optional ECRC, the unmodified ECRC will almost certainly indicate an error. The action to be taken if a TLP containing an ECRC is MC copied to an egress Port that has MC_Overlay enabled, are outlined in [Table 8-3](#). If MC_Overlay is not enabled, the TLP is forwarded, unmodified. If MC_Overlay is enabled and the TLP has no ECRC, the modified TLP, with its address replaced as specified in the previous paragraph, is forwarded. If the TLP has an ECRC but ECRC re-generation is not enabled, then the modified TLP is forwarded with its ECRC dropped and the *TD* bit in the header Cleared, to indicate that no ECRC is attached. If the TLP has an ECRC and ECRC re-generation is enabled, an ECRC is performed before the TLP is forwarded. If the ECRC passes, the TLP is forwarded with a re-generated ECRC. If the ECRC check fails, the TLP is forwarded with an inverted re-generated ECRC.

Table 8-3. ECRC Rules for MC_Overlay^a

MC_Overlay Enabled	TLP with ECRC	ECRC Re-Generation Supported	Action if ECRC Check Passes	Action if ECRC Check Fails
No	X	X	Forward TLP unmodified.	
Yes	No	X	Forward modified TLP.	
Yes	Yes	Yes	Forward modified TLP with re-generated ECRC.	Forward modified TLP with inverted re-generated ECRC.

a. "X" is "Don't Care."

8.6.6.1 Multicast to Endpoints without Multicast Extended Capability

An endpoint function that does not contain a **Multicast Extended Capability** structure cannot distinguish MC TLPs from Unicast TLPs. It is possible to take advantage of this, to use such endpoints as MC targets. The PEX 8747 Port above the device can be configured to overlap at least part of the MC Address range, or the MC_Overlay mechanism can be used.

8.6.6.2 Congestion Avoidance

The use of MC increases the output Link use of switches to a degree proportional to both the size of the MC groups used and the fraction of MC traffic to total traffic, which can increase the risk of congestion and spreading. To mitigate this risk, design components that are intended to serve as MC targets to consume MC TLPs at wire speed. Components intended to serve as MC sources should consider adding a rate-limiting mechanism.

8.6.7 Multicast Extended Capability

MC functionality is controlled by the **Multicast Extended Capability** structure. Multiple copies of this structure are required – one for each PEX 8747 Port that supports MC. To provide implementation efficiencies, certain fields within each of the MC Capability structures within a component, must be programmed the same. Results are indeterminate if this is not the case. The fields and registers that must be configured with the same values include MC_Enable, MC_Num_Group, MC_Base_Address, and MC_Index_Position. These same fields in an endpoint's **Multicast Extended Capability** structure must match those configured within a **Multicast Extended Capability** structure of the PEX 8747 above the endpoint, or in which the Root Complex integrated endpoint is integrated.



Chapter 9 Interrupts

9.1 Interrupt Support

The PEX 8747 supports the PCI Express interrupt model, which uses two mechanisms:

- INT_x Interrupt Message-type emulation (compatible with the *PCI r3.0*-defined Interrupt signals)
- Message Signaled Interrupt (MSI), when enabled

For Conventional PCI compatibility, the PCI INT_x emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifics. The PCI INT_x emulation mechanism virtualizes PCI physical Interrupt signals, by using an in-band signaling mechanism, for the assertion and de-assertion of INT_x interrupt signals.

In addition to PCI INT_x-compatible interrupt emulation, the PEX 8747 supports the MSI mechanism. The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r3.0*.

INT_x and MSIs are mutually exclusive, on a per-Port basis; either can be enabled in a system (depending upon which interrupt type the system software supports), but never concurrently within the same domain. (Refer to the **PCI Command** register *Interrupt Disable* bit, offset 04h[10], and **MSI Control** register *MSI Enable* bit, offset 48h[16], respectively.) The PEX 8747 does not convert received INT_x Messages to MSI Messages.

The PEX 8747's external Interrupt output, **PEX_INTA#**, indicates the assertion and/or de-assertion of the internally generated INT_x signal:

- **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output for GPIO-Generated Interrupts* bit (Port 0, 8, or 16, offset 720h[6]).

When this bit is Set, Device-Specific errors trigger PEX_INTA# assertion.

- **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output for Link State Event-Triggered Interrupts* bit (Port 0, 8, or 16, offset 720h[4]).

When this bit is Set, Link State events trigger PEX_INTA# assertion; however, an INT_x Message is not generated in this case.

In both cases, PEX_INTA# assertion and INT_x Message generation are mutually exclusive, on a per-Port basis.

9.1.1 Interrupt Sources or Events

The PEX 8747 internally generated interrupt/Message sources include:

- [Presence Detect Changed](#) (SerDes Receiver Detect^a on Lane(s) associated with that Port)
- [Data Link Layer State Changed](#)
- General-Purpose Input/Output (GPIO) events

The PEX 8747 externally generated interrupt/Message sources include INT_x Messages from Downstream devices.

[Table 9-1](#) lists the interrupt sources.

a. The SerDes Receiver Detect mechanism is comprised of the [Physical Layer Receiver Detect Status](#) register [Receiver Detected on Lane x](#) bits (Port 0, 8, or 16, offset 200h[31:16]).

Table 9-1. Interrupt Sources

Event/Error	Description
Link State events	<p>Slot Status register (offset 80h):</p> <ul style="list-style-type: none"> • <i>Presence Detect Changed</i> (Downstream Ports, bit 19) is Set • <i>Data Link Layer State Changed</i> (Downstream Ports, bit 24) is Set
PCI Express Hot Plug events	<p>The master control of Hot Plug interrupts is the Slot Control register <i>Hot Plug Interrupt Enable</i> bit (Downstream Ports, offset 80h[5]).</p> <p>There are two sources of Hot Plug interrupts. Each Hot Plug source has its own <i>Enable</i> bit in the Slot Control register:</p> <ul style="list-style-type: none"> • <i>Presence Detect Changed</i> (bit 19) • <i>Data Link Layer State Changed</i> (bit 24) <p>The interrupt status of each Hot Plug source is provided by the Port's Slot Status register (Downstream Ports, offset 80h).</p> <p><i>Note: Presence (Slot Status register Presence Detect State bit (Downstream Ports, offset 80h[22])) is determined by the logical OR of the SerDes Receiver Detect (Physical Layer Receiver Detect Status register Receiver Detected on Lane x bits (Port 0, 8, or 16, offset 200h[31:16])).</i></p>
General-Purpose Input Interrupt events	<p>External interrupt from any of the PORT_GOODx# and GPIOx signals that are configured as an Interrupt input in the GPIO x_y Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and 604h).</p>
Device-Specific Error conditions	<ul style="list-style-type: none"> • Device-Specific (RAM ECC) errors indicated by the Device-Specific Error Status x register bit(s), if not masked in their corresponding Device-Specific Error Mask x register bit(s) (Port 0, 8, or 16, offsets 700h, 708h, 710h, and/or 718h (Status) and offsets 704h, 70Ch, 714h, and/or 71Ch (Mask)). <p><i>Note: Device-Specific (RAM ECC) errors can be signaled by interrupt, and/or as an Uncorrectable Internal error that is fatal (Uncorrectable Error Status register Uncorrectable Internal Error Status and Uncorrectable Error Severity register Uncorrectable Internal Error Severity bits (offsets FB8h[22] and FC0h[22], respectively, are Set).</i></p>

9.1.2 Interrupt Handling

The PEX 8747 provides an Interrupt Generation module with each Port. The module reads the Request for interrupts from different sources, then generates an MSI or PCI-compatible Assert_INT_x/Deassert_INT_x Interrupt Message. MSIs support a PCI Express edge-triggered interrupt, whereas Assert_INT_x and Deassert_INT_x Message transactions emulate PCI level-triggered interrupt signaling. The System Interrupt Controller functions include:

- Sensing Interrupt events
- Signaling the interrupt, by way of the INT_x mechanism, and Setting the *Interrupt Status* bit
- Signaling the interrupt, by way of the MSI mechanism
- Handling INT_x-type Interrupt Messages from Downstream devices

The PEX 8747 supports INT_x or MSIs, as per the *PCI Express Base r3.0*.

One INTA# Interrupt output, [PEX_INTA#](#), is implemented.

9.2 INTx Emulation Support

The PEX 8747 supports PCI INTx emulation, to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software. PCI INTx emulation virtualizes PCI physical Interrupt signals, by using the in-band signaling mechanism.

PCI **Interrupt** registers (defined in the *PCI r3.0*) are supported. The Port's *PCI r3.0* **PCI Command** register *Interrupt Disable* and **PCI Status** register *Interrupt Status* bits are also supported (offset 04h[10 and 19], respectively).

Although the *PCI Express Base r3.0* provides INTA#, INTB#, INTC#, and INTD# for INTx signaling, the PEX 8747 uses only INTA# for internal Interrupt Message generation, because it is a single-function device. However, incoming Messages from Downstream devices can be of INTA#, INTB#, INTC#, or INTD# type. Internally generated INTA# Messages from the Downstream Port are also re-mapped and collapsed at the Upstream Port, according to the Downstream Port's Device Number, with its own Device Number and Received Device Number from the Downstream device.

When an interrupt is requested, the Port's **PCI Status** register *Interrupt Status* bit is Set. If INTx interrupts are enabled (Port's **PCI Command** register *Interrupt Disable* and **MSI Control** register *MSI Enable* bits, offsets 04h[10] and 48h[16], are both Cleared, respectively), an Assert_INTx Message is generated and transmitted Upstream to indicate the Port interrupt status. For each interrupt event, there is a corresponding *Interrupt Mask* bit; an Interrupt Message can be generated only when the corresponding *Interrupt Mask* bit is Cleared. Software reads and Clears the event and *Interrupt Status* bit after servicing the interrupt.

A Port de-asserts INTx or PEX_INTA# interrupts, in response to one or more of the following conditions:

- Port's **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- Upstream Port Link goes down (DL_Down condition), or receives a Hot Reset (unless Hot Reset/DL_Down Reset is disabled, by Setting the **Debug** register *Upstream Port DL_Down Reset Propagation Disable* bit (Upstream Port, offset A30h[4]))
- Software Clears the corresponding *Interrupt Status* bit

9.2.1 INTx-Type Interrupt Message Re-Mapping and Collapsing

The Upstream Port re-maps and collapses the INTx *virtual wires* received at a Downstream Port, based upon the Downstream Port's Device Number and Received INTx Message Requester ID Device Number, and generates a new Interrupt Message, according to the mapping defined in [Table 9-2](#).

Each virtual PCI-to-PCI bridge of a Downstream Port specifies the Port Number associated with the INTx (Interrupt) Messages received or generated, and forwards the Interrupt Messages Upstream.

A Downstream Port transmits an Assert_INTA/Deassert_INTA Message to the Upstream Port, due to a PCI Express Hot Plug, Link State, and/or GPIO error/event.

Internally generated INTx Messages always originate as type INTA Messages, because the PEX 8747 is a single-function device. Internally generated Interrupt INTA Messages from Downstream Ports are re-mapped at the Upstream Port to INTA, INTB, INTC, or INTD Messages, according to the mapping defined in [Table 9-2](#).

INTx Messages from Downstream devices and from internally generated Interrupt Messages are ORed together to generate INTA, INTB, INTC, or INTD level-sensitive signals, and edge-detection circuitry in the Upstream Port generates the Assert_INTx and Deassert_INTx Messages. The Upstream Port then forwards the new Messages Upstream, by way of its Link.

Table 9-2. Downstream/Upstream Port INTx Interrupt Message Mapping

Device Number ^a	At Downstream Port	By Upstream Port
0, 8, 16	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
9, 17	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA

a. [Table 4-1](#) indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.

9.3 MSI Support

One of the interrupt schemes supported by the PEX 8747 is the MSI mechanism, which is required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSIs are edge-triggered interrupts.

Note: *MSIs and INTx are mutually exclusive, on a per-Port basis. The mechanisms that generate these types of interrupts **cannot** be simultaneously enabled.*

9.3.1 MSI Operation

At configuration time, system software traverses the function Capability list. If a **Capability ID** of 05h is found, the function implements MSIs. System software reads the **MSI Capability** structure registers, to determine function capabilities.

The Port's **MSI Control** register *Multiple Message Capable* field (offset 48h[19:17]) default value is 010b, which indicates that the PEX 8747 can request up to four MSI Vectors (Address and Data). When the Port's register's *Multiple Message Enable* field (offset 48h[22:20]) is Cleared (default), only one Vector is allocated, and therefore, the PEX 8747 can generate only one Vector for all errors or events. When system software writes a 010b value to the *Multiple Message Enable* field, four-Vector support is enabled (the quantity of Vectors supported is dependent upon the value).

System software initializes the Port's MSI Address registers (offsets 4Ch and 50h) and **MSI Data** register (offset 54h), with a system-specified Vector. After system software enables the MSI function (by Setting the Port's **MSI Control** register *MSI Enable* bit, offset 48h[16]), when an Interrupt event occurs, the Interrupt Generation module generates a DWord Memory Write to the address specified by the Port's **MSI Address** (lower 32 bits of the *Message Address* field) and **MSI Upper Address** (upper 32 bits of the *Message Address* field) register contents (offsets 4Ch and 50h, respectively). The single DWord Payload includes zero (0) for the upper two bytes, and the lower two bytes are taken from the **MSI Data** register. The Port's **MSI Control** register *Multiple Message Enable* field (offset 48h[22:20]) can be programmed to a value of 000b, 001b, or 010b. When programmed to 010b, the lower three bits of Message data are changed to indicate the general type of interrupt event that occurred.

The quantity of MSI Vectors generated is dependent upon the quantity enabled:

- If **one** MSI Vector is enabled (default), all three interrupt events are combined into a single Vector
- If **two** MSI Vectors are allocated, the individual Vectors indicate:
 - Vector[0] Link State-/PM-triggered interrupt event or GPIO-generated event
 - Vector[1] Device-specific RAM ECC error event
- If **four** MSI Vectors are allocated (up to three Vectors are used), the individual Vectors indicate:
 - Vector[0] Link State-/PM-triggered interrupt event
 - Vector[1] Device-specific RAM ECC error event
 - Vector[2] GPIO-generated event
 - Vector[3] **Reserved**

If a non-masked Interrupt event occurs before system software Sets the **MSI Control** register *MSI Enable* bit, normally (but unlike Conventional PCI interrupts, which are level-triggered), an MSI packet is sent immediately after software Sets the *MSI Enable* bit, to notify the system of the prior event. Alternatively, MSIs for prior events can be disabled, on a per-Port basis, by Setting the **ECC Error Check Disable** register *Disable Sending MSI if MSI Is Enabled after Interrupt Status Set* bit (Port 0, 8, or 16, offset 720h[10]).

When the error or event that caused the interrupt is serviced, the PEX 8747 can generate a new MSI Memory Write as a result of new events. Because MSIs are edge-triggered events, the **MSI Mask** register *Interrupt Mask* bits (offset 58h[2:0]) are provided, to use for masking the events. A new MSI can be generated only after the *Interrupt Status* bits are serviced. System software should mask these bits when an MSI event is being processed.

The **MSI Control** register *MSI 64-Bit Address Capable* bit is enabled (offset 48h[23] is Set), by default. If the serial EEPROM and/or I²C/SMBus Clears the bit, the **MSI Capability** structure is reduced by 1 DWord (*that is*, register offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively).

9.3.2 MSI Capability Registers

For details, refer to [Section 11.9, “Message Signaled Interrupt Capability Registers \(Offsets 48h – 64h\).”](#)

9.4 PEX_INTA# Interrupts

PEX_INTA# Interrupt output is enabled when the following conditions are met:

- INTx Messages are enabled (Port's **PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared) and MSIs are disabled (Port's **MSI Control** register *MSI Enable* bit, offset 48h[16], is Cleared)
- PEX_INTA# output is enabled for the following errors and events, when the **ECC Error Check Disable** register bit associated with that error or event is Set:
 - *Enable PEX_INTA# Interrupt Output for GPIO-Generated Interrupts* bit (Port 0, 8, or 16, offset 720h[6])
 - *Enable PEX_INTA# Interrupt Output for Link State Event-Triggered Interrupts* bit (Port 0, 8, or 16, offset 720h[4])

The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:

- Conventional PCI INTx Message generation
- Native MSI transaction generation
- Device-Specific PEX_INTA# assertion

PEX_INTA# assertion (Low) indicates that the PEX 8747 detected one or more of the events and/or errors (if not masked) listed in [Table 9-1](#).

Note: *PEX_INTA# assertion and INTx messaging are mutually exclusive for a given interrupt event. When MSIs are enabled (Port's *MSI Enable* bit is Set), both INTx and PEX_INTA# are disabled for PEX 8747 internally generated interrupts. The forwarding of external INTx Messages received from a Downstream Port to the Upstream Port is always enabled.*

9.5 General-Purpose Input/Output

The PEX 8747 contains 11 General-Purpose Input/Output (GPIO) balls. They can be used as GPIO, interrupt, or PORT_GOOD indicators. The balls can default to the PORT_GOOD output function, either through register programming and/or the [STRAP_TESTMODE0](#) input state. The logic that controls the GPIO ball function is driven from the Chip-specific **GPIO** registers (Port 0, offsets [600h](#) through [63Ch](#)).

[Table 9-3](#) lists the Chip-specific registers (located in Port 0) used for GPIO functionality.

Table 9-3. Registers Used for GPIO Functionality

Offset	Register
600h	GPIO 0_9 Direction Control
604h	GPIO 10 Direction Control
614h	GPIO 0_10 Input De-Bounce
61Ch	GPIO 0_10 Input Data
624h	GPIO 0_10 Output Data
62Ch	GPIO 0_10 Interrupt Polarity
634h	GPIO 0_10 Interrupt Status
63Ch	GPIO 0_10 Interrupt Mask

10.1 Overview

The PEX 8747 Power Management (PM) features provide the following services:

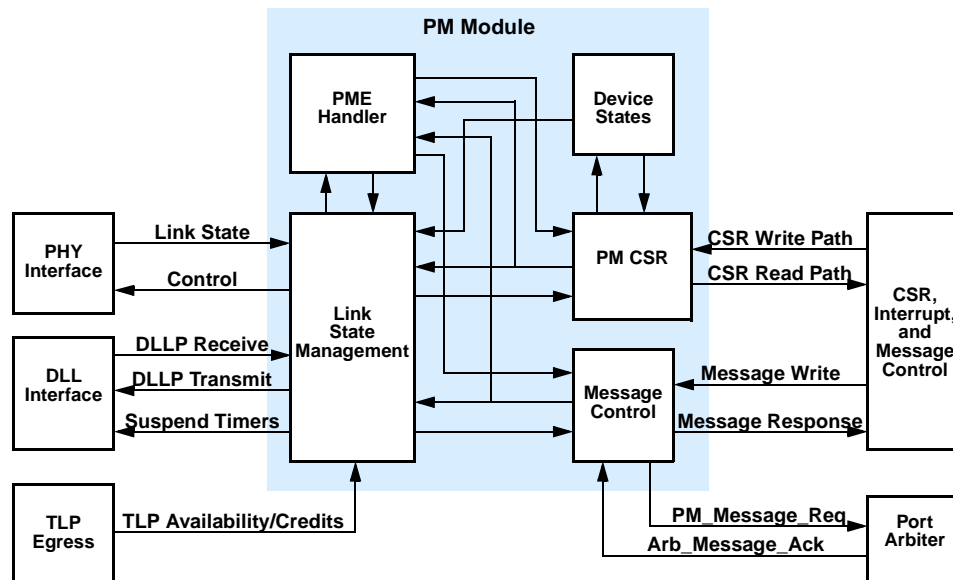
- Mechanisms to identify PM capabilities
- Ability to transition into certain PM states
- Notification of the current PM state of each Port
- Support for the option to wakeup the system upon a specific event

The PEX 8747 supports hardware-autonomous PM and software-driven D-State PM. The switch also supports the L0s and L1 Link PM states in hardware-autonomous Active State Power Management (ASPM), as well as the L1, L2/L3 Ready, and L3 Link PM states in Conventional PCI-compatible PM. D0, D3hot, and D3cold states are supported in Conventional PCI-compatible PM. Because the PEX 8747 does *not support* Vaux, Power Management Event (PME) generation from the D3cold state is *not supported*.

The PM module interfaces with a Physical Layer (PHY) electrical sub-block, to transition the Link state into a low-power state, when the module receives a Power State Change Request from a Downstream component, or an internal event forces the Link state entry into low-power states in hardware-autonomous ASPM mode. PCI Express Link states are not directly visible to Conventional PCI Bus driver software; however, they are derived from the PM state of the components residing on those Links.

Figure 10-1 provides a functional block diagram of the PEX 8747 PM module.

Figure 10-1. PM Module Functional Block Diagram



10.2 Power Management Features

- *PCI Express Base r3.0*-compliant
- *PCI Power Mgmt. r1.2*-compliant
- Link Power Management States (*L-States*; also referred to as *Link PM states*)
 - PCI Bus Power Management – L1, L2/L3 Ready, and L3 (Vaux is ***not supported***)
 - Active State Power Management (ASPM) – L0s and L1
- Device Power Management State (*D-States*; also referred to as *PCI Express PCI-PM states*)
 - D0 (D0 Uninitialized and D0 Active) and D3 (D3hot and D3cold) support
- Power Management Event (PME) support from D3hot
- PME due to PCI Express Hot Plug events
- Forwards PME_Turn_Off broadcast Messages
- Implements Gen 3-specific Control and Status register and associated interrupts
- Supports ASPM L0s, ASPM L1, PCI PM L1, and L2/L3 Ready Link PM states

10.3 Power Management Capability

10.3.1 Device Power Management States

The PEX 8747 supports the PCI Express PCI-PM D0 and D3hot states. The PCI-PM D1 and D2 states, which are optional in the *PCI Express Base r3.0*, are **not supported**.

The D3hot state can be entered from the D0 Uninitialized or D0 Active states, when system software programs the Port's **PCI Power Management Status and Control** register *Power State* field (offset 44h[1:0]) to 11b. The PCI-PM D0 Uninitialized state can be entered from the D3hot state when system software Clears the Port's *Power State* field.

10.3.1.1 D0 State

A PCI Express device must be put into the PCI Express PCI-PM D0 state before it can be used. When the device enters the D0 state following a Fundamental Reset, it is in the D0 Uninitialized state. A subsequent Reset forces the device into the D0 Uninitialized state.

Other than the Fundamental Reset that brings the device to the D0 Uninitialized state, all other PM state transitions are explicitly controlled by software.

A device enters the PCI Express PCI-PM D0 Active state when system software Sets any combination of the **PCI Command** register *Bus Master Enable*, *Memory Access Enable*, and/or *I/O Access Enable* bits (offset 04h[2, 1, and/or 0], respectively).

10.3.1.2 D3hot State

In the PCI Express PCI-PM D3hot state, PCI Express Hot Plug or Link State operations can cause the PEX 8747 to generate a PME.

Only Type 0 Configuration accesses are allowed in the D3hot state. Memory and I/O transactions result in an Unsupported Request (UR). Completions flowing in either direction are not affected.

Type 1 transactions flowing toward a PEX 8747 Port in the D3hot state are terminated as URs. Type 0 Configuration transactions complete successfully. When the PEX 8747 Upstream Port is programmed to the D3hot state, the Port initiates Conventional PCI-PM L1 Link PM state entry.

10.3.2 Link Power Management States

PEX 8747 components hold their Upstream and Downstream Links in the L0 Link PM state during standard device operation (PCI Express PCI-PM D0 Active state). ASPM defines a mechanism for components in the PCI Express PCI-PM D0 state, to reduce Link power by placing their Links into a low-power state and instructing the other end of the Link to do likewise. This capability allows hardware-autonomous, dynamic Link power reduction beyond what is achievable by software-only-controlled PM. Table 10-1 defines the relationship between a component's Power state and Upstream Link. Table 10-2 defines the relationship between Link PM states and power-saving actions.

PCI Express PCI-PM L1 and L2/L3 Ready Link PM states are controlled by software programming the PEX 8747 into the PCI Express PCI-PM D3hot state, and subsequently causing the Root Complex to broadcast the PME_Turn_Off Message to the Downstream hierarchy.

Table 10-1. Relationship between Component Power State and Upstream Link

Downstream Component PCI Express PCI-PM State	Permissible Upstream Component PCI Express PCI-PM State	Permissible Interconnect Link PM State
D0	D0	L0, and optionally L0s and L1 if ASPM is enabled
D3hot	D0-to-D3hot	L1, L2/L3 Ready.
D3cold (no Vaux)	D0-to-D3cold	L3 (off). Zero power.

Table 10-2. Relationship between Link PM States and Power-Saving Actions

Link PM State	Power-Saving Actions
Tx L0s	PHY Tx Lanes are in a High-Impedance state.
Rx L0s	PHY Rx Lanes are in a low-power state.
L1	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L2/L3 Ready	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L3 (D3cold)	Component is fully powered Off.

10.3.3 Active State Power Management – L0s Link PM State Transition

L0s Link PM state entry is mandatory, and this state is allowable only in Active State Link Power Management (ASPM). Each device reports its support to L0s entry through the Port's **Link Capability** register *Active State Power Management (ASPM) Support* field (offset 74h[11:10]). Software enables L0s state entry, by writing into Active state Link PM Control register. The L0s Link PM state is optimized for short entry and exit latencies, while providing substantial power savings. If the L0s state is enabled in a device, transmit Links that are not being used must be brought into the L0s state.

Link Layer Timers are *not* affected by a transition to the L0 Link PM state. When in the L0s state, Links return to the L0 state, regardless of whether there are any TLP traffic situations to transmit Flow Control (FC) updates, which occurs every 30 μ s minimum.

10.3.3.1 Rx L0s Link PM State Entry

The PEX 8747 allows its Rx Lanes to go into the L0s Link PM state, regardless of whether its Tx is enabled for L0s.

10.3.3.2 Rx L0s Link PM State Exit

The endpoint Transmitter at the opposite end of a PCI Express Link transmits a quantity of FTS and goes back to L0 state. If the PEX 8747 Receiver achieves symbol and bit lock, it settles into the L0 Link PM state. Otherwise, the Receiver enters the *Recovery* state.

10.3.3.3 Tx L0s Link PM State Entry Conditions

L0s Link PM State Entry Conditions – Upstream Port

The following four conditions must be met for the Upstream Port to enter the L0s state:

1. All PEX 8747 Downstream Port Receiver Lanes are in the L0s Link PM or deeper state. If the PEX 8747 Downstream Port Link is in a *Link Down* state, this condition is also satisfied.
2. No pending TLPs (including Retry TLPs), or there are no credits available to transmit pending TLPs.
3. No DLLPs pending in the DLL.
4. Enabled in the Port's **Link Capability** register *Active State Power Management (ASPM) Support* field (offset 74h[11:10]), programmed to 01b or 11b), for going into the L0s state.

The PM module directs the Upstream Link to go into the L0s state when Conditions 1, 2, and 3 are met for a specified period of time and Condition 4 is satisfied. The idle time can be selected, as either 1 μ s (default) or 4 μ s, in the Port's **Power Management Hot Plug User Configuration** register *L0s Entry Idle Count* bit (offset F70h[0]). If these conditions are met for the specified time period of time, PM directs the PHY to the L0s state.

L0s Link PM State Entry Conditions – Downstream Ports

The following four conditions must be met for the Upstream Port to enter the L0s state:

1. All PEX 8747 Upstream Port Receiver Lanes are in the L0s state.
2. No pending TLPs (including Retry TLPs), or there are no credits available to transmit pending TLPs.
3. No DLLPs pending.
4. Enabled in the Port's **Link Capability** register *Active State Power Management (ASPM) Support* field (offset 74h[11:10], programmed to 01b or 11b), for going into the L0s state.

The PM module directs the Downstream Link to go into the L0s state when Conditions 1, 2, and 3 are met for a specified period of time and Condition 4 is satisfied. The idle time can be selected, as either 1 μ s (default) or 4 μ s, in the Port's **Power Management Hot Plug User Configuration** register *L0s Entry Idle Count* bit (offset F70h[0]).

10.3.3.4 L0s Link PM State Exit Conditions

Components from either end of a PCI Express Link can initiate exit from the L0s Link state.

L0s Link PM State Exit Conditions – Upstream Port

One or more of the following conditions must be met for the Upstream Port to exit the L0s state:

- If there are pending DLLPs or TLPs to transmit, –or–
- If any of the Downstream Port Rx Lanes exit the L0s state. When a Downstream Port Rx Lane exits the L0s or L1 Link PM state, a Link State Change vendor-defined Message is transmitted to the Upstream Port.
- Upstream Port ASPM L1 entry conditions are met.
- Upstream Port is placed into the PCI Express PCI-PM D3hot state.
- Link is Set to retrain, as a result of a DLLP timeout or Replay Number Rollover.

L0s Link PM State Exit Conditions – Downstream Ports

One or more of the following conditions must be met for a Downstream Port to exit the L0s state and enter the L0 Link PM state:

- If there are pending DLLPs or TLPs to transmit, –or–
- If any of the Upstream Port Rx Lanes exit the L0s state. When an Upstream Port Rx Lane exits the L0s or L1 Link PM state, a Link State Change vendor-defined Message is transmitted to all Downstream Ports.
- Port's **Link Control** register *Retrain Link* or *Link Disable* bit (Downstream Ports, offset 78h[5:4], respectively) is Set.
- If a PCI-PM L1 Entry Request or Active State L1 Request is received from the Downstream direction.

The PM module directs the PHY to change from the L0s state to the operational L0 state, when any of the conditions listed above are met. The PHY transmits the Fast Training Sets (FTS), then enters the L0 state.

10.3.3.5 L1 Link PM State Entry

The L1 state is a deeper power-saving state than the L0s Link PM state, with both Tx and Rx Lanes settling into Electrical Idle after L1 negotiation is complete.

A PCI Express Upstream Link can enter the L1 state when:

- Upstream Port is placed into the PCI Express PCI-PM D3hot state.
- Upstream Port is in the D0 Active state, and Idle conditions (explained below) are satisfied and the Port is enabled in the Port's **Link Control** register *Active State Power Management (ASPM)* field is programmed for ASPM L1 (offset 78h[1:0] is programmed to 10b or 11b)

Downstream Ports never initiate a L1 state entry. Downstream Port Links can enter the L1 state when:

- Downstream device is in the D0 state and initiates L1 state entry (Port's **Link Control** register *Active State Power Management (ASPM)* field (offset 78h[1:0]) is programmed to 10b or 11b).
- Downstream device is placed into a PCI Express PCI-PM D3hot state, and initiates L1 state entry

Entry into the L1 state is always initiated by the Upstream Port or a Downstream device. ASPM L1 state is optional, and software-controlled, by writing into the *Active State Power Management (ASPM)* field. However, L1 state entry is also possible in the PCI Express PCI-PM, when the Upstream Port is placed into a state other than the PCI Express PCI-PM D0 state. This transition is required. Conditions for entering the ASPM L1 state are implementation-specific. Downstream Ports never initiate L1 state entry.

A Port cannot directly go from the L0s to L1 state while in ASPM. In ASPM, the transition is L0s -> L0 -> L1. After L1 state entry, Flow Control Update Timers are suspended.

PCI-PM-compatible L1 entry protocol uses the PM_enter_L1_DLLP; however, ASPM uses PM_active_state_request_L1_Dllp. Downstream Ports never NAK the PM_enter_L1_DLLP received from a Downstream device; however, it can NAK PM_active_state_request_L1_Dllp, if there is something to transmit.

ASPM L1 State Entry Conditions – Upstream Port

The Upstream Port requests ASPM L1 state entry and waits up to 1 to 2 μ s, when the following conditions are met:

- Upstream Port is in the PCI Express PCI-PM D0 state, and enabled for ASPM L1 state entry (Port's **Link Control** register *Active State Power Management (ASPM)* field (offset 78h[1:0]) is programmed to 10b or 11b)
- All Downstream Port Links are in the L1 or deeper state, or the Link is Down
- No pending TLPs to transmit, including TLPs waiting for DLL ACK/NAK (in the Retry buffer)
- No pending DLLPs, except for FC DLLPs

Also, the Upstream Port should have the maximum FC credits to transmit the maximum packet size for each enabled Virtual Channel (VC) packet type. The Upstream Port suspends the transmission of new TLPs.

The Upstream Port continuously transmits PM_active_state_request_L1_Dllp, until it sees a PM_request_Ack DLLP or PM_Active_state_Nak TLP Message. These DLLPs are transmitted with no more a 4-symbol time gap on the Upstream Link.

After the Upstream Port receives PM_request_Ack DLLP, it directs the PHY to enter the L1 state. The Link settles into the L1 state when an Electrical Idle Ordered-Set (EIOS) is transmitted, and Electrical Idle is received. After a PM_Active_state_Nak TLP is received, the Link enters the L0s state, as soon as possible, if conditions are met.

PEX 8747 Upstream Port when enabled for L0s and L1 ASPM, and is in L0s for more than 2 μ s and above L1 entry conditions are met, exits L0s and negotiates for L1 entry.

Upstream Port Requests PCI Express PCI-PM L1 Entry

The Upstream Port requests PCI Express PCI-PM L1 state entry, when the following six conditions are met:

- Software places the Upstream Port into the PCI Express PCI-PM D3hot state.
- Upstream Port suspends the scheduling of new TLPs, after a Completion for that particular packet is transmitted Upstream.
- Upstream Port waits until all previously transmitted TLPs are acknowledged. During this time, the Upstream Port receives TLPs and DLLPs. Also transmits ACK/NAK and FC DLLPs.
- Upstream Port waits for a sufficient quantity of FC credits, for all types of TLP packets.
- Upstream Port waits for all the Retry TLPs to complete.
- After the Upstream Port transmits all pending TLPs, it transmits a PM_EnterL1_Dllp Upstream, with no more than a 4-symbol time gap.

When the Upstream Port receives the PM_Request_Ack DLLP, it directs the Link to enter the L1 state.

When in the L1 state, if an Electrical Idle exit is detected, or a TLP must be transmitted, the Upstream Port exits the L1 state, transmits the pending TLP(s), if required, then re-enters the PCI Express PCI-PM L1 state after a 16- μ s delay. The Upstream Port must detect a continuous 16 μ s of the PHY L0 state for the next state entry.

Downstream Port Accepts Request from Downstream Device PM_active_state_request_L1_Dllp

A Downstream Port accepts a Request from the Downstream device PM_active_state_request_L1_Dllp and suspends the transmission of new TLPs, when the following three conditions are met:

- Downstream Port supports, and is enabled for, ASPM L1 state entry (Port's [Link Control](#) register [Active State Power Management \(ASPM\)](#) field (Downstream Ports, offset 78h[1:0]) is programmed to 10b or 11b)
- No TLPs are scheduled for transmission
- No DLLPs, other than FC DLLPs, are pending

The Downstream Port transmits PM_request_Ack DLLP continuously until the receive Lanes goes to Electrical Idle, which indicates the other side of the Link has received Ack. After it receives Electrical Idle, power management directs the PHY to go to the L1 state.

If the conditions for going to L1 are not satisfied, PEX 8747 Downstream Port transmits PM_Active_state_Nak Message and it remains in the L0 state.

Downstream Port Accepts Request from Downstream Device PM_Enter_L1_Dllp

A Downstream Port accepts a Request from the Downstream device PM_enter_L1_Dllp, if the following three conditions are met:

- No TLPs are scheduled for transmission
- TLP transmissions are suspended
- Downstream Port received a Link Layer ACK for all transmitted TLPs

The Downstream Port continuously transmits PM_Enter_Ack_DLLP, with no more than a 4-symbol time gap between subsequent DLLPs. When the Downstream Port “sees” the Rx Lanes go into Electrical Idle, the Port directs the PHY to enter the L1 state.

10.3.3.6 L1 Link PM State Exit Conditions

Devices on either end of a PCI Express Link can initiate exit from the L1 state. Unlike the L1 state entry protocol, in which both ends of the Link must negotiate for the resultant Link state, L1 state exit does *not* require negotiation.

ASPM L1 Link PM State Exit Conditions – Upstream Port

The following conditions must be met for the Upstream Port to exit the ASPM L1 state:

- Any Downstream Port exits the L1 state.
- TLPs are pending transmission.
- Any Upstream Port Rx Lane exits Electrical Idle.
- Upstream Port is placed in the PCI Express PCI-PM D3hot state.

PCI Express PCI-PM D3hot State Exit Conditions – Upstream Port

One or both of the following conditions must be met for the Upstream Port to exit the PCI Express PCI-PM D3hot state:

- Any Upstream Port Rx Lane exits Electrical Idle, –or–
- Downstream Port exited the L1 state as the result of a Downstream Port Rx Lane exiting Electrical Idle while in the L1 state.

ASPM L1 Link PM State Exit Conditions – Downstream Ports

The following conditions must be met for a Downstream Port to exit the ASPM L1 state:

- Any Downstream Rx Lanes exit Electrical Idle.
- TLPs are pending transmission on the Link.
- Upstream Port starts to exit the L1 state. Downstream Ports, which are in the L1 state as the result of a Downstream device being placed into the PCI Express PCI-PM D3hot state, are not affected by this transition.

PCI Express PCI-PM D3hot State Exit Conditions – Downstream Ports

The following conditions must be met for a Downstream Port to exit the PCI Express PCI-PM D3hot state:

- Any Downstream Rx Lanes exit Electrical Idle.
- TLPs are pending transmission on the Link.

10.3.3.7 L1 Link PM State Entry Negotiation Interruption – ASPM and PCI Express PCI-PM

Per the *PCI Express Base r3.0*, when L1 state entry negotiation is interrupted, the state machine on both ends of the PCI Express Link should return to an Idle state. A Port can be in any of the states described in the sections that follow, when L1 state entry negotiation is interrupted, usually as the result of a trip through the *Recovery* state.

L1 Link PM State Entry Negotiation Interruption – Upstream Port

What occurs after L1 state entry negotiation is interrupted on the Upstream Port is dependent upon the following:

- **Started requesting L1 entry, using PM_request DLLPs** – When the Tx or Rx *Recovery* state occurs, the Port stops receiving Requests, returns to an Idle state, then waits 10 μ s before making another L1 state entry Request, –or– the Tx Lane should enter the L0s Link PM state.
- **Waiting for a PM request ACK** – When the Tx or Rx *Recovery* state occurs, the Port returns to an Idle state, then waits 10 μ s before making another L1 state entry Request, –or– the Tx Lane should enter the L0s Link PM state.
- **After receiving a PM Request ACK, directs the PHY to the L1 state, and the PHY has not reached the L1 state and the PHY enters the Tx or Rx Recovery state** – The Port returns to an Idle state, then waits 10 μ s before making another L1 state entry Request, –or– the Tx Lane should enter the L0s Link PM state.
- **After the PHY transmits an EIOS and settles in the Tx L1 state, the Rx has not yet reached the L1 state, and an Rx Recovery state occurs or the Port's Link Control register Retrain Link bit (Downstream Ports, offset 78h[5]) is Set** – The Port directs the PHY Tx to exit the L1 state.

L1 Link PM State Entry Negotiation Interruption – Downstream Ports

What occurs after L1 state entry negotiation is interrupted on the Downstream Ports is dependent upon the following:

- **Transmits PM_request ACK DLLPs for an L1 state entry Request** – When the Tx or Rx *Recovery* state occurs, the Port returns to an Idle state, then waits 10 μ s before validating another L1 state entry Request from the Downstream device, –or– the Rx should enter the L0s Link PM state, to validate the next L1 state entry Request.
- **Waits for Electrical Idle from the other side of the PCI Express Link** – When the Tx or Rx *Recovery* state occurs, the Port returns to an Idle state, then waits 10 μ s before validating another L1 state entry Request from the Downstream device, –or– the Rx should enter the L0s Link PM state, to validate the next L1 state entry Request.
- **Rx is in the L1 state and directs the PHY to enter the L1 state** – If the PHY enters the Tx *Recovery* state because the Port's Link Control register Retrain Link bit (Downstream Ports, offset 78h[5]) is Set, the Port returns to an Idle state, then waits 10 μ s before validating another L1 state entry Request from the Downstream device, –or– the Rx should enter the L0s Link PM state, to validate the next L1 state entry Request.

10.3.3.8 L2/L3 Link PM State Entry

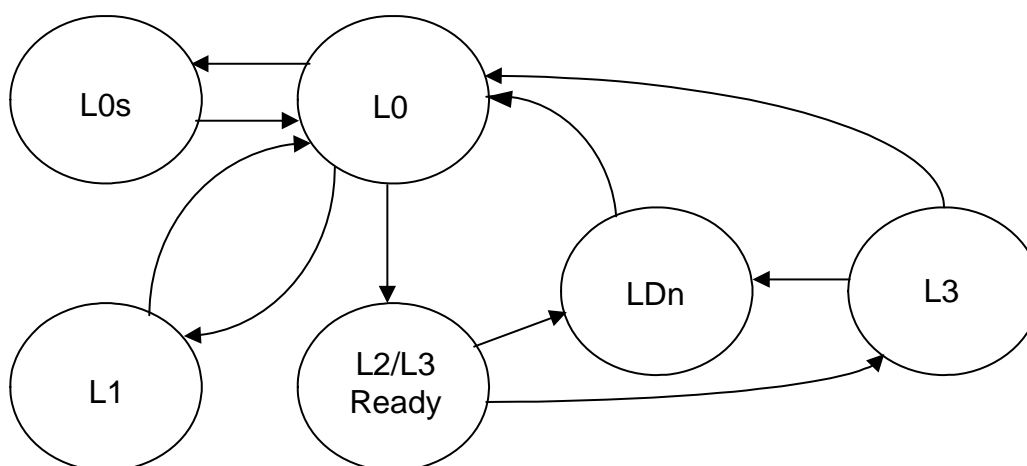
The L2 and L3 states are the staging points for removing main power. Support for the L2/L3 Ready transition protocol is required.

The L2 and L3 states are related to the PCI Express PCI-PM D-state transitions. L2/L3 Ready is the state in which a given Link enters when the platform is preparing to enter its system sleep state. Following completion of the L2/L3 Ready state transition protocol, the Link enters the L2/L3 Ready state. After main power is removed, the Link settles into the L3 state. The time for the L2/L3 Ready state entry transition is indicated by completion of the PME_Turn_Off/PME_TO_Ack handshake sequence. Any actions on the part of the Downstream component necessary to ready itself for power loss must be completed prior to initiating the transition to the L2/L3 Ready state. After all preparations for loss of power and clock are complete, the Downstream component initiates L2/L3 Ready state entry, by transmitting the PM_EnterL23 DLLP Upstream.

Exit from the L2/L3 Ready state, back to the L0 Link PM state, can be initiated only by an Upstream-initiated transaction that targets the Downstream component (Upstream Electrical Idle exit) in the same manner that an Upstream-initiated transaction trigger would trigger the transition from the L1 to L0 Link PM states.

Figure 10-2 illustrates the Link PM state transitions.

Figure 10-2. Link PM State Transitions



PME_TO_Ack TLP Flow from Downstream Device to Upstream Port

Because all previously transmitted packets must first be transmitted Upstream, before transmitting the PME_TO_Ack packet, the PEX 8747 performs the following tasks:

1. When a PME_TO_Ack is received from a Downstream device, it is routed to the Station's Upstream Egress module.
2. The Egress module decodes the PME_TO_Ack TLP, then informs the Upstream Port's PM module that it received the PME_TO_Ack.
3. When the Upstream Port receives the PME_TO_Ack Message from all enabled Downstream Ports, it transmits PME_TO_Ack Message toward the Root Complex. This Message flushes the previously transmitted PM_PME Messages, due to PEX 8747 internal events.

L2/L3 Ready Link PM State Entry Sequence – Upstream Port

System software places all Downstream devices into the PCI Express PCI-PM D3hot state, before broadcasting the PME_Turn_Off Message. The Root Complex then transmits the Message to the Upstream Port's PM module. The Upstream Port then unicasts the Message to all Downstream Ports, which reports an active Data Link Layer (DLL). Downstream Ports receive a PME_Turn_Off Message from Upstream, then transmit the Message to the Downstream device(s).

1. Upstream Port waits for a PME_TO_Ack Message, from all Downstream devices.
2. Waits for all pending TLP transmission to complete.
3. After all Downstream Ports receive the PME_TO_Ack, the PEX 8747 transmits the PME_TO_Ack Upstream.
4. PEX 8747 transmits the PM_Enter_L23_DLLP Upstream, after all Downstream Ports are in the L2/L3 Ready state.
5. When in the L2/L3 Ready state, if a HP_PWR_GOOD_x input is de-asserted (main power is removed), the Link settles into the L3 Link PM state.

Note: When in the L2/L3 Ready state, a Receiver exiting Electrical Idle also causes exit from the L2/L3 Ready state. The LTSSM enters the Link Down (LDn) state, then the PEX 8747 receives a Soft Reset, which also brings all Downstream Ports to the LDn state, from the L2/L3 Ready state.

After the Upstream Port is in the L2/L3 Ready state, Rx Electrical Idle exit causes the Link to transition to the LDn state, then subsequently enter the *Detect* state.

L2/L3 Ready Link PM State Entry Sequence – Downstream Ports

When a Downstream Port is going into the L2/L3 Ready state, the PEX 8747 performs the following tasks:

1. Downstream Port receives a PME_Turn_Off Message from the Upstream Port.
2. Downstream Port suspends the transmission of new PM_PME Messages (upon global power-off).
3. Transmits PME_Turn_Off Message to the Downstream device after Clearing all pending TLPs.
4. Waits for a PM_Enter_L23_DLLP from the Downstream device. When the PEX 8747 receives the PM_Enter_L23_DLLP, the switch transmits a PM_request_ACK DLLP, then waits for the Rx to enter the L2/L3 Ready state. After the Rx goes into Electrical Idle, the Tx enters the L2/L3 Ready state. The Upstream scoreboard is updated though vendor-defined Messages.
5. When in the L2/L3 Ready state, if a HP_PWR_GOOD_x input is de-asserted (main power is removed), the Link settles into the L3 Link PM state.

10.4 Power Management Tracking

Upstream Port logic tracks the Link status of each Downstream and Upstream Port Link, to derive the following conditions:

- Upstream Port enters the L0s Link PM state when all enabled Downstream Receivers are in the L0s Link PM state or deeper, or in a Link Down state.
- Upstream Port enters the active L1 Link PM state, only when all Downstream Ports are in the active L1 Link PM state or deeper, or the Link is Down.
- When a Downstream Port is in the active L1 Link PM state and an ASPM L1 Link PM state exit is occurring in the Downstream Port, the Upstream Port exits the L1 Link PM state.
- When the Upstream Port is in the active L1 Link PM state and an active L1 Link PM state exit is occurring, due to Receiver Electrical Idle exit, the Downstream Port exits the L1 Link PM state.
- When a PME_TO_Ack Message is received only on all active (not in Link Down) Downstream Ports, a PME_TO_Ack Message is issued toward the Upstream Port.
- When all Downstream Ports are in the L2/L3 Ready Link PM or Link Down state, the Upstream Port transmits PM_ENTER_L23 Data Link Layer Packets (DLLPs) toward the Root Complex.

10.5 Power Management Event Handler

PM_PME Messages are Posted Transaction Layer Packets (TLPs) that inform the PM software which agent within the PCI Express hierarchy has requested a PM-state change. PM_PME Messages are always routed toward the Root Complex.

PCI Express components are permitted to wake the system from any supported PM state, through a PME Request.

When a PEX 8747 Downstream Port is in the PCI Express PCI-PM D3hot state, the following PCI Express Hot Plug events cause the Port's **PCI Power Management Status and Control** register *PME Status* bit (offset 44h[15]) to be Set:

- *Presence Detect Changed* (SerDes Receiver Detect^a on Lane(s) associated with that Port)
- *Data Link Layer State Changed*

This causes the Downstream Port to generate a PM_PME Message, if the Port's **PCI Power Management Status and Control** register *PME Enable* bit (offset 44h[8]) is Set.

*a. The SerDes Receiver Detect mechanism is comprised of the **Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Port 0, 8, or 16, offset 200h[31:16]).*



Chapter 11 Port Registers

11.1 Introduction

This chapter defines the PEX 8747 Port registers. Each PEX 8747 Port has its own Configuration, Capability, Control, and Status register space. The register mapping is the same for each Port. (Refer to [Table 11-1](#).) This chapter also presents the PEX 8747 programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in the Upstream Port and Downstream Ports. (Refer to [Table 11-3](#).)

All PEX 8747 registers can be accessed by Memory Requests. Registers outside the following Device-Specific ranges can also be accessed by Configuration Requests:

- 200h through AFCh
- B0Ch through B6Ch
- B80h through C30h

For reliable operation, software should not write to register offsets that are identified as ***Reserved***.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI-to-PCI Bridge r1.2*
- *PCI Express Base r3.0*

11.2 Type 1 Port Register Map

Table 11-1 defines the Type 1 Port register mapping.

Table 11-1. Type 1 Port Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)																																Capability Pointer (40h)																00h
																																																...
																																																34h
																Next Capability Pointer (48h)																Capability ID (01h)																3Ch
PCI Power Management Capability Registers (Offsets 40h – 44h)																																40h																
																Next Capability Pointer (68h)																Capability ID (05h)																44h
Message Signaled Interrupt Capability Registers (Offsets 48h – 64h)																																48h																
																Next Capability Pointer (A4h)																Capability ID (10h)																...
PCI Express Capability Registers (Offsets 68h – A0h)																																64h																
																Next Capability Pointer (00h)																SSID/SSVID Capability ID (0Dh)																68h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)																																...																
Next Capability Offset (FB4h)								1h								PCI Express Extended Capability ID (0003h)																FCh																
Device Serial Number Extended Capability Registers (Offsets 100h – 108h)																																100h																
																																...																
Next Capability Offset (148h)								1h								PCI Express Extended Capability ID (0019h)																108h																
Secondary PCI Express Extended Capability Registers (Offsets 10Ch – 134h)																																10Ch																
Next Capability Offset (10Ch)								1h								PCI Express Extended Capability ID (0004h)																...																
Power Budget Extended Capability Registers (Offsets 138h – 144h)																																134h																
Next Capability Offset (E00h)								1h								PCI Express Extended Capability ID (0002h)																138h																
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)																																144h																
Device-Specific Registers (Offsets 1C0h – A74h)																																148h																
																																...																
																																1BCh																
																																1C0h																
																																...																
																																A74h																
Reserved																																A78h – AFCh																

Table 11-1. Type 1 Port Register Map (Cont.)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Next Capability Offset (B70h)																1h				PCI Express Extended Capability ID (0018h)																B00h
Latency Tolerance Reporting Extended Capability Registers (Offsets B00h – B08h)																																...	B08h			
Reserved																																B0Ch –	B6Ch			
Next Capability Offset 2 (000h)																1h				PCI Express Extended Capability ID 2 (000Bh)																B70h
Device-Specific Registers (Offsets B70h – DFCh)																																...	DFCh			
Next Capability Offset (B00h or F24h)																1h				PCI Express Extended Capability ID (0012h)																E00h
Multicast Extended Capability Registers (Offsets E00h – E2Ch)																																...	E2Ch			
Reserved																																E30h –	F20h			
Next Capability Offset (B70h)																1h				PCI Express Extended Capability ID (000Dh)																F24h
ACS Extended Capability Registers (Offsets F24h – F2Ch)																																...	F2Ch			
Device-Specific Registers (Offsets F30h – FB0h)																																F30h	...	FB0h		
Next Capability Offset (138h)																1h				PCI Express Extended Capability ID (0001h)																FB4h
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)																																...	FDCh			
Reserved																																FE0h –	FFCh			

11.3 Port Register Configuration and Map

The PEX 8747 Port registers are configured similarly – not all the same. Port 0 of Station 0, Port 8 of Station 1, and Port 16 of Station 2 include more Device-Specific registers than the other Ports. Port 0 also contains registers that are used to set up and control the PEX 8747, as well as a serial EEPROM interface, I²C Slave interface, and SMBus Slave interface logic and control. The Port registers contain setup and control information specific to the Station and its Port(s). [Table 11-2](#) defines the Port register configuration and map.

Table 11-2. Port Register Configuration and Map

Register Types	Station 0, Port 0	Station 1, Port 8 Station 2, Port 16	Station 1, Port 9 Station 2, Port 17 ^a
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)	00h – 0Ch, 18h – 3Ch	00h – 0Ch, 18h – 3Ch	00h – 0Ch, 18h – 3Ch
	Upstream Port 10h, 14h		
PCI Power Management Capability Registers (Offsets 40h – 44h)	40h – 44h	40h – 44h	40h – 44h
Message Signaled Interrupt Capability Registers (Offsets 48h – 64h)	48h – 64h	48h – 64h	48h – 64h
PCI Express Capability Registers (Offsets 68h – A0h)	68h – 78h 84h – A0h	68h – 78h 84h – A0h	68h – 78h 84h – A0h
	Downstream Ports 7Ch, 80h		
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)	A4h – FCh	A4h – FCh	A4h – FCh
Device Serial Number Extended Capability Registers (Offsets 100h – 108h)	100h – 108h	100h – 108h	100h – 108h
Secondary PCI Express Extended Capability Registers (Offsets 10Ch – 134h)	10Ch – 134h	10Ch – 134h	10Ch – 134h
Power Budget Extended Capability Registers (Offsets 138h – 144h)	Upstream Port 138h – 144h		
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)	148h – 1BCh	148h – 1BCh	148h – 174h
WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)	178h – 1BCh	178h – 1BCh	
Device-Specific Registers (Offsets 1C0h – A74h)			
Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)	1D0h – 1D8h	1D0h – 1D8h	
Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1E4h)	1DCh – 1E4h	1DCh – 1E0h	1DCh – 1E0h
Device-Specific Registers – Read Pacing (Offset 1E8h)	1E8h		
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h – 25Ch	200h – 25Ch	
Device-Specific Registers – Serial EEPROM (Offsets 260h – 270h)	260h – 270h		
Device-Specific Registers – I2C and SMBus Slave Interfaces (Offsets 290h – 2FCh)	290h – 2FCh		

Table 11-2. Port Register Configuration and Map (Cont.)

Register Types	Station 0, Port 0	Station 1, Port 8 Station 2, Port 16	Station 1, Port 9 Station 2, Port 17 ^a
Device-Specific Registers – Port Configuration and Lane Status (Offsets 300h – 350h)	300h – 350h		
Device-Specific Registers – Port Configuration (Offsets 354h – 46Ch)	354h – 46Ch		
Device-Specific Registers – General-Purpose Input/Output (Offsets 600h – 68Ch)	600h – 68Ch		
Device-Specific Registers – PORT_GOOD Selector (Offsets 6A0h – 6A8h)	6A0h – 6A8h		
Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)	700h – 75Ch	700h – 75Ch	724h, 728h
Device-Specific Registers – Control (Offsets 760h – 774h)	760h – 774h	760h – 774h	
Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)	778h – 8FCh	778h – 8FCh	
Device-Specific Registers – Ingress Credit Handler (Offsets 9ECh – A2Ch)	9ECh – A2Ch	9ECh – A2Ch	9FCh – A2Ch
Device-Specific Registers – Debug (Offsets A30h – A74h)	Upstream Port A30h – A74h		
Latency Tolerance Reporting Extended Capability Registers (Offsets B00h – B08h)	Upstream Port B00h – B08h		
Device-Specific Registers (Offsets B70h – DFCh)			
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)	B70h – B7Ch	B70h – B7Ch	B70h – B7Ch
Device-Specific Registers – Physical Layer (Offsets B80h – C88h)	B80h – C88h	B80h – C88h	
Multicast Extended Capability Registers (Offsets E00h – E2Ch)	E00h – E2Ch	E00h – E2Ch	E00h – E2Ch
ACS Extended Capability Registers (Offsets F24h – F2Ch)	Downstream Ports F24h – F2Ch		
Device-Specific Registers (Offsets F30h – FB0h)			
Device-Specific Registers – Egress Control (Offsets F30h – F44h)	F30h – F44h	F30h – F44h	F30h – F44h
Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)	F48h, F5Ch	F48h, F5Ch	F48h, F5Ch
	Upstream Port F4Ch – F58h, F60h		
Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)	F70h – FB0h	F70h – FB0h	F70h – FB0h
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)	FB4h – FDCh	FB4h – FDCh	FB4h – FDCh

a. Some Ports are used only within specific Port configurations. Refer to [Table 11-5](#) for details.

11.4 Register Access

Each PEX 8747 Port implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) comprise the PCI-compatible Configuration Space, and the upper 960 DWords (offsets 100h through FFFh) comprise the PCI Express Extended Configuration Space. The PEX 8747 supports six mechanisms for accessing the registers:

- [PCI r3.0-Compatible Configuration Mechanism](#)
- [PCI Express Enhanced Configuration Access Mechanism](#)
- [Device-Specific Memory-Mapped Configuration Mechanism](#)
- I²C Slave Interface (refer to [Section 7.2, “I2C Slave Interface”](#))
- SMBus Slave Interface (refer to [Section 7.3, “SMBus Slave Interface”](#))
- Serial Peripheral Interface (SPI) Bus (refer to [Chapter 6, “Serial EEPROM Controller”](#))

The sideband register access mechanisms (serial EEPROM, I²C, and/or SMBus) can modify Read-Only (RO) register values.

Each Port captures the Bus Number and Device Number on every Type 0 Configuration Write, as required by the *PCI r3.0*. Therefore, following a Fundamental Reset, software must initially perform a Configuration Write to each Port (using either the [PCI r3.0-Compatible Configuration Mechanism](#) or [PCI Express Enhanced Configuration Access Mechanism](#)), to allow each Port to capture its designated Bus Number and Device Number. The initial access to each Port, *for example*, could be a Configuration Write Request to a RO register, such as the **Device ID** / **Vendor ID** register (offset 00h).

Note: *An option is provided to allow the serial EEPROM and/or I²C/SMBus to initialize the Port's **Captured Bus and Device Numbers** registers (offset 1DCh), instead of the required initial Configuration Write to each Port; however, this option is not recommended.*

11.4.1 PCI r3.0-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PCI Express Configuration Space within each Port. PCI Express Configuration Request transactions use the following Addressing fields:

- *Bus Number*
- *Device Number*
- *Function Number*
- *Extended Register Number and Register Number*

Notes: *When an Alternative Routing-ID Interpretation (ARI) device is targeted, and the Downstream Port immediately above it is enabled for ARI Forwarding, the Device Number (in associated Routing IDs, Requester IDs, and Completer IDs) is implied to be 0, and the traditional 5-bit Device Number and 3-bit Function Number fields are interpreted as a single 8-bit Function Number field.*

For ARI devices, discovery and enumeration of Extended Functions require ARI-aware software.

Together, the *Extended Register Number* and *Register Number* fields specify the Configuration Space address of the register being accessed (concatenated such that the *Extended Register Number* forms the more-significant bits). For PCI-compatible Configuration Requests (that target the first 256 bytes of a Function's Configuration Space, the *Extended Register Address* field must be all zeros (0)). The PCI Express Extended Configuration Space (offsets 100h through FFFh) can be accessed by the [PCI Express Enhanced Configuration Access Mechanism](#) (ECAM), except for the register ranges noted in [Section 11.4.2](#), or [Device-Specific Memory-Mapped Configuration Mechanism](#), which can access all registers.

The *PCI r3.0-Compatible* Configuration mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8747 Configuration registers. Each Port can convert a Type 1 Configuration Request (destined to a Downstream Port or device) to a Type 0 Configuration Request (targeting the next Downstream Port or device), as described below.

The PEX 8747 decodes all Type 1 Configuration accesses received on its Upstream Port, when any of the following conditions are met:

- If the Bus Number in the Configuration access is not within the Upstream Port's Secondary Bus Number and Subordinate Bus Number range, the Upstream Port responds with an Unsupported Request (UR).
- Specified Bus Number in the Configuration access is the PEX 8747 internal virtual PCI Bus Number, the PEX 8747 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
 - If the specified device corresponds to the PCI-to-PCI bridge in one of the PEX 8747 Downstream Ports, the PEX 8747 processes the Read or Write Request to the specified Downstream Port register specified in the original Type 1 Configuration access.
 - If the specified Device Number does not correspond to any of the PEX 8747 Downstream Port Device Numbers, the PEX 8747 responds with a UR.
- If the specified Bus Number in the Type 1 Configuration access is not the PEX 8747 internal virtual PCI Bus Number, but is the Bus Number of one of the PEX 8747 Downstream Port secondary/subordinate buses, the PEX 8747 passes the Configuration access on to the PCI Express Link attached to that PEX 8747 Downstream Port.
 - If the specified Bus Number is the Downstream Port Secondary Bus Number, and the specified Device Number is 0, the PEX 8747 converts the Type 1 Configuration access to a Type 0 Configuration access before passing it on.
 - If the specified Device Number is not 0, the Downstream Port drops the Transaction Layer Packet (TLP) and generates a UR.
- If the specified Bus Number is not the Downstream Port Secondary Bus Number, the PEX 8747 passes along the Type 1 Configuration access, without change.

11.4.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism (ECAM) is implemented on all PCI Express PCs and on systems that do not implement a processor-specific firmware interface to the Configuration Space. The mechanism provides a Memory-Mapped Address space in the Root Complex, through which the Root Complex translates a Memory access into one or more Configuration Requests. Device drivers normally use an application programming interface (API) provided by the Operating System (OS), to use this mechanism.

The mechanism can be used to access PEX 8747 registers that are defined by Specifications. This mechanism *cannot*, however, access the Device-Specific registers (which are instead accessible by the Device-Specific Memory-Mapped Configuration Mechanism) in the following offset ranges, per Port:

- 200h through AFCh
- B0Ch through B6Ch
- B80h through C30h

Silicon Revision CA provides an option to enable ECAM access to all PEX 8747 registers, however, by Setting the **Station-Based Control** register *Device-Specific Register Access by Extended Configuration Request Enable* bit (Port 0, 8, or 16, offset 760h[16]), in the Station that contains the Upstream Port.

11.4.3 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the Configuration registers of all Ports, within a single 256-KB Memory map, as listed in [Table 11-3](#). The registers of each Port are contained within a 4-KB range. The PEX 8747 supports a maximum of up to five simultaneously active Ports.

This mechanism follows the *PCI Express Base r3.0* Configuration Request Routing rules, which do not allow the propagation of Configuration Requests from Downstream-to-Upstream, nor peer-to-peer. By default, if any PEX 8747 Downstream Port receives a Memory Request from a Downstream device targeting the PEX 8747 Configuration registers, the Port:

- Responds to a Memory Read Request with a Completion indicating an Unsupported Request (UR) Uncorrectable error
- For Memory Writes:
 - Silently discards a Memory Write Request (default, in compliance with the *PCI Express Base r2.1*), –or–
 - If the **ECC Error Check Disable** register *Software Force Error Enable* bit (Downstream Ports, offset 720h[2]) is Set, the Port responds with a UR

In Memory Requests that target PEX 8747 registers, the Payload Length indicated within the Memory Request Header must be 1 DWord. Lengths greater than 1 DWord result in a Completer Abort error.

To use this mechanism, program the Upstream Port Type 1 Configuration Space **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively), which are typically enumerated at boot time by BIOS or the OS software. After the PEX 8747 Upstream Port BARs are enumerated, Port 0 registers can be accessed with Memory Reads from and Writes to the first 4 KB (0000h to 0FFFh), Port 1 registers can be accessed with Memory Reads from and Writes to the second 4 KB (1000h to 1FFFh), and so forth. Within each of these 4-KB windows, individual registers are located at the DWord offsets indicated in [Table 11-1](#).

Table 11-3. Register Offsets from Upstream Port BAR0/1 Base Address

Port Number	Internal Register 4-KB Memory Space Range	Location Range
Port 0	0_0000h to 0_0FFFh	0 to 4 KB
Port 8	0_8000h to 0_8FFFh	32 to 36 KB
Port 9	0_9000h to 0_9FFFh	36 to 40 KB
Port 16	1_0000h to 1_0FFFh	64 to 68 KB
Port 17	1_1000h to 1_1FFFh	68 to 72 KB

11.5 Register Descriptions

The remainder of this chapter details the PEX 8747 registers, including:

- Bit/field names
- Description of register functions for the PEX 8747 Upstream Port and Downstream Ports
- Type (*such as* RW or HwInit; refer to [Table 11-4](#) for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8747 serial EEPROM and/or I²C/SMBus Initialization feature
- Default power-on/reset value

Table 11-4. Register Types, Grouped by User Accessibility

Type	Description
HwInit	Hardware-Initialized Refers to the PEX 8747 Hardware-Initialization mechanism or PEX 8747 Serial EEPROM and/or I ² C register Initialization features. RO after initialization and can only be reset with a Fundamental Reset. HwInit register bits are not modified by a Soft Reset.
RO	Read-Only Read-Only and cannot be altered by software. Permitted to be initialized by the PEX 8747 Hardware-Initialization mechanism or PEX 8747 serial EEPROM and/or I ² C/SMBus register Initialization features.
ROS	Read-Only, Sticky Same as RO, except that bits are neither initialized nor modified by a Soft Reset.
RsvdP	Reserved and Preserved <i>Reserved</i> for future RW implementations. Registers are RO and must return a value of 0 when read. Software must preserve value read for Writes to bits.
RsvdZ	Reserved and Zero <i>Reserved</i> for future RW1C implementations. Registers are RO and must return a value of 0 when read. Software must use 0 for Writes to bits.
RW	Read-Write Read/Write and permitted to be Set or Cleared by software to the needed state.
RW1C	Write 1 to Clear Status Indicates status when read. A status bit Set by the system (to indicate status) is Cleared, by writing 1 to that bit. Writing 0 has no effect.
RW1CS	Write 1 to Clear, Sticky Same as RW1C, except that bits are neither initialized nor modified by a Soft Reset.
RWS	Read-Write, Sticky Same as RW, except that bits are Set or Cleared by software to the needed state. Bits are neither initialized nor modified by a Soft Reset.
RZ	Software Read Zero Software Read always returns a value of 0; however, software is allowed to write this register.

11.6 Port Configurations and Station/Station Port/Port/ SerDes Module/Lane Relationship

This section discusses the PEX 8747 Port configurations, as well as information related to Stations, Station Ports, Ports, SerDes modules, and Lanes.

In this chapter, the term “SerDes quad” or “quad” refers to assembling SerDes modules into groups of four contiguous Lanes for testing purposes.

11.6.1 Port Configurations

Table 11-5 defines the PEX 8747 Port configurations, as well as the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes. For further details regarding Port configuration, refer to Section 4.4.1.1, “Port Configurations.”

Table 11-5. Port Configurations

# ^a	Fixed x16 Link Width	Port Configuration Register Value Port 0, Offset 300h[2:0]	Station 0 [Lanes/SerDes]/Port	
			Port 0 ^b	—
1	Station 0, Port 0 is always x16	001b	x16 [0-15]	
# ^a	Port Configuration Strapping Input States STRAP_STN1_PORTCFG0 ^c	Port Configuration Register Value Port 0, Offset 300h[5:3]	Station 1 [Lanes/SerDes]/Port	
			Port 8 ^b	Port 9
1	Z	001b	x16 [16-31]	
2	1	010b	x8 [16-23]	x8 [24-31]
# ^a	Port Configuration Strapping Input States STRAP_STN2_PORTCFG0 ^c	Port Configuration Register Value Port 0, Offset 300h[8:6]	Station 2 [Lanes/SerDes]/Port	
			Port 16 ^b	Port 17
1	Z	001b	x16 [32-47]	
2	1	010b	x8 [32-39]	x8 [40-47]

- Port Configuration Number, which is the decimal equivalent of the **Port Configuration** register Port Configuration for Station *x* field(s)' (Port 0, offset 300h[8:6, 5:3, and/or 2:0]) binary value.
- Ports 0, 8, and 16 are also “Station Ports” within their respective Stations. Station Ports are used to control the Station-specific registers.
- “Z” means “floating.” Z is used for the 3-state inputs that have three functions, depending upon whether the input is pulled or tied High to **VDD18**, pulled or tied Low to **VSS** (Ground), or left floating (not connected). Each one of these three input states (1, 0, or Z, respectively) results in a different function for that I/O input.

11.7 PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the PCI-Compatible Type 1 Configuration Header registers. [Table 11-6](#) defines the register map.

Table 11-6. PCI-Compatible Type 1 Configuration Header Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
Device ID																Vendor ID																00h
PCI Status																PCI Command																04h
PCI Class Code																		PCI Revision ID														08h
PCI BIST <i>(Not Supported)</i>								PCI Header Type								Master Latency Timer <i>(Not Supported)</i>								Cache Line Size								0Ch
Base Address 0																																10h
Base Address 1																																14h
Secondary Latency Timer <i>(Not Supported)</i>								Subordinate Bus Number								Secondary Bus Number								Primary Bus Number								18h
Secondary Status								<i>Not Supported/Reserved</i>								I/O Limit								I/O Base								1Ch
Memory Limit																Memory Base																20h
Prefetchable Memory Limit																Prefetchable Memory Base																24h
Prefetchable Memory Upper Base Address																																28h
Prefetchable Memory Upper Limit Address																																2Ch
I/O Limit Upper 16 Bits																I/O Base Upper 16 Bits																30h
<i>Reserved</i>																								Capability Pointer (40h)								34h
Expansion ROM Base Address <i>(Reserved)</i>																																38h
<i>Not Supported/Reserved</i>								Bridge Control								PCI Interrupt Pin								PCI Interrupt Line								3Ch

Register 11-1. 00h PCI Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	Vendor ID Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I ² C.	RO	Yes	10B5h
31:16	Device ID Identifies the particular device. Defaults to the PLX part number for the PEX 8747, if not overwritten by serial EEPROM and/or I ² C.	RO	Yes	8747h

**Register 11-2. 04h PCI Command/Status
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
PCI Command				
0	I/O Access Enable 0 = PEX 8747 ignores I/O Space accesses on the Port's primary interface 1 = PEX 8747 responds to I/O Space accesses on the Port's primary interface	RW	Yes	0
1	Memory Access Enable 0 = PEX 8747 ignores Memory Space accesses on the Port's primary interface 1 = PEX 8747 responds to Memory Space accesses on the Port's primary interface	RW	Yes	0
2	Bus Master Enable Controls PEX 8747 Memory and I/O Request forwarding Upstream. Does not affect Message (including INTx Interrupt Messages) forwarding nor Completions traveling Upstream or Downstream. 0 = PEX 8747 handles Memory and I/O Requests received on the Port's Downstream/secondary interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8747 returns a Completion with UR Completion status. Because MSI Messages are in-band Memory Writes, disables MSI Messages as well. 1 = PEX 8747 forwards Memory and I/O Requests Upstream.	RW	Yes	0
3	Special Cycle Enable <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
4	Memory Write and Invalidate Enable <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
5	VGA Palette Snoop <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
6	Parity Error Response Enable Controls bit 24 (<i>Master Data Parity Error Detected</i>).	RW	Yes	0
7	IDSEL Stepping/Wait Cycle Control <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0

**Register 11-2. 04h PCI Command/Status
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
8	SERR# Enable Controls bit 30 (<i>Signaled System Error</i>). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex, and, enables primary interface forwarding of ERR_FATAL and ERR_NONFATAL Messages from Downstream Ports and devices when the Port's Bridge Control register <i>SERR# Enable</i> bit (offset 3Ch[17]) is Set	RW	Yes	0
9	Fast Back-to-Back Transactions Enable <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
10	Interrupt Disable 0 = Port is enabled to generate INT _x Interrupt Messages and assert <i>PEX_INTA#</i> output 1 = Port is prevented from generating INT _x Interrupt Messages and asserting <i>PEX_INTA#</i> output	RW	Yes	0
15:11	<i>Reserved</i>	RsvdP	No	0-0h
PCI Status				
18:16	<i>Reserved</i>	RsvdP	No	000b
19	Interrupt Status 0 = No INT _x Interrupt Message is pending 1 = INT _x Interrupt Message is pending internally to the Port, –or– <i>PEX_INTA#</i> (if enabled) is asserted	RO	No	0
20	Capability List Capability function is supported. Set, as required by the <i>PCI Express Base r3.0</i> .	RO	Yes	1
21	66 MHz Capable Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
22	<i>Reserved</i>	RsvdP	No	0
23	Fast Back-to-Back Transactions Capable <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0

**Register 11-2. 04h PCI Command/Status
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
24	Master Data Parity Error Detected If bit 6 (<i>Parity Error Response Enable</i>) is Set, the Port Sets this bit when the Port: <ul style="list-style-type: none"> Forwards the poisoned TLP Write Request from the secondary to the primary interface, –or– Receives a Completion marked as poisoned on the primary interface If the <i>Parity Error Response Enable</i> bit is Cleared, the PEX 8747 never Sets this bit. This error is natively reported by the Uncorrectable Error Status register <i>Poisoned TLP Status</i> bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	DEVSEL# Timing <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	00b
27	Signaled Target Abort The Upstream Port Sets this bit when any one of the following conditions are met: <ul style="list-style-type: none"> Upstream Port receives a Memory Request targeting a PEX 8747 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord Upstream Port receives a Memory Request targeting a PEX 8747 register address within a non-existent Port Downstream Port Sets this bit if it detects an Access Control Services (ACS) violation This error is reported by the Uncorrectable Error Status register <i>Completer Abort Status</i> bit (offset FB8h[15]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
28	Received Target Abort <i>Reserved</i>	RsvdP	No	0
29	Received Master Abort <i>Reserved</i>	RsvdP	No	0
30	Signaled System Error If bit 8 (<i>SERR# Enable</i>) is Set, the Port Sets this bit when it transmits or forwards an ERR_FATAL or ERR_NONFATAL Message Upstream. This error is natively reported by the Device Status register <i>Fatal Error Detected</i> and <i>Non-Fatal Error Detected</i> bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	Detected Parity Error This error is natively reported by the Uncorrectable Error Status register <i>Poisoned TLP Status</i> bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = Port received a Poisoned TLP on its primary side, regardless of the bit 6 (<i>Parity Error Response Enable</i>) state	RW1C	Yes	0

**Register 11-3. 08h PCI Class Code and Revision ID
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
PCI Revision ID				
7:0	Revision ID Unless overwritten by the serial EEPROM, returns the Silicon Revision (BAh), the PLX-assigned Revision ID for this version of the PEX 8747. The PEX 8747 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	BAh
PCI Class Code				060400h
15:8	Register-Level Programming Interface The PEX 8747 Ports support the <i>PCI-to-PCI Bridge r1.2</i> requirements, but not subtractive decoding, on their Upstream interface.	RO	Yes	00h
23:16	Sub-Class Code PCI-to-PCI bridge.	RO	Yes	04h
31:24	Base Class Code Bridge device.	RO	Yes	06h

**Register 11-4. 0Ch Miscellaneous Control
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Cache Line Size				
7:0	Cache Line Size System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8747 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	Master Latency Timer <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	00h
PCI Header Type				
22:16	Configuration Layout Type The Port's Configuration Space Header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the <i>PCI-to-PCI Bridge r1.2</i> .	RO	No	01h
23	Multi-Function Device 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	PCI BIST <i>Not supported</i> Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

**Register 11-5. 10h Base Address 0
(Upstream Port)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
0	Memory Space Indicator 0 = Base Address register maps the PEX 8747 Configuration registers into Memory space <i>Note: The Upstream Port is hardwired to 0.</i>	Upstream	RO	No	0
	<i>Reserved</i>	Downstream	RsvdP	No	0
2:1	Memory Map Type 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are <i>Reserved</i> .	Upstream	RO	Yes	00b
	<i>Reserved</i>	Downstream	RsvdP	No	00b
3	Prefetchable 0 = Base Address register maps the PEX 8747 Configuration registers into Non-Prefetchable Memory space <i>Note: The Upstream Port is hardwired to 0.</i>	Upstream	RO	Yes	0
	<i>Reserved</i>	Downstream	RsvdP	No	0
17:4	<i>Reserved</i>		RsvdP	No	0-0h
31:18	Base Address 0 Base Address (BAR0) for the Device-Specific Memory-Mapped Configuration mechanism.	Upstream	RW	Yes	0-0h
	<i>Reserved</i>	Downstream	RsvdP	No	0-0h

**Register 11-6. 14h Base Address 1
(Upstream Port)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
31:0	Base Address 1 For 64-bit addressing, Base Address 1 (BAR1) extends Base Address 0 (BAR0) to provide the upper 32 Address bits when the Base Address 0 register <i>Memory Map Type</i> field (Upstream Port, offset 10h[2:1]) is programmed to 10b.	Upstream	RW	Yes	0000_0000h
	RO when the Base Address 0 register is not enabled as a 64-bit BAR (<i>Memory Map Type</i> field (Upstream Port, offset 10h[2:1]) is not programmed to 10b).		RO	Yes	0000_0000h
	<i>Reserved</i>	Downstream	RsvdP	No	0000_0000h

**Register 11-7. 18h Bus Number
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	Primary Bus Number Primary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment to which the primary interface of this Port is connected. Programmed by Configuration software.	RW	Yes	00h
15:8	Secondary Bus Number Secondary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment that is the secondary interface of this Port. Programmed by Configuration software.	RW	Yes	00h
23:16	Subordinate Bus Number Subordinate Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the highest numbered PCI Bus segment that is subordinate to this Port. Programmed by Configuration software.	RW	Yes	00h
31:24	Secondary Latency Timer <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	00h

Register 11-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>Note: If I/O Address decoding is enabled (PCI Command register I/O Access Enable bit, offset 04h[0], is Set), the Port forwards I/O transactions from the Port's primary interface to the Port's secondary interface (Downstream) if an I/O address is within the range defined by the I/O Base and I/O Limit registers when the Base is less than or equal to the Limit.</p> <p>Conversely, the Port forwards I/O transactions from the Port's secondary interface to the Port's primary interface (Upstream) if an I/O address is outside this Address range. If the Port does not implement an I/O Address range, the Port forwards all I/O transactions on the Port's secondary interface Upstream, to the Port's primary interface.</p>				
I/O Base				
3:0	I/O Base Addressing Capability 1h = 32-bit I/O Address decoding is supported All other encodings are Reserved .	RO	Yes	1h
7:4	I/O_BAR[15:12] I/O Base Address[15:12]. The Ports use their I/O Base and I/O Limit registers to determine the address range of I/O transactions to forward from one interface to the other. I/O Base Address[15:12] bits specify the Port's I/O Base Address[15:12]. The PEX 8747 assumes I/O Base Address[11:0]=000h. For 16-bit I/O addressing, the PEX 8747 assumes Address[31:16]=0000h. For 32-bit addressing, the PEX 8747 decodes Address[31:0], and uses the I/O Upper Base and Limit Address register I/O Base Upper 16 Bits and I/O Limit Upper 16 Bits fields (offset 30h[15:0 and 31:16], respectively).	RW	Yes	Fh
I/O Limit				
11:8	I/O Limit Addressing Capability 1h = 32-bit I/O Address decoding is supported All other encodings are Reserved .	RO	Yes	1h
15:12	I/O_Limit[15:12] I/O Limit Address[15:12]. The Ports use their I/O Base and I/O Limit registers to determine the Address range of I/O transactions to forward from one interface to the other. I/O Limit Address[15:12] bits specify the Port's I/O Limit Address[15:12]. The PEX 8747 assumes I/O Limit Address[11:0]=FFFh. For 16-bit I/O addressing, the PEX 8747 decodes Address bits [15:0] and assumes I/O Limit Address[31:16]=0000h. For 32-bit addressing, the PEX 8747 decodes Address bits [31:0], and uses the I/O Upper Base and Limit Address register I/O Base Upper 16 Bits and I/O Limit Upper 16 Bits fields (offset 30h[15:0 and 31:16], respectively).	RW	Yes	0h

**Register 11-8. 1Ch Secondary Status, I/O Limit, and I/O Base
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Secondary Status				
20:16	<i>Reserved</i>	RsvdP	No	0-0h
21	66 MHz Capable <i>Not supported</i> 0 = Not enabled, because PCI Express does <i>not support</i> 66 MHz	RsvdP	No	0
22	<i>Reserved</i>	RsvdP	No	0
23	Fast Back-to-Back Transactions Capable <i>Reserved</i> Not enabled, because PCI Express does <i>not support</i> this function.	RsvdP	No	0
24	Master Data Parity Error If the Bridge Control register <i>Parity Error Response Enable</i> bit (offset 3Ch[16]) is Set, the Port Sets this bit when transmitting or receiving a TLP on its Downstream side, and when either of the following two conditions occur: <ul style="list-style-type: none"> Port receives Completion marked poisoned Port forwards poisoned TLP Write Request If the <i>Parity Error Response Enable</i> bit is Cleared, the PEX 8747 never Sets this bit. These errors are reported by the Port's Uncorrectable Error Status register <i>Poisoned TLP Status</i> bit (offset FB8h[12]), and mirrored to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	DEVSEL# Timing <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	00b
27	Signaled Target Abort Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
28	Received Target Abort Cleared, as required by the <i>PCI Express Base r3.0</i> , because the PEX 8747 never initiates a Request itself.	RsvdP	No	0
29	Received Master Abort Cleared, as required by the <i>PCI Express Base r3.0</i> , because the PEX 8747 never initiates a Request itself.	RsvdP	No	0
30	Received System Error 1 = Downstream Port received an ERR_FATAL or ERR_NONFATAL Message on its secondary interface from a Downstream device	RW1C	Yes	0
31	Detected Parity Error 1 = Downstream Port received a poisoned TLP from a Downstream device (Set regardless of the Bridge Control register <i>Parity Error Response Enable</i> bit (offset 3Ch[16]) state)	RW1C	Yes	0

**Register 11-9. 20h Memory Base and Limit
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>Note: The Port forwards Memory transactions from its primary interface to its secondary interface (Downstream) if a Memory address is within the range defined by the Memory Base and Memory Limit registers (when the Base is less than or equal to the Limit).</p> <p>Conversely, the Port forwards Memory transactions from its secondary interface to its primary interface (Upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the Prefetchable Memory Base (offsets 28h + 24h[15:0]) and Prefetchable Memory Limit (offsets 2Ch + 24h[31:16]) registers).</p>				
Memory Base				
3:0	Reserved	RsvdP	No	0h
15:4	MEM_BAR[31:20] Memory Base Address[31:20]. Specifies the Port's Non-Prefetchable Memory Base Address[31:20]. The PEX 8747 assumes Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Memory Limit				
19:16	Reserved	RsvdP	No	0h
31:20	MEM_Limit[31:20] Memory Limit Address[31:20]. Specifies the Port's Non-Prefetchable Memory Limit Address[31:20]. The PEX 8747 assumes Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

**Register 11-10. 24h Prefetchable Memory Base and Limit
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>Note: The Port forwards Memory transactions from its primary interface to its secondary interface (Downstream) if a Memory address is within the range defined by the Prefetchable Memory Base (offsets 28h + 24h[15:0]) and Prefetchable Memory Limit (offsets 2Ch + 24h[31:16]) registers (when the Base is less than or equal to the Limit).</p> <p>Conversely, the Port forwards Memory transactions from its secondary interface to its primary interface (Upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the Memory Base and Memory Limit registers (offset 20h)).</p>				
Prefetchable Memory Base				
0	Prefetchable Memory Base Capability 0 = Port supports 32-bit Prefetchable Memory Addressing 1 = Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the <i>PCI Express Base r3.0</i> Note: If the application needs 32-bit only Prefetchable space, the serial EEPROM and/or I ² C must Clear both this bit and bit 16 (Prefetchable Memory Limit Capability).	RO	Yes	1
3:1	Reserved	RsvdP	No	000b
15:4	PMEM_BAR[31:20] Prefetchable Memory Base Address[31:20]. Specifies the Port's Prefetchable Memory Base Address[31:20]. The PEX 8747 assumes Prefetchable Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Prefetchable Memory Limit				
16	Prefetchable Memory Limit Capability 0 = Port supports 32-bit Prefetchable Memory Addressing 1 = Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the <i>PCI Express Base r3.0</i>	RO	Yes	1
19:17	Reserved	RsvdP	No	000b
31:20	PMEM_Limit[31:20] Prefetchable Memory Limit Address[31:20]. Specifies the Port's Prefetchable Memory Limit Address[31:20]. The PEX 8747 assumes Prefetchable Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

**Register 11-11. 28h Prefetchable Memory Upper Base Address
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default	
31:0	PBUP[63:32] Prefetchable Memory Base Address[63:32]. The PEX 8747 uses this register for Prefetchable Memory Upper Base Address[63:32].	Offset 24h[0]=1	RW	Yes	0000_0000h
	When the Prefetchable Memory Base register <i>Prefetchable Memory Base Capability</i> field indicates 32-bit addressing, this register is RO and returns a value of 0000_0000h.	Offset 24h[0]=0	RO	No	0000_0000h

**Register 11-12. 2Ch Prefetchable Memory Upper Limit Address
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default	
31:0	PLIMUP[63:32] Prefetchable Memory Limit Address[63:32]. The PEX 8747 uses this register for Prefetchable Memory Upper Limit Address[63:32]. When the Prefetchable Memory Limit register <i>Prefetchable Memory Limit Capability</i> field indicates 32-bit addressing, this register is RO and returns a value of 0000_0000h. <i>Note: The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.</i>	Offset 24h[16]=1	RW	Yes	0000_0000h
	Offset 24h[16]=0	RO	No	0000_0000h	

**Register 11-13. 30h I/O Upper Base and Limit Address
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default	
I/O Base Upper 16 Bits					
15:0	I/O Base Upper 16 Bits The PEX 8747 uses this register for I/O Base Address[31:16]. When the I/O Base register <i>I/O Base Addressing Capability</i> field indicates 16-bit addressing, this register is RO and returns a value of 0000h.	Offset 1Ch[3:0]=1h	RW	Yes	0000h
		Offset 1Ch[3:0]=0h	RO	No	0000h
I/O Limit Upper 16 Bits					
31:16	I/O Limit Upper 16 Bits The PEX 8747 uses this register for I/O Limit Address[31:16]. When the I/O Limit register <i>I/O Limit Addressing Capability</i> field indicates 16-bit addressing, this register is RO and returns a value of 0000h. <i>Note: The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.</i>	Offset 1Ch[11:8]=1h	RW	Yes	0000h
		Offset 1Ch[11:8]=0h	RO	No	0000h

**Register 11-14. 34h Capability Pointer
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	Capability Pointer Default 40h points to the PCI Power Management Capability structure.	RO	Yes	40h
31:8	<i>Reserved</i>	RsvdP	No	0000_00h

**Register 11-15. 38h Expansion ROM Base Address
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	Expansion ROM Base Address <i>Reserved</i>	RsvdP	No	0000_0000h

Register 11-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
PCI Interrupt Signal				
7:0	PCI Interrupt Line Interrupt line routing value. The PEX 8747 does <i>not</i> use this register; however, the register is included for operating system and device driver use.	RW	Yes	00h
15:8	PCI Interrupt Pin Identifies the Conventional PCI Interrupt Message(s) that the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8747. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
Bridge Control				
16	Parity Error Response Enable Controls the response to Poisoned TLPs. 0 = Disables the Port's Secondary Status register <i>Master Data Parity Error</i> bit (offset 1Ch[24]) 1 = Enables the Port's Secondary Status register <i>Master Data Parity Error</i> bit (offset 1Ch[24])	RW	Yes	0
17	SERR# Enable Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the Port's PCI Command register <i>SERR# Enable</i> bit (offset 04h[8]) is also Set, enables the Port's PCI Status register <i>Signaled System Error</i> bit (offset 04h[30]).	RW	Yes	0
18	ISA Enable Modifies the PEX 8747's response to Conventional PCI ISA I/O addresses enabled by the Port's I/O Base and I/O Limit registers (offset 1Ch[7:0 and 15:8], respectively) and located in the first 64 KB of the PCI I/O Address space (0000_0000h to 0000_FFFFh). 0 = Port's I/O Base and I/O Limit registers, and I/O Base Upper 16 Bits and I/O Limit Upper 16 Bits registers (offset 30h[15:0 and 31:16], respectively), define the Port's I/O Address range 1 = If the Port's I/O Address range (defined by the Port's I/O Base , I/O Limit , I/O Base Upper 16 Bits , I/O Limit Upper 16 Bits registers) includes I/O addresses below 64 KB, the upper 768 I/O addresses within each 1-KB block below 64 KB are excluded from the Port's I/O Address range <i>Note: Refer also to the Ingress Control register <i>Disable VGA BIOS Memory Access Decoding</i> bit (Upstream Port, offset F60h[28]).</i>	RW	Yes	0

**Register 11-16. 3Ch Bridge Control and PCI Interrupt Signal
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
19	<p>VGA Enable</p> <p>Modifies the bridge response to VGA-compatible addresses.</p> <p>When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface):</p> <ul style="list-style-type: none"> Memory addresses within the range 000A_0000h to 000B_FFFFh I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) <p>Additionally, when Set, forwarding of these addresses is independent of the:</p> <ul style="list-style-type: none"> Memory and I/O Address ranges defined by the bridge I/O Base, I/O Limit, Memory Base, Memory Limit, Prefetchable Memory Base, and Prefetchable Memory Limit registers Bit 18 (<i>ISA Enable</i>) Setting <p>VGA address forwarding is qualified by the Port's PCI Command register <i>Memory Access Enable</i> and <i>I/O Access Enable</i> bits (offset 04h[1:0], respectively). The default state of this bit after reset must be 0.</p> <p>0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges</p> <p>1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the <i>Memory Access Enable</i> and <i>I/O Access Enable</i> bits are Set), independent of the Memory and I/O Address ranges and independent of the <i>ISA Enable</i> bit</p> <p>Notes: When Set in an egress Port, the Port is configured as a non-Cut-Thru path. (Refer to Section 2.1.3.2, "Cut-Thru Mode," for further details.)</p> <p>Refer also to the Ingress Control register <i>Disable VGA BIOS Memory Access Decoding</i> bit (Upstream Port, offset F60h[28]).</p> <p>Conventional PCI VGA support – To avoid potential I/O address conflicts, if the VGA Enable bit is Set in the Upstream Port and a Downstream Port, Set the Port's PCI Command register <i>I/O Access Enable</i> bit (offset 04h[0]) in the remaining Downstream Ports, unless those Downstream Ports are configured to use default 32-bit address decoding and their I/O Address range is programmed above 1_0000h.</p>	RW	Yes	0

**Register 11-16. 3Ch Bridge Control and PCI Interrupt Signal
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
20	VGA 16-Bit Decode Enable Used only when bit 19 (<i>VGA Enable</i>) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses <i>Note:</i> Refer also to the <i>Ingress Control</i> register <i>Disable VGA BIOS Memory Access Decoding</i> bit (Upstream Port, offset F60h[28]).	RW	Yes	0
21	Master Abort Mode <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
22	Secondary Bus Reset 1 = Causes a Hot Reset on the Port's Downstream Link	RW	Yes	0
23	Fast Back-to-Back Transactions Enable <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
24	Primary Discard Timer <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
25	Secondary Discard Timer <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
26	Discard Timer Status <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
27	Discard Timer SERR# Enable <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
31:28	Reserved	RsvdP	No	0h

This section details the PCI Power Management Capability registers. [Table 11-7](#) defines the register map.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions <i>(Reserved)</i>	PCI Power Management Status and Control		44h

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	Capability ID Program to 01h, to indicate that the Capability structure is the PCI Power Management Capability structure.	RO	Yes	01h
15:8	Next Capability Pointer Default 48h points to the MSI Capability structure.	RO	Yes	48h
18:16	Version Default 011b indicates compliance with the <i>PCI Power Mgmt. r1.2</i> .	RO	Yes	011b
19	PME Clock Power Management Event (PME) clock. Does not apply to PCI Express. Returns a value of 0.	RsvdP	No	0
20	Reserved	RsvdP	No	0
21	Device-Specific Initialization 0 = Device-Specific Initialization is <i>not</i> required	RO	Yes	0
24:22	AUX Current The PEX 8747 does <i>not support</i> PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	D1 Support <i>Not supported</i> 0 = PEX 8747 does <i>not support</i> the D1 Device PM state	RsvdP	No	0
26	D2 Support <i>Not supported</i> 0 = PEX 8747 does <i>not support</i> the D2 Device PM state	RsvdP	No	0
31:27	PME Support Bits [31, 30, and 27] must be Set, to indicate that the PEX 8747 will forward PME Messages, as required by the <i>PCI Express Base r3.0</i> .	RO	Yes	19h

**Register 11-18. 44h PCI Power Management Status and Control
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
PCI Power Management Status and Control				
1:0	Power State Used to determine the Port's current Device PM state, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – <i>Not supported</i> 10b = D2 – <i>Not supported</i> 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	Reserved	RsvdP	No	0
3	No Soft Reset 1 = Devices transitioning from the D3hot to D0 state, because of Power State commands, do not perform an internal reset	ROS	Yes	1
7:4	Reserved	RsvdP	No	0h
8	PME Enable 0 = Disables PME generation by the Port ^a 1 = Enables PME generation by the Port	RWS	No	0
12:9	Data Select Initially writable by serial EEPROM and/or I ² C only ^b . This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I ² C Write occurs to this register. Selects the Port's field [14:13] (<i>Data Scale</i>) and PCI Power Management Data register <i>Data</i> field (offset 44h[31:24]). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are Reserved .	RO	Yes	0h
14:13	Data Scale Writable by serial EEPROM and/or I ² C only ^b . Indicates the scaling factor to be used when interpreting the PCI Power Management Data register <i>Data</i> field (offset 44h [31:24]) value. The value and meaning of the <i>Data Scale</i> field varies, depending upon which data value is selected by field [12:9] (<i>Data Select</i>). There are four internal <i>Data Scale</i> fields (one each, per <i>Data Select</i> values 0h, 3h, 4h, and 7h), per Port. For other <i>Data Select</i> values, the <i>Data Scale</i> value returned is 0h.	RO	Yes	00b
15	PME Status 0 = PME is not generated by the Port ^a 1 = PME is being generated by the Port	RW1CS	No	0

**Register 11-18. 44h PCI Power Management Status and Control
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	<i>Reserved</i>	RsvdP	No	0-0h
22	B2/B3 Support <i>Reserved</i> Cleared, as required by the <i>PCI Power Mgmt. r1.2</i> .	RsvdP	No	0
23	Bus Power/Clock Control Enable <i>Reserved</i> Cleared, as required by the <i>PCI Power Mgmt. r1.2</i> .	RsvdP	No	0
PCI Power Management Data				
31:24	Data Writable by serial EEPROM and/or I ² C only ^b . There are four supported <i>Data Select</i> values (0h, 3h, 4h, and 7h), per Port. For other <i>Data Select</i> values, the <i>Data</i> value returned is 00h. Selected by the Port's PCI Power Management Status and Control register <i>Data Select</i> field (offset 44h[12:9]).	RO	Yes	00h

- a. Because the PEX 8747 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.
- b. With no serial EEPROM nor previous I²C programming, Reads return a value of 00h for the **PCI Power Management Status and Control** register *Data Scale* and **PCI Power Management Data** register *Data* fields (for all *Data Selects*).

This section details the Message Signaled Interrupt (MSI) Capability registers. [Table 11-8](#) defines the register map.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

MSI Control	Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address			4Ch
MSI Upper Address			50h
<i>Reserved</i>	MSI Data		54h
<i>Reserved</i>		MSI Mask	58h
MSI Status			5Ch
<i>Reserved</i>			60h – 64h

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**Register 11-19. 48h MSI Capability
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
MSI Capability Header				
7:0	Capability ID Program to 05h, as required by the <i>PCI r3.0</i> .	RO	Yes	05h
15:8	Next Capability Pointer Program to 68h, to point to the PCI Express Capability structure.	RO	Yes	68h
MSI Control				
16	MSI Enable 0 = MSIs for the Port are disabled 1 = MSIs for the Port are enabled, and INTx Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	Multiple Message Capable 000b = Port can request only one MSI Vector 001b = Port can request two MSI Vectors 010b = Port can request four MSI Vectors All other encodings are <i>Reserved</i> .	RO	Yes	010b
22:20	Multiple Message Enable 000b = Port is allocated one MSI Vector, by default 001b = Port is allocated two MSI Vectors 010b = Port is allocated four MSI Vectors All other encodings are <i>Reserved</i> . <i>Note:</i> This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.	RW	Yes	000b
23	MSI 64-Bit Address Capable 0 = PEX 8747 is capable of generating MSI 32-bit addresses (Port's MSI Address register, offset 4Ch, is the Message address) 1 = PEX 8747 is capable of generating MSI 64-bit addresses (Port's MSI Address register, offset 4Ch, is the lower 32 bits of the Message address, and MSI Upper Address register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	Per Vector Masking Capable 0 = PEX 8747 does not have Per Vector Masking capability 1 = PEX 8747 has Per Vector Masking capability	RO	Yes	1
31:25	<i>Reserved</i>	RsvdP	No	0-0h

**Register 11-20. 4Ch MSI Address
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
1:0	<i>Reserved</i>	RsvdP	No	00b
31:2	Message Address <i>Note:</i> If the Port's MSI Control register MSI 64-Bit Address Capable bit (offset 48h[23]) is Set (default), refer to the Port's MSI Upper Address register for the MSI Upper Address (offset 50h).	RW	Yes	0-0h

**Register 11-21. 50h MSI Upper Address
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	Message Upper Address This register is valid/used only when the Port's MSI Control register MSI 64-Bit Address Capable bit (offset 48h[23]) is Set. MSI Write transaction upper address[63:32]. <i>Note:</i> Refer to register offset 4Ch for the MSI Address.	RW	Yes	0000_0000h

**Register 11-22. 54h MSI Data
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<i>Note:</i> The offset for this register changes from 54h, to 50h, when the Port's MSI Control register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.				
15:0	Message Data MSI Write transaction TLP payload.	RW	Yes	0000h
31:16	<i>Reserved</i>	RsvdP	No	0000h

**Register 11-23. 58h MSI Mask
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Port interrupt sources are grouped into three categories – Link State-/PM events, Device-Specific RAM ECC error events, and GPIO-generated interrupts.</p> <p>The quantity of MSI Vectors that are generated is determined by the Port's MSI Control register <i>Multiple Message Capable</i> and <i>Multiple Message Enable</i> fields (offset 48h[19:17 and 22:20], respectively):</p> <ul style="list-style-type: none"> • If one MSI Vector is enabled (default), all three interrupt events are combined into a single Vector • If two MSI Vectors are allocated, the individual Vectors indicate: <ul style="list-style-type: none"> – Vector[0] Link State-/PM-triggered interrupt event or GPIO-generated event – Vector[1] Device-specific RAM ECC error event • If four MSI Vectors are allocated (up to three Vectors are used), the individual Vectors indicate: <ul style="list-style-type: none"> – Vector[0] Link State-/PM-triggered interrupt event – Vector[1] Device-specific RAM ECC error event – Vector[2] GPIO-generated event – Vector[3] Reserved <p>Notes: The offset for this register changes from 58h, to 54h, when the Port's MSI Control register <i>MSI 64-Bit Address Capable</i> bit (offset 48h[23]) is Cleared.</p> <p>The bits in this register can be used to mask the Port's respective MSI Status register bits (offset 5Ch).</p>					
0	MSI Mask for Link State Events MSI mask for Power Management event- or Link State event-generated interrupts.	All Ports, when offset 48h[22:20]=001b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the MSI Control register <i>Multiple Message Enable</i> field indicates that the Host has allocated one Vector.	All Ports, when offset 48h[22:20]=000b	RW	Yes	0
1	Reserved		RsvdP	No	0
2	MSI Mask for GPIO-Generated Interrupts	Port 0, when offset 48h[22:20]=001b	RW	Yes	0
	Reserved	Otherwise, when offset 48h[22:20]=000b	RsvdP	No	0
3	Reserved		RW	Yes	0
5:3	Reserved		RsvdP	No	000b
7:6	Reserved		RW	Yes	00b
31:8	Reserved		RsvdP	No	0000_00h

**Register 11-24. 5Ch MSI Status
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Port interrupt sources are grouped into three categories – Link State-/PM events, Device-Specific RAM ECC error events, and GPIO-generated interrupts.</p> <p>The quantity of MSI Vectors that are generated is determined by the Port's MSI Control register <i>Multiple Message Capable</i> and <i>Multiple Message Enable</i> fields (offset 48h[19:17 and 22:20], respectively):</p> <ul style="list-style-type: none"> • If one MSI Vector is enabled (default), all three interrupt events are combined into a single Vector • If two MSI Vectors are allocated, the individual Vectors indicate: <ul style="list-style-type: none"> – Vector[0] Link State-/PM-triggered interrupt event or GPIO-generated event – Vector[1] Device-specific RAM ECC error event • If four MSI Vectors are allocated (up to three Vectors are used), the individual Vectors indicate: <ul style="list-style-type: none"> – Vector[0] Link State-/PM-triggered interrupt event – Vector[1] Device-specific RAM ECC error event – Vector[2] GPIO-generated event – Vector[3] Reserved <p>Notes: The offset for this register changes from 5Ch, to 58h, when the Port's MSI Control register <i>MSI 64-Bit Address Capable</i> bit (offset 48h[23]) is Cleared.</p> <p>The bits in this register can be masked by the Port's respective MSI Mask register bits (offset 58h).</p>					
0	MSI Pending Status for Link State Events MSI pending status for Power Management event- or Link State event-generated interrupts.	All Ports, when offset 48h[22:20]=001b	RO	No	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for all interrupt sources when the MSI Control register <i>Multiple Message Enable</i> field indicates that the Host has allocated one Vector.	All Ports, when offset 48h[22:20]=000b	RsvdP	No	0
1	Reserved		RsvdP	No	0
2	MSI Pending Status for GPIO-Generated Interrupts	Port 0, when offset 48h[22:20]=001b	RO	No	0
	Reserved	Otherwise, when offset 48h[22:20]=000b	RsvdP	No	0
3	Reserved		RW	Yes	0
31:3	Reserved		RsvdP	No	0-0h

11.10 PCI Express Capability Registers (Offsets 68h – A0h)

This section details the PCI Express Capability registers. Hot Plug Capability, Command, Status, and Events are included in these registers. [Table 11-9](#) defines the register map.

Table 11-9. PCI Express Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																															
PCI Express Capability																Next Capability Pointer (A4h)																Capability ID (10h)																68h															
Device Capability																																																6Ch															
Device Status																Reserved/Not supported																Device Control																70h															
Link Capability																																																74h															
Link Status																Link Control																																78h															
Reserved (Upstream) Slot Capability (Downstream)																																																7Ch															
Reserved (Upstream)																																																80h															
Slot Status (Downstream)																Slot Control (Downstream)																																84h – 88h															
Reserved																																																8Ch															
Device Capability 2																																																90h															
Device Status 2 (Reserved)																Device Control 2																																94h															
Link Capability 2																																																98h															
Link Status 2																Link Control 2																																9Ch – A0h															
Reserved																																																A0h															

Register 11-25. 68h PCI Express Capability List and Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
PCI Express Capability List					
7:0	Capability ID Program to 10h, as required by the <i>PCI Express Base r3.0</i> .		RO	Yes	10h
15:8	Next Capability Pointer Program to A4h, to point to the Subsystem Capability structure.		RO	Yes	A4h
PCI Express Capability					
19:16	Capability Version The PEX 8747 Ports program this field to 2h, as required by the <i>PCI Express Base r3.0</i> .		RO	Yes	2h
23:20	Device/Port Type Set at reset, as required by the <i>PCI Express Base r3.0</i> .	Upstream	RO	Yes	5h
		Downstream	RO	Yes	6h
24	Slot Implemented 0 = Disables or connects to the Upstream Port	Upstream	RsvdP	No	0
	0 = Disables or connects to an integrated component 1 = Indicates that the Downstream Port connects to a slot, as opposed to being connected to an integrated component or being disabled <i>Note: The PEX 8747 serial EEPROM register Initialization capability, and/or I²C/SMBus when STRAP_I2C_SMBUS_CFG_EN#=L, can be used to Clear this bit, indicating that the Downstream Port connects to an integrated component or is disabled.</i>	Downstream	ROS	Yes	1
29:25	Interrupt Message Number The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.		RO	Yes	00_000b
31:30	Reserved		RsvdP	No	00b

**Register 11-26. 6Ch Device Capability
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
2:0	Maximum Payload Size Supported <i>Note: The default Maximum Payload Size supported is based upon the STRAP_STNx_PORTCFG0 3-state inputs. If the serial EEPROM or I²C/SMBus changes the Port configuration (from the strapped value), it must also program the value of this field, accordingly (with the value dependent upon the Station having the most enabled Ports).</i> 000b = Port supports a 128-byte maximum payload 001b = Port supports a 256-byte maximum payload 010b = Port supports a 512-byte maximum payload 011b = Port supports a 1,024-byte maximum payload 100b = Port supports a 2,048-byte maximum payload (default) No other encodings are supported.		HwInit	Yes	100b
4:3	Phantom Functions Supported <i>Not supported</i>		RO	Yes	00b
5	Extended Tag Field Supported 0 = Maximum <i>Tag</i> field is 5 bits 1 = Maximum <i>Tag</i> field is 8 bits		RO	Yes	0
8:6	Endpoint L0s Acceptable Latency <i>Not supported</i> Because the PEX 8747 is a switch and not an endpoint, the PEX 8747 does not support this feature. 000b = Disables the capability		RO	Yes	000b
11:9	Endpoint L1 Acceptable Latency <i>Not supported</i> Because the PEX 8747 is a switch and not an endpoint, the PEX 8747 does not support this feature. 000b = Disables the capability		RO	Yes	000b
14:12	Reserved , as required by the <i>PCI Express Base r3.0</i> .		RsvdP	No	000b
15	Role-Based Error Reporting		RO	Yes	1

**Register 11-26. 6Ch Device Capability
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
17:16	<i>Reserved</i>		RsvdP	No	00b
25:18	Captured Slot Power Limit Value For Upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (<i>Captured Slot Power Limit Scale</i>).	Upstream	RO	Yes	00h
	<i>Not valid</i>	Downstream	RsvdP	No	00h
27:26	Captured Slot Power Limit Scale For Upstream Port, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (<i>Captured Slot Power Limit Value</i>). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	Upstream	RO	Yes	00b
	<i>Not valid</i>	Downstream	RsvdP	No	00b
31:28	<i>Reserved</i>		RsvdP	No	0h

**Register 11-27. 70h Device Status and Control
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Device Control				
0	Correctable Error Reporting Enable 0 = Disables 1 = Enables the Port to report Correctable errors	RW	Yes	0
1	Non-Fatal Error Reporting Enable 0 = Disables 1 = Enables the Port to report Non-Fatal errors	RW	Yes	0
2	Fatal Error Reporting Enable 0 = Disables 1 = Enables the Port to report Fatal errors	RW	Yes	0
3	Unsupported Request Reporting Enable 0 = Disables 1 = Enables the Port to report UR errors	RW	Yes	0
4	Enable Relaxed Ordering <i>Not supported</i> The value of this bit has no effect upon internal logic.	RW	Yes	1
7:5	Maximum Payload Size Software can change this field to configure the Ports to support other Payload Sizes; however, software cannot change this field to a value larger than that indicated by the Device Capability register <i>Maximum Payload Size Supported</i> field (offset 6Ch[2:0]). 000b = Port supports a 128-byte maximum payload 001b = Port supports a 256-byte maximum payload 010b = Port supports a 512-byte maximum payload 011b = Port supports a 1,024-byte maximum payload 100b = Port supports a 2,048-byte maximum payload No other encodings are supported.	RW	Yes	000b
8	Extended Tag Field Enable <i>Not supported</i>	RsvdP	No	0
9	Phantom Functions Enable <i>Not supported</i>	RsvdP	No	0
10	AUX Power PM Enable <i>Not supported</i>	RsvdP	No	0
11	Enable No Snoop <i>Not supported</i>	RW	Yes	1
14:12	Max Read Request Size <i>Not supported</i>	RsvdP	No	000b
15	Reserved Hardwired to 0, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0

**Register 11-27. 70h Device Status and Control
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Device Status				
16	Correctable Error Detected 0 = Port did not detect a Correctable error 1 = Port detected a Correctable error, regardless of the bit 0 (<i>Correctable Error Reporting Enable</i>) state	RW1C	Yes	0
17	Non-Fatal Error Detected 0 = Port did not detect a Non-Fatal error 1 = Port detected a Non-Fatal error, regardless of the bit 1 (<i>Non-Fatal Error Reporting Enable</i>) state	RW1C	Yes	0
18	Fatal Error Detected 0 = Port did not detect a Fatal error 1 = Port detected a Fatal error, regardless of the bit 2 (<i>Fatal Error Reporting Enable</i>) state	RW1C	Yes	0
19	Unsupported Request Detected 0 = Port did not detect a UR 1 = Port detected a UR, regardless of the bit 3 (<i>Unsupported Request Reporting Enable</i>) state	RW1C	Yes	0
20	AUX Power Detected <i>Not supported</i>	RsvdP	No	0
21	Transactions Pending <i>Not supported</i> Cleared, as required by the <i>PCI Express Base r3.0</i> .	RsvdP	No	0
31:22	Reserved	RsvdP	No	0-0h

**Register 11-28. 74h Link Capability
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Note: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Ports and Lanes (Link widths).					
3:0	Maximum Link Speed Indicates the Port's maximum Link speed. The encoding is the binary value of the bit location in the Port's Link Capability 2 register <i>Supported Link Speeds Vector</i> field (offset 94h[7:1]) that corresponds to the maximum Link speed. <i>For example</i> , the default value 3h indicates that the maximum Link speed is that which corresponds to bit 3 in the <i>Supported Link Speeds Vector</i> field, which is 8.0 GT/s. The default value for all Ports can be globally changed to 2h (Gen 2 maximum speed) or 1h (Gen 1 maximum speed), according to the STRAP_GEN1_GEN2 input state (Z = 2h (Gen 2), or 0 = 1h (Gen 1)).		RO	Yes	3h
9:4	Maximum Link Width The PEX 8747 maximum Link width is x16 = 01_0000b. Actual maximum Link width is defined by the STRAP_STNx_PORTCFG0 3-state inputs. 00_0000b = Reserved 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are not supported .		ROS	No	Defined by STRAP_STNx_PORTCFG0 input states, or programmed by serial EEPROM value for the Port Configuration -related register (Port 0, offset 300h)
11:10	Active State Power Management (ASPM) Support Active State Link PM support. Indicates the level of ASPM supported by the Port. 00b = No ASPM support 01b = L0s Link PM state is supported 10b = L1 Link PM state is supported 11b = L0s and L1 Link PM states are supported		RO	Yes	11b

**Register 11-28. 74h Link Capability
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
14:12	<p>L0s Exit Latency</p> <p>Indicates the L0s Link PM state exit latency for the Port's PCI Express Link. The value reported indicates the length of time this Port requires to complete the L0s to L0 Link PM state transition.</p> <p>If L0s is not supported, the value of this field is undefined; however, for the recommended value, refer to the Implementation Note in the <i>PCI Express Base r3.0</i>, Section 5.4.1.1, "Potential Issues with Legacy Software When L0s is Not Supported."</p> <p>000b = Less than 64 ns 001b = 64 ns to less than 128 ns 010b = 128 ns to less than 256 ns 011b = 256 ns to less than 512 ns 100b = 512 ns to less than 1 μs 101b = 1 μs to less than 2 μs 110b = 2 to 4 μs (default) 111b = More than 4 μs</p>		RO	No	110b

**Register 11-28. 74h Link Capability
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
17:15	L1 Exit Latency Indicates the L1 Link PM state exit latency for the Port's PCI Express Link. The value reported indicates the length of time that this Port requires to complete the ASPM L1 to L0 Link PM state transition. If L0 is not supported, the value of this field is undefined. 000b = Less than 1 μ s 001b = 1 μ s to less than 2 μ s (5.0 GT/s) 010b = 2 μ s to less than 4 μ s (default, 2.5 GT/s) 011b = 4 μ s to less than 8 μ s 100b = 8 μ s to less than 16 μ s 101b = 16 μ s to less than 32 μ s 110b = 32 to 64 μ s 111b = More than 64 μ s		RO	Yes	010b
18	Clock Power Management Capable <i>Not supported</i>	Upstream	RO	Yes	0
	<i>Not supported</i> Must be hardwired to 0.	Downstream	RO	No	0
19	Reserved Must be hardwired to 0, for Upstream Port and components that do not support this optional capability.	Upstream	RsvdP	No	0
	Surprise Down Error Reporting Capable Must be Set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. If this bit is Cleared, the Port's Uncorrectable Error Status register <i>Surprise Down Error Status</i> bit (Downstream Ports, offset FB8h[5]) is disabled.	Downstream	RO	Yes	1

**Register 11-28. 74h Link Capability
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
20	<i>Reserved</i>	Upstream	RsvdP	No	0
	Data Link Layer Link Active Reporting Capable	Downstream	RO	Yes	1
21	<i>Reserved</i> Hardwired to 0, as required by the <i>PCI Express Base r3.0</i> .	Upstream	RsvdP	No	0
	Link Bandwidth Notification Capability 1 = Indicates support for the Link Bandwidth Notification status and interrupt mechanisms	Downstream	RO	Yes	1
22	ASPM Optionality Compliance		HwInit	Yes	1
23	<i>Reserved</i>		RsvdP	No	0
31:24	Port Number The Port Number is defined by 3-state input Strapping options. <i>Note: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i> Station 0 – Port 0 (always enabled) Station 1, STRAP_STN1_PORTCFG0 – Ports 8, 9 Station 2STRAP_STN2_PORTCFG0 – Ports 16, 17		ROS	Yes	Defined by STRAP_STNx_PORTCFG0 input states, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station x</i> field(s) (Port 0, offset 300h[8:6, 5:3, and/or 2:0])

**Register 11-29. 78h Link Status and Control
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Link Control					
1:0	Active State Power Management (ASPM) 00b = Disable ^a 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries		RW	Yes	00b
2	<i>Reserved</i>		RsvdP	No	0
3	Read Request Return Parameter Control Read Request Return Parameter “R” control. Read Completion Boundary (RCB). Cleared, as required by the <i>PCI Express Base r3.0</i> .		RO	Yes	0

**Register 11-29. 78h Link Status and Control
(All Ports) (Cont.)**

Bit(s)	Description		Ports	Type	Serial EEPROM and I ² C	Default
4	<i>Not valid</i>	Offset F70h[29]=0	Upstream	RsvdP	No	0
	Link Disable Functionality is enabled when the Port's Power Management Hot Plug User Configuration register <i>PHY Upstream Port Control Write Enable</i> bit (offset F70h[29]) is Set. 1 = Places the Upstream Port's Link into the <i>Disabled</i> Link Training state	Offset F70h[29]=1	Upstream	RW	Yes	0
	1 = Places the Downstream Port's Link into the <i>Disabled</i> Link Training state		Downstream	RW	Yes	0
5	<i>Not valid</i> Always read as 0.	Offset F70h[29]=0	Upstream	RsvdP	No	0
	Retrain Link Functionality is enabled when the Port's Power Management Hot Plug User Configuration register <i>PHY Upstream Port Control Write Enable</i> bit (offset F70h[29]) is Set. Always returns a value of 0 when read; however, software is allowed to write this register. Writing 1 to this bit causes the Upstream Port to initiate retraining of its PCI Express Link.	Offset F70h[29]=1	Upstream	RZ	Yes	0
	Always returns a value of 0 when read; however, software is allowed to write this register. Writing 1 to this bit causes the Downstream Port to initiate retraining of its PCI Express Link.		Downstream	RZ	Yes	0
6	Common Clock Configuration 0 = Port and the device at the other end of the Port's PCI Express Link use an asynchronous Reference Clock source 1 = Port and the device at the other end of the Port's PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)			RW	Yes	0
7	Extended Sync Setting this bit causes the Port to transmit: <ul style="list-style-type: none">• 4,096 FTS Ordered-Sets in the L0s Link PM state,• Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state,• Finally, transmission of 1,024 TS1 Ordered-Sets in the <i>Recovery</i> state.			RW	Yes	0

Register 11-29. 78h Link Status and Control
(All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
8	Clock Power Management Enable <i>Not supported</i>		RsvdP	No	0
9	Hardware-Autonomous Width Disable <i>Reserved</i>		RsvdP	No	0
10	<i>Reserved</i>	Upstream	RsvdP	No	0
	Link Bandwidth Management Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the Port's Link Status register Link Bandwidth Management Status bit (Downstream Ports, offset 78h[30]) has been Set	Downstream	RW	Yes	0
11	<i>Reserved</i>	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the Port's Link Status register Link Autonomous Bandwidth Status bit (Downstream Ports, offset 78h[31]) has been Set	Downstream	RW	Yes	0
15:12	<i>Reserved</i>		RsvdP	No	0h
Link Status					
19:16	Current Link Speed Indicates the negotiated Link speed of the Port's PCI Express Link. The encoding is the binary value of the bit location in the Port's Link Capability 2 register Supported Link Speeds Vector field (offset 94h[7:1]) that corresponds to the current Link speed. <i>For example</i> , a value of 1h indicates that the current Link speed is that which corresponds to bit 1 in the Supported Link Speeds Vector field, which is 2.5 GT/s. If the Link is not up, the value of this field is undefined.		RO	No	1h
25:20	Negotiated Link Width Dependent upon the physical Port configuration. Link width is determined by the negotiated value with the attached Lane/Port. If the Link is not up, the value of this field is undefined. 00_0000b = Link is Down (default) 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are <i>not supported</i> .		RO	No	00_0000b
26	<i>Reserved</i>		RsvdP	No	0
27	<i>Reserved</i>	Upstream	RsvdP	No	0
	Link Training 1 = Indicates that the Downstream Port requested Link training, and the Link training is in-progress or about to start	Downstream	RO	No	0

**Register 11-29. 78h Link Status and Control
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
28	Slot Clock Configuration 0 = Indicates that the PEX 8747 uses an independent clock 1 = Indicates that the PEX 8747 uses the same physical Reference Clock that the platform provides on the connector		HwInit	Yes	0
29	<i>Reserved</i>	Upstream	RsvdP	No	0
	Data Link Layer Link Active When Set, and the Port's Link Capability register <i>Data Link Layer Link Active Reporting Capable</i> bit (Downstream Ports, offset 74h[20]) is also Set, indicates the following: <ul style="list-style-type: none"> Data Link Layer (DLL) is in the <i>DL_Active</i> state Link is operational Flow Control (FC) Initialization has successfully completed 	Downstream	RO	Yes	0
30	<i>Reserved</i>	Upstream	RsvdP	No	0
	Link Bandwidth Management Status Set by hardware to indicate that either of the following has occurred, without the Port transitioning through DL_Down status: <ul style="list-style-type: none"> Link retraining has completed following a Write of 1 to the Port's Link Control register <i>Retrain Link</i> bit (Downstream Ports, offset 78h[5]) Hardware has changed Link speed or width, to attempt to correct unreliable Link operation, either through an Link Training and Status State Machine (LTSSM) timeout or higher-level process 	Downstream	RW1C	Yes	0
31	<i>Reserved</i>	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Status Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.	Downstream	RW1C	Yes	0

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

**Register 11-30. 7Ch Slot Capability
(Downstream Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
6:0	<i>Reserved</i>		RsvdP	No	0-0h
14:7	<i>Reserved</i>	Upstream	RsvdP	No	00h
	Slot Power Limit Value The maximum power supplied by the corresponding PEX 8747 Downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the field [16:15] (<i>Slot Power Limit Scale</i>) value. This field must be implemented if the PCI Express Capability register <i>Slot Implemented</i> bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I ² C Writes to this register or a DLL Up event causes the Downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the Downstream device's Upstream Port Device Capability register <i>Captured Slot Power Limit Value</i> and <i>Captured Slot Power Limit Scale</i> fields.	Downstream	RO	Yes	19h
16:15	<i>Reserved</i>	Upstream	RsvdP	No	00b
	Slot Power Limit Scale The maximum power supplied by the corresponding PEX 8747 Downstream slot is determined by multiplying the value in this field by the field [14:7] (<i>Slot Power Limit Value</i>) value. This field must be implemented if the PCI Express Capability register <i>Slot Implemented</i> bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I ² C Writes to this register or a DLL Up event causes the Downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the Downstream device's Upstream Port Device Capability register <i>Captured Slot Power Limit Value</i> and <i>Captured Slot Power Limit Scale</i> fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Downstream	RO	Yes	00b
18:17	<i>Reserved</i>		RsvdP	No	00b

**Register 11-30. 7Ch Slot Capability
(Downstream Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default	
31:19	<i>Reserved</i>	Upstream	RsvdP	No	0-0h	
	Physical Slot Number Indicates the physical Slot Number attached to this Port. If the PCI Express Capability register <i>Slot Implemented</i> bit (offset 68h[24]) is Set (default), this field must be hardware-initialized to a value that assigns a Slot Number that is unique within the chassis, regardless of the form factor associated with the slot. Must be initialized to 0h for Ports connected to devices that are integrated on the system board.		Downstream	HwInit	Yes	0-0h
	Bit(s)	Description/Function				
	23:19	Port Numbers 0, 8, 9, 16, and 17				
	25:24	I2C_ADDR0 input binary value (input state 0, Z, or 1 is converted to binary value 00b, 01b, or 10b, respectively)				
	31:26	0000_00b				

**Register 11-31. 80h Slot Status and Control
(Downstream Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Slot Control					
2:0	<i>Reserved</i>		RsvdP	No	000b
3	<i>Not valid</i>	Upstream	RsvdP	No	0
	Presence Detect Changed Enable A Presence Detect Changed event is triggered by the Downstream Port's SerDes Receiver Detect (Physical Layer Receiver Detect Status register <i>Receiver Detected on Lane x</i> bits (Port 0, 8, or 16, offset 200h[31:16])). 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 state (Port's PCI Power Management Status and Control register <i>Power State</i> field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot state (the <i>Power State</i> field bits are both Set), for a Presence Detect Changed event on the Downstream Port	Downstream	RW	Yes	0
4	<i>Reserved</i>		RsvdP	No	0
5	<i>Reserved</i>	Upstream	RsvdP	No	0
	Hot Plug Interrupt Enable 0 = Function is disabled 1 = Enables an interrupt on enabled Link State events for the Downstream Port	Downstream	RW	Yes	0
11:6	<i>Reserved</i>		RsvdP	No	0-0h
12	<i>Not valid</i>	Upstream	RsvdP	No	0
	Data Link Layer State Changed Enable Enables software notification with an interrupt if the Port is in the D0 state (Port's PCI Power Management Status and Control register <i>Power State</i> field, offset 44h[1:0], is Cleared), or with a PME Message if the Port is in the D3hot state (the <i>Power State</i> field bits are both Set), when the Port's Link Status register <i>Data Link Layer Link Active</i> bit (Downstream Ports, offset 78h[29]) is changed.	Downstream	RW	Yes	0
15:13	<i>Reserved</i>		RsvdP	No	000b

**Register 11-31. 80h Slot Status and Control
(Downstream Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Slot Status					
18:16	<i>Reserved</i>		RsvdP	No	000b
19	<i>Reserved</i>	Upstream	RsvdP	No	0
	Presence Detect Changed A Presence Detect Changed event is triggered by the Downstream Port's SerDes Receiver Detect (Physical Layer Receiver Detect Status register <i>Receiver Detected on Lane x</i> bits (Port 0, 8, or 16, offset 200h[31:16])). Write 1 to Clear. 1 = Value reported in bit 22 (<i>Presence Detect State</i>) changed	Downstream	RW1C	Yes	0
21:20	<i>Reserved</i>		RsvdP	No	00b
22	<i>Not valid</i>	Upstream	RsvdP	No	0
	Presence Detect State For Downstream Ports that implement slots, indicates the presence of an adapter in the slot, reflected by the logical OR of the Downstream Port's SerDes Receiver Detect (Physical Layer Receiver Detect Status register <i>Receiver Detected on Lane x</i> bits (Port 0, 8, or 16, offset 200h[31:16])). Hardwired to 1 when the PCI Express Capability register <i>Slot Implemented</i> bit (offset 68h[24]) value is 0. 0 = Slot is empty, or device is not present 1 = Slot is occupied, or device is present	Offset 68h[24]=1 Downstream	RO	No	0
		Offset 68h[24]=0 Downstream	RO	No	1
23	<i>Reserved</i>		RsvdZ	No	0
24	<i>Not valid</i>	Upstream	RsvdP	No	0
	Data Link Layer State Changed In response to a Data Link Layer State Changed event, software must read the Port's Link Status register <i>Data Link Layer Link Active</i> bit (Downstream Ports, offset 78h[29]), to determine whether the Link is active before initiating Configuration Requests to the device. 1 = Value reported in the Link Status register <i>Data Link Layer Link Active</i> bit changed	Downstream	RW1C	Yes	0
31:25	<i>Reserved</i>		RsvdZ	No	0-0h

**Register 11-32. 8Ch Device Capability 2
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
4:0	<i>Reserved</i>		RsvdP	No	0-0h
5	<i>Reserved</i>	Upstream	RsvdP	No	0
	ARI Forwarding Supported 0 = Alternative Routing-ID Interpretation (ARI) forwarding is not supported 1 = ARI forwarding is supported	Downstream	RO	Yes	1
6	AtomicOp Routing Supported		RO	Yes	1
10:7	<i>Reserved</i>		RsvdP	No	0h
11	LTR Mechanism Supported 0 = Latency Tolerance Reporting (LTR) mechanism is not supported 1 = LTR mechanism is supported		RO	Yes	1
17:12	<i>Reserved</i>		RsvdP	No	0-0h
18	OBFF Mechanism Supported Bit 0 Indicates whether the Optimized Buffer Flush/Fill (OBFF) mechanism is supported. 0 = OBFF is not supported 1 = OBFF is supported, using Message signaling only		RO	Yes	1
31:19	<i>Reserved</i>		RsvdP	No	0-0h

**Register 11-33. 90h Device Status and Control 2
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Device Control 2					
4:0	<i>Reserved</i>		RsvdP	No	0-0h
5	<i>Reserved</i>	Upstream	RsvdP	No	0
	ARI Forwarding Enable 0 = Disabled 1 = Enabled; Downstream Port disables its traditional Device Number field from being forced to 0 when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to extended functions in an ARI device immediately below the Port	Downstream	RW	Yes	0
6	<i>Reserved</i>		RsvdP	No	0
7	AtomicOp Egress Blocking		RW	Yes	0
9:8	<i>Reserved</i>		RsvdP	No	00b
10	LTR Mechanism Enable 0 = Disables LTR mechanism 1 = Enables LTR mechanism		RW	Yes	0
12:11	<i>Reserved</i>		RsvdP	No	00b
14:13	OBFF Enable 00b = Disabled 01b = Enabled using Message Signaling [Variation A] 10b = Enabled using Message Signaling [Variation B] 11b = <i>Reserved</i>		RW	Yes	00b
15	<i>Reserved</i>		RsvdP	No	0
Device Status 2					
31:16	<i>Reserved</i>		RsvdP	No	0000h

**Register 11-34. 94h Link Capability 2
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default	
0	<i>Reserved</i>	RsvdP	No	0	
7:1	Supported Link Speeds Vector Supports 2.5, 5.0, and 8.0 GT/s Link speeds. Indicates the supported Link speed(s) of the associated Port. For each bit, a value of 1 indicates that the corresponding Link speed is supported; otherwise, the Link speed is <i>not supported</i> .	RO	Yes	07h	
	Bit(s)				Description/Function
	1				2.5 GT/s (Gen 1)
	2				5.0 GT/s (Gen 2)
	3				8.0 GT/s (Gen 3)
	7:4				<i>Reserved</i>
8	Cross-Link Supported 0 (Ports that support Link speeds of 8.0 GT/s or higher) = Indicates that the associated Port does not support cross-links 0 (Ports that support only Link speeds of 2.5 or 5.0 GT/s) = Does not provide information regarding the Port’s level of cross-link support 1 = Indicates that the associated Port supports cross-links <i>Notes: It is recommended that this bit be Set in any Port that supports cross-links, even though doing so is only required for Ports that also support operating at 8.0 GT/s or higher Link speeds.</i> <i>Software should use this bit when referencing fields whose definition depends upon whether the Port supports cross-links.</i>	RO	Yes	1	
31:9	<i>Reserved</i>	RsvdP	No	0-0h	

**Register 11-35. 98h Link Status and Control 2
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Link Control 2					
3:0	Target Link Speed Sets the Target Compliance mode speed when software is using bit 4 (<i>Enter Compliance</i>) to force a Link into Compliance mode.	Upstream	RWS	Yes	3h
	Sets an upper limit on Link operational speed, by restricting the values advertised by the Upstream component in its training sequences. Also Sets the Target Compliance mode speed when software is using bit 4 (<i>Enter Compliance</i>) to force a Link into Compliance mode. The encoding is the binary value of the bit location in the Port's Link Capability 2 register <i>Supported Link Speeds Vector</i> field (offset 94h[7:1]) that corresponds to the target Link speed. <i>For example</i> , a value of 3h indicates that the current Link speed is that which corresponds to bit 3 in the <i>Supported Link Speeds Vector</i> field, which is 8.0 GT/s. If a value written to this field does not correspond to a supported speed (as indicated by the Port's Link Capability register <i>Maximum Link Speed</i> field (offset 74h[3:0])), the value of this field is undefined. The default value of this field is the highest supported Link speed (as reported in the Port's <i>Maximum Link Speed</i> field); however, the default value for all Ports can be globally changed to 2h (Gen 2 maximum speed) or 1h (Gen 1 maximum speed), according to the STRAP_GEN1_GEN2 input state (Z = 2h (Gen 2), or 0 = 1h (Gen 1)).	Downstream	RWS	Yes	3h

Register 11-35. 98h Link Status and Control 2
(All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
4	Enter Compliance Software is permitted to force a Link to enter Compliance mode at the speed indicated in field [3:0] (<i>Target Link Speed</i>), by Setting this bit in both components on a Link, and then initiating a Hot Reset on the Link. The default value of this bit following a Fundamental Reset is 0.		RWS	Yes	0
5	Hardware-Autonomous Speed Disable <i>Reserved</i> Initial transition to the highest supported common Link speed is not blocked by this bit.		RsvdP	No	0
6	<i>Not valid</i>	Upstream	RsvdP	Yes	0
	Selectable De-Emphasis Selects the standard de-emphasis level when the Link is operating at 5.0 GT/s. When the Link is operating at 2.5 GT/s, the Setting of this bit has no effect (de-emphasis at 2.5 GT/s is -3.5 dB). 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)	Downstream	HwInit	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
9:7	Transmit Margin Intended for debug and compliance testing only.		RWS	Yes	000b
10	Enter Modified Compliance Intended for debug and compliance testing only.		RWS	Yes	0
11	Compliance SOS <i>This bit is applicable only when the Link is operating at 2.5 or 5.0 GT/s.</i> 1 = LTSSM must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern		RWS	Yes	0

Register 11-35. 98h Link Status and Control 2
(All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
15:12	Compliance Preset/De-Emphasis Intended for debug and compliance testing only. 8.0 GT/s Data Rate Sets the Transmitter Preset in the <i>Polling.Compliance</i> substate, if the entry occurred due to bit 4 (<i>Enter Compliance</i>) being Set. The encodings are defined in the <i>PCI Express Base r3.0</i> , Section 4.2.3.2, “Encoding of Presets.” Results are undefined if a Reserved preset encoding is used when entering the <i>Polling.Compliance</i> substate in this way. 5.0 GT/s Data Rate Sets the de-emphasis level in the <i>Polling.Compliance</i> substate, if the entry occurred due to bit 4 (<i>Enter Compliance</i>) being Set. 0h = -6 dB (Link is operating at 5.0 GT/s) 1h = -3.5 dB (Link is operating at 2.5 GT/s) 2.5 GT/s Data Rate The programming of this field has no effect.		RWS	Yes	0h
Link Status 2					
16	Current De-Emphasis Level Reflects the de-emphasis level when the Link is operating at 5.0 GT/s. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at either 2.5 or 5.0 GT/s)		RO	Yes	0
17	Equalization Complete 1 = Indicates that the Transmitter Equalization procedure has completed		ROS	Yes	0
18	Equalization Phase 1 Successful 1 = Indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed		ROS	Yes	0
19	Equalization Phase 2 Successful 1 = Indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed		ROS	Yes	0
20	Equalization Phase 3 Successful 1 = Indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed		ROS	Yes	0
21	Link Equalization Request Set by hardware, to request the Link equalization process to be performed on the Link.		RW1C	Yes	0
31:22	Reserved		RsvdP	No	0-0h

11.11 Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)

This section details the Subsystem ID and Subsystem Vendor ID Capability registers. [Table 11-10](#) defines the register map.

Table 11-10. Subsystem ID and Subsystem Vendor ID Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
<i>Reserved</i>	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh) A4h
Subsystem ID	Subsystem Vendor ID A8h	
<i>Reserved</i>		ACH – FCh

Register 11-36. A4h Subsystem Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	SSID/SSVID Capability ID SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the <i>PCI-to-PCI Bridge r1.2</i> .	RO	Yes	0Dh
15:8	Next Capability Pointer 00h = This capability is the last capability in the PEX 8747 Port's Capabilities list The PEX 8747 Extended Capabilities list starts at offset 100h.	RO	Yes	00h
31:16	<i>Reserved</i>	RsvdP	No	0000h

Register 11-37. A8h Subsystem ID and Subsystem Vendor ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	Subsystem Vendor ID The Vendor ID (offset 00h[15:0]) identifies the manufacturer of the PEX 8747, and the Subsystem Vendor ID optionally identifies the board or system vendor. As with the Vendor ID value, the Subsystem Vendor ID value must be a valid PCI-SIG-assigned Vendor ID. The value of this field is usually identical for all PEX 8747 Ports.	RO	Yes	10B5h
31:16	Subsystem ID The Device ID (offset 00h[31:16]) identifies the PEX 8747, and optionally the Subsystem ID in combination with the Subsystem Vendor ID, uniquely identifies the board or system. The value of this field is usually identical for all PEX 8747 Ports, and is chosen or assigned only by the “owner” of the valid Vendor ID value used for the Subsystem Vendor ID. If the board or system vendor is not a PCI-SIG member, PLX can assign, free of charge, a unique Subsystem ID value, in which case the Subsystem Vendor ID remains the PLX default value, 10B5h.	RO	Yes	8747h

11.12 Device Serial Number Extended Capability Registers (Offsets 100h – 108h)

This section details the Device Serial Number Extended Capability registers. [Table 11-11](#) defines the register map.

Table 11-11. Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Next Capability Offset (FB4h)																Capability Version (1h)				PCI Express Extended Capability ID (0003h)																100h
Serial Number (Lower DW)																																104h				
Serial Number (Upper DW)																																108h				

Register 11-38. 100h Device Serial Number Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID Program to 0003h, as required by the <i>PCI Express Base r3.0</i> .	RO	Yes	0003h
19:16	Capability Version Program to 1h, as required by the <i>PCI Express Base r3.0</i> .	RO	Yes	1h
31:20	Next Capability Offset Program to FB4h, which addresses the Advanced Error Reporting Extended Capability structure.	RO	Yes	FB4h

**Register 11-39. 104h Serial Number (Lower DW)
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	PCI Express Device Serial Number (1st DW) Lower half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the <i>PCI Express Base r3.0</i> , all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8747 Ports. The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64 TM), of which the upper 24 bits are the Company ID value (00_0EDFh) assigned by the IEEE Registration Authority, and the lower 40 bits are the Extension ID assigned by the identified Company (PLX). The most through least significant bytes are contained within the lowest through highest Byte addresses, respectively.	RO	Yes	B5DF_0E00h

**Register 11-40. 108h Serial Number (Upper DW)
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	PCI Express Device Serial Number (2nd DW) Upper half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the <i>PCI Express Base r3.0</i> , all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8747 Ports. The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64), of which the upper 24 bits are the Company ID value (00_0EDFh) assigned by the IEEE Registration Authority, and the lower 40 bits are the Extension ID assigned by the identified Company (PLX). The most through least significant bytes are contained within the lowest through highest Byte addresses, respectively.	RO	Yes	Silicon Revision BA: BA_8700_10h Silicon Revision CA: CA_8700_10h

11.13 Secondary PCI Express Extended Capability Registers (Offsets 10Ch – 134h)

This section details the Secondary PCI Express Extended Capability registers. [Table 11-12](#) defines the register map.

Table 11-12. Secondary PCI Express Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
Next Capability Offset (148h)										Capability Version (1h)						PCI Express Extended Capability ID (0019h)																10Ch
Link Control 3																																110h
<i>Reserved</i>																Lane Error Status																114h
Lane 1, 17, or 33 Equalization Control																Lane 0, 16, or 32 Equalization Control																118h
Lane 3, 19, or 35 Equalization Control																Lane 2, 18, or 34 Equalization Control																11Ch
Lane 5, 21, or 37 Equalization Control																Lane 4, 20, or 36 Equalization Control																120h
Lane 7, 23, or 39 Equalization Control																Lane 6, 22, or 38 Equalization Control																124h
Lane 9, 25, or 41 Equalization Control																Lane 8, 24, or 40 Equalization Control																128h
Lane 11, 27, or 43 Equalization Control																Lane 10, 26, or 42 Equalization Control																12Ch
Lane 13, 29, or 45 Equalization Control																Lane 12, 28, or 44 Equalization Control																130h
Lane 15, 31, or 47 Equalization Control																Lane 14, 30, or 46 Equalization Control																134h

Register 11-41. 10Ch Secondary PCI Express Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID Program to 0019h, as required by the <i>PCI Express Base r3.0</i> .	RO	Yes	0019h
19:16	Capability Version Program to 1h, as required by the <i>PCI Express Base r3.0</i> .	RO	Yes	1h
31:20	Next Capability Offset Program to 148h, which addresses the Virtual Channel Extended Capability structure.	RO	Yes	148h

**Register 11-42. 110h Link Control 3
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
0	<i>Reserved</i> if the Port's Link Capability 2 register <i>Cross-Link Supported</i> bit (offset 94h[8]) is Cleared.	Upstream	RsvdP	No	0
	Perform Equalization Writable if the Port's Link Capability 2 register <i>Cross-Link Supported</i> bit (offset 94h[8]) is programmed to a non-zero value. 1 = When 1 is written to the Port's Link Control register <i>Retrain Link</i> bit (Downstream Ports, offset 78h[5]), with the Port's Link Control 2 register <i>Target Link Speed</i> field (offset 98h[3:0]) programmed to 8.0 GT/s, the Downstream Port must perform Transmitter Equalization	Upstream/ Downstream	RW	Yes	0
1	<i>Reserved</i> if the Port's Link Capability 2 register <i>Cross-Link Supported</i> bit (offset 94h[8]) is Cleared.	Upstream	RsvdP	No	0
	Link Equalization Request Interrupt Enable Writable if the Port's Link Capability 2 register <i>Cross-Link Supported</i> bit (offset 94h[8]) is programmed to a non-zero value. 1 = Enables the generation of an interrupt, to indicate that the Port's Link Status 2 register <i>Link Equalization Request</i> bit (offset 98h[21]) has been Set	Upstream/ Downstream	RW	Yes	0
31:2	<i>Reserved</i>		RsvdP	No	0-0h

**Register 11-43. 114h Lane Error Status
(All Ports)**

Bit(s)	Description	Lane x	Type	Serial EEPROM and I ² C	Default
Bits [15:0] are intended for debug purposes only. <i>Notes:</i> Except for Ports that are configured as x16, the bits in this register reflect status for all Ports within the Station, rather than the individual Port associated with the Lane. The Lane x column is provided to indicate the Lane Number associated with each bit. Lane 0 is associated with Station 0, Lane 16 is associated with Station 1, and so forth. For further details regarding the Lane/Station relationship, refer to Table 11-5 .					
0	Lane x Error Status 0 = No Lane-based error is detected on the Lane 1 = Lane-based error is detected on the Lane	0, 16, or 32	RW1C	No	0
1		1, 17, or 33	RW1C	No	0
2		2, 18, or 34	RW1C	No	0
3		3, 19, or 35	RW1C	No	0
4		4, 20, or 36	RW1C	No	0
5		5, 21, or 37	RW1C	No	0
6		6, 22, or 38	RW1C	No	0
7		7, 23, or 39	RW1C	No	0
8		8, 24, or 40	RW1C	No	0
9		9, 25, or 41	RW1C	No	0
10		10, 26, or 42	RW1C	No	0
11		11, 27, or 43	RW1C	No	0
12		12, 28, or 44	RW1C	No	0
13		13, 29, or 45	RW1C	No	0
14		14, 30, or 46	RW1C	No	0
15		15, 31, or 47	RW1C	No	0
31:16	Reserved		RsvdP	No	0000h

Register 11-44. 118h Lane 0, 16, or 32 and 1, 17, or 33 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 0, 16, or 32 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-44. 118h Lane 0, 16, or 32 and 1, 17, or 33 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 1, 17, or 33 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-45. 11Ch Lane 2, 18, or 34 and 3, 19, or 35 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 2, 18, or 34 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-45. 11Ch Lane 2, 18, or 34 and 3, 19, or 35 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 3, 19, or 35 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-46. 120h Lane 4, 20, or 36 and 5, 21, or 37 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 4, 20, or 36 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-46. 120h Lane 4, 20, or 36 and 5, 21, or 37 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 5, 21, or 37 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-47. 124h Lane 6, 22, or 38 and 7, 23, or 39 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 6, 22, or 38 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-47. 124h Lane 6, 22, or 38 and 7, 23, or 39 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 7, 23, or 39 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-48. 128h Lane 8, 24, or 40 and 9, 25, or 41 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 8, 24, or 40 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-48. 128h Lane 8, 24, or 40 and 9, 25, or 41 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 9, 25, or 41 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-49. 12Ch Lane 10, 26, or 42 and 11, 27, or 43 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 10, 26, or 42 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-49. 12Ch Lane 10, 26, or 42 and 11, 27, or 43 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 11, 27, or 43 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-50. 130h Lane 12, 28, or 44 and 13, 29, or 45 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 12, 28, or 44 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-50. 130h Lane 12, 28, or 44 and 13, 29, or 45 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 13, 29, or 45 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

Register 11-51. 134h Lane 14, 30, or 46 and 15, 31, or 47 Equalization Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 14, 30, or 46 Equalization Control					
3:0	<i>Reserved</i>	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
6:4	<i>Reserved</i>	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
7	<i>Reserved</i>		RsvdP	No	0
11:8	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
14:12	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
15	<i>Reserved</i>		RsvdP	No	0

Register 11-51. 134h Lane 14, 30, or 46 and 15, 31, or 47 Equalization Control (All Ports) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Lane 15, 31, or 47 Equalization Control					
19:16	Reserved	Upstream	RsvdP	No	0h
	Downstream Port Transmitter Preset Preset used by the Downstream Port's Transmitters during Equalization Phase 1. Can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
22:20	Reserved	Upstream	RsvdP	No	000b
	Downstream Port Receiver Preset Hint Contains the Receiver Preset Hint value received from the Downstream device during Link Equalization, which can be used to adjust the Downstream Port's Receivers upon the change to Gen 3 speed. Use of the Receiver Preset Hint is optional (per the <i>PCI Express Base r3.0</i>), and the Port does not use the Hint.	Downstream	ROS	Yes	000b
23	Reserved		RsvdP	No	0
27:24	Upstream Port Transmitter Preset For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Transmit Preset value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	Fh
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device must use this value for its Transmitter Preset upon the speed change to Gen 3 speed. For Downstream Ports, the value can be loaded using the User Lane Equalization Control register (Port 0, 8, or 16, offset BC8h).	Downstream	ROS	Yes	0h
30:28	Upstream Port Receiver Preset Hint For Upstream Port, this field is intended for debug and diagnostics. If cross-link (enabled by default) is disabled for this Port (bit 8 of the Port's Link Control 2 register <i>Transmit Margin</i> field (offset 98h[9:7]) is Cleared), this field contains the Receiver Preset Hint value captured from the Equalization TS2s that are received on the associated Lane during Link Equalization; otherwise, this field is not used.	Upstream	ROS	No	111b
	For Downstream Ports, the Port transmits this value to the Downstream device, within the equalization TS2s sent during the <i>Recovery.RcvrCfg</i> substate preceding the speed change to Gen 3 speed. The Downstream device can use this value to adjust its Receivers upon the speed change to Gen 3 speed. For Downstream Ports, contains the value sent on the associated Lane during Link Equalization.	Downstream	ROS	Yes	000b
31	Reserved		RsvdP	No	0

11.14 Power Budget Extended Capability Registers (Offsets 138h – 144h)

This section details the Power Budget Extended Capability registers. These registers work differently than the others, especially with respect to serial EEPROM Reads and Writes. *For example*, when writing to Index 5 of the **Power Budget Data** register (Upstream Port, offset 140h), write 5 into the **Data Select** register *Data Select* field (Upstream Port, offset 13Ch[7:0]), then write the value into the **Power Budget Data** register. Table 11-13 defines the register map.

Table 11-13. Power Budget Extended Capability Register Map (Upstream Port)

31 30 29 28 27 26 25 24 23 22 21 20												15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
Next Capability Offset (10Ch) (Upstream)												Capability Version (1h) (Upstream)				PCI Express Extended Capability ID (0004h) (Upstream)												138h
<i>Reserved</i> (Downstream)																												
<i>Reserved</i> (Upstream)																Data Select (Upstream)								13Ch				
<i>Reserved</i> (Downstream)																												
Power Budget Data (Upstream)												<i>Reserved</i> (Downstream)												140h				
Power Budget Capability (Upstream) <i>Reserved</i> (Downstream)																												
144h																												

Register 11-52. 138h Power Budget Extended Capability Header (Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID Program to 0004h, as required by the <i>PCI Express Base r3.0</i> .	Upstream	RO	Yes	0004h
	<i>Reserved</i>	Downstream	RsvdP	No	0000h
19:16	Capability Version Program to 1h, as required by the <i>PCI Express Base r3.0</i> .	Upstream	RO	Yes	1h
	<i>Reserved</i>	Downstream	RsvdP	No	0h
31:20	Next Capability Offset Program to 10Ch, which addresses the Secondary PCI Express Extended Capability structure.	Upstream	RO	Yes	10Ch
	<i>Reserved</i>	Downstream	RsvdP	No	000h

**Register 11-53. 13Ch Data Select
(Upstream Port)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
7:0	Data Select Indexes the Power Budget data reported, by way of eight Upstream Port Power Budget Data registers, and selects the DWord of Power Budget data that appears in each Power Budget Data register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	Upstream	RW	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
31:8	Reserved		RsvdP	No	0000_00h

**Register 11-54. 140h Power Budget Data
(Upstream Port)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Note: Eight Upstream Port registers can be programmed, through the serial EEPROM, I ² C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the Data Select register Data Select field (offset 13Ch[7:0]).					
7:0	Base Power Eight Upstream Port registers. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (Data Scale) contents, to produce the actual power consumption value.	Upstream	RO	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
9:8	Data Scale Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (Base Power) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
12:10	PM Sub-State 000b = Power Management substate of the operating condition being described	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b

**Register 11-54. 140h Power Budget Data
(Upstream Port) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
14:13	PM State Power Management state of the operating condition being described. 00b = D0 state 11b = D3 state All other encodings are <i>Reserved</i> .	Upstream	RO	Yes	00b
	<i>Reserved</i>	Downstream	RsvdP	No	00b
17:15	Type Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are <i>Reserved</i> .	Upstream	RO	Yes	000b
	<i>Reserved</i>	Downstream	RsvdP	No	000b
20:18	Power Rail Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are <i>Reserved</i> .	Upstream	RO	Yes	000b
	<i>Reserved</i>	Downstream	RsvdP	No	000b
31:21	<i>Reserved</i>		RsvdP	No	0-0h

**Register 11-55. 144h Power Budget Capability
(Upstream Port)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
0	System Allocated 1 = Power budget for the device is included within the system power budget	Upstream	HwInit	Yes	1
	<i>Reserved</i>	Downstream	RsvdP	No	0
31:1	<i>Reserved</i>		RsvdP	No	0-0h

11.15 Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

This section details the Virtual Channel Extended Capability registers, which are duplicated for each Port, as well as the WRR Port Arbitration Table registers. [Table 11-14](#) defines the register map for one Port.

Table 11-14. Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
Next Capability Offset (E00h)												Capability Version (1h)				PCI Express Extended Capability ID (0002h)																148h
Port VC Capability 1																																14Ch
<i>Reserved</i>																				Port VC Capability 2												150h
Port VC Status (<i>Reserved</i>)																Port VC Control																154h
VC0 Resource Capability																																158h
VC0 Resource Control																																15Ch
VC0 Resource Status																<i>Reserved</i>																160h
<i>Reserved</i>																																164h –
WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)																																178h
																																...
																																1BCh

Register 11-56. 148h Virtual Channel Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID Program to 0002h, as required by the <i>PCI Express Base r3.0</i> .	RO	No	0002h
19:16	Capability Version Program to 1h, as required by the <i>PCI Express Base r3.0</i> .	RO	No	1h
31:20	Next Capability Offset Next extended capability is the Multicast Extended Capability structure, offset E00h.	RO	No	E00h

**Register 11-57. 14Ch Port VC Capability 1
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
2:0	Extended VC Counter 000b = Port supports only one Virtual Channel, VC0 001b = <i>Reserved</i> , because the PEX 8747 supports only one VC All other encodings are <i>Reserved</i> .		RO	No	000b
3	<i>Reserved</i>		RsvdP	No	0
6:4	Low-Priority Extended VC Counter For Strict Priority arbitration, indicates the quantity of extended Virtual Channels (VCs) (those in addition to VC0) that belong to the Low-Priority VC group for this Port. 000b = For this Port, only VC0 belongs to the Low-Priority VC group 001b = <i>Reserved</i> , because the PEX 8747 supports only one VC All other encodings are <i>Reserved</i> .		RO	No	000b
7	<i>Reserved</i>		RsvdP	No	0
9:8	Reference Clock <i>Reserved</i>		RsvdP	No	00b
11:10	Port Arbitration Table Entry Size 00b = Port Arbitration Table entry size is 1 bit 11b = Port Arbitration Table entry size is 8 bits All other encodings are <i>Reserved</i> .	Upstream	RO	Yes	11b
	<i>Reserved</i>	Downstream	RsvdP	No	00b
31:12	<i>Reserved</i>		RsvdP	No	0000_0h

**Register 11-58. 150h Port VC Capability 2
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	VC Arbitration Capability Indicates the type of VC arbitration supported by the device for the LPVC (Low-Priority Extended VC) group. 00h = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is not supported 01h = <i>Reserved</i> , because the PEX 8747 supports only one VC (Port VC Capability 2 register <i>Low-Priority Extended VC Counter</i> field, offset 14Ch[6:4]=000b)	RO	No	00h
31:8	<i>Reserved</i>	RsvdP	No	0000_00h

**Register 11-59. 154h Port VC Status and Control
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Port VC Control				
0	Load VC Arbitration Table <i>Not supported</i> The PEX 8747 supports only one Virtual Channel, VC0; therefore, a VC Arbitration Table is not present (Port VC Capability 2 register <i>Port Arbitration Table Offset</i> field (offset 150h[31:24]) is Cleared). Reads always return a value of 0.	RsvdP	No	0
3:1	VC Arbitration Select Selects the Port's VC arbitration type, as per the supported arbitration type indicated by the Port VC Capability 2 register <i>VC Arbitration Capability</i> field (offset 150h[7:0]) value. 000b = Bit 0; Round-Robin (Hardware-Fixed) arbitration scheme All other encodings are <i>Reserved</i> .	RW	Yes	000b
15:4	<i>Reserved</i>	RsvdP	No	000h
Port VC Status				
16	VC Arbitration Table Status <i>Reserved</i>	RsvdP	No	0
31:17	<i>Reserved</i>	RsvdP	No	0-0h

**Register 11-60. 158h VC0 Resource Capability
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
2:0	Port Arbitration Capability Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 32 Phases Bit 2 = 1 – WRR arbitration with 64 Phases	Upstream	RO	No	100b
		Downstream	RO	No	001b
13:3	Reserved		RsvdP	No	0-0h
14	Advanced Packet Switching		RsvdP	No	0
15	Reject Snoop Transactions Not a PCI Express switch feature; therefore, this bit is Cleared.		RsvdP	No	0
22:16	Maximum Time Slots Reserved		RsvdP	No	000_0000b
23	Reserved		RsvdP	No	0
31:24	Port Arbitration Table Offset Offset of the Port Arbitration Table, as the quantity of DQWords from the Base address of the Virtual Channel Extended Capability structure. (Refer to Section 11.15.1 for further details.) 00h = Port Arbitration Table is not present 03h = Port Arbitration Table is located at register offset 178h	Upstream	RO	No	03h
	Reserved	Downstream	RO	No	00h

**Register 11-61. 15Ch VC0 Resource Control
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
0	TC/VC Map Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	<i>Reserved</i>		RsvdP	No	00h
16	Load Port Arbitration Table Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns a value of 0.	Upstream	RW	Yes	0
	<i>Reserved</i>	Downstream	RsvdP	No	0
19:17	Port Arbitration Select Selects the Port's Port Arbitration type. Indicates the bit number in the VC0 Resource Capability register <i>Port Arbitration Capability</i> field (offset 158h[2:0]) that corresponds to the arbitration type. Allowed values: <ul style="list-style-type: none">000b if the Port Arbitration Table is not present000b or 010b if the Port Arbitration Table is present 000b = Fair Bandwidth (Hardware-Fixed Arbitration) 010b = Weighted Round-Robin with 64 Phases <i>Note: If software programs other values, hardware ignores the value.</i>	Upstream	RW	Yes	010b
		Downstream	RW	Yes	000b
23:20	<i>Reserved</i>	RsvdP	No	0h	
26:24	VC0 ID Defines the Port's VC0 ID code. 000b = VC0 (default; VC0 is the only/default VC) All other encodings are <i>Reserved</i> .	RsvdP	RO	No	000b
30:27	<i>Reserved</i>	RsvdP	No	0h	
31	VC0 Enable 0 = Not allowed 1 = Enables the Port's VC0	RsvdP	RO	No	1

**Register 11-62. 160h VC0 Resource Status
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
15:0	<i>Reserved</i>		RsvdP	No	0000h
16	Port Arbitration Table Status 0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the VC0 Resource Control register <i>Load Port Arbitration Table</i> bit (offset 15Ch[16]), or if the Port Arbitration Table is not implemented, then this bit is <i>Reserved</i> 1 = Port Arbitration Table entry was written to by software	Upstream	RO	No	0
	<i>Reserved</i>	Downstream	RsvdP	No	0
17	VC0 Negotiation Pending 0 = Port's VC0 negotiation is complete 1 = Port's VC0 initialization is not complete		RO	Yes	1
31:18	<i>Reserved</i>		RsvdP	No	0-0h

11.15.1 WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)

This section details the WRR Port Arbitration Table registers. Port Arbitration Table phases are used to determine Port weighting during “Weighted Round-Robin (WRR) with 64 Phases” Port arbitration.

Table 11-15 defines the register map. The numbers along the top of the register map table indicate the 8-bit fields of each 32-bit register. There are 64 phases, and any active Port Number can go into each Port *x* Phase *x* box.

Note: *The Port Arbitration Table is used only by the Upstream Port when Weighted Round-Robin with 64-Phase Port Arbitration is selected, by way of the VC0 Resource Control register Port Arbitration Select field (offset 15Ch[19:17]=010b).*

**Table 11-15. WRR Port Arbitration Table Register Map
(Ports 0, 8, and 16)**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																																
Port <i>x</i> , Phase 3																Port <i>x</i> , Phase 2																Port <i>x</i> , Phase 1																Port <i>x</i> , Phase 0																178h
Port <i>x</i> , Phase 7																Port <i>x</i> , Phase 6																Port <i>x</i> , Phase 5																Port <i>x</i> , Phase 4																17Ch
Port <i>x</i> , Phase 11																Port <i>x</i> , Phase 10																Port <i>x</i> , Phase 9																Port <i>x</i> , Phase 8																180h
Port <i>x</i> , Phase 15																Port <i>x</i> , Phase 14																Port <i>x</i> , Phase 13																Port <i>x</i> , Phase 12																184h
Port <i>x</i> , Phase 19																Port <i>x</i> , Phase 18																Port <i>x</i> , Phase 17																Port <i>x</i> , Phase 16																188h
Port <i>x</i> , Phase 23																Port <i>x</i> , Phase 22																Port <i>x</i> , Phase 21																Port <i>x</i> , Phase 20																18Ch
Port <i>x</i> , Phase 27																Port <i>x</i> , Phase 26																Port <i>x</i> , Phase 25																Port <i>x</i> , Phase 24																190h
Port <i>x</i> , Phase 31																Port <i>x</i> , Phase 30																Port <i>x</i> , Phase 29																Port <i>x</i> , Phase 28																194h
Port <i>x</i> , Phase 35																Port <i>x</i> , Phase 34																Port <i>x</i> , Phase 33																Port <i>x</i> , Phase 32																198h
Port <i>x</i> , Phase 39																Port <i>x</i> , Phase 38																Port <i>x</i> , Phase 37																Port <i>x</i> , Phase 36																19Ch
Port <i>x</i> , Phase 43																Port <i>x</i> , Phase 42																Port <i>x</i> , Phase 41																Port <i>x</i> , Phase 40																1A0h
Port <i>x</i> , Phase 47																Port <i>x</i> , Phase 46																Port <i>x</i> , Phase 45																Port <i>x</i> , Phase 44																1A4h
Port <i>x</i> , Phase 51																Port <i>x</i> , Phase 50																Port <i>x</i> , Phase 49																Port <i>x</i> , Phase 48																1A8h
Port <i>x</i> , Phase 55																Port <i>x</i> , Phase 54																Port <i>x</i> , Phase 53																Port <i>x</i> , Phase 52																1ACh
Port <i>x</i> , Phase 59																Port <i>x</i> , Phase 58																Port <i>x</i> , Phase 57																Port <i>x</i> , Phase 56																1B0h
Port <i>x</i> , Phase 63																Port <i>x</i> , Phase 62																Port <i>x</i> , Phase 61																Port <i>x</i> , Phase 60																1B4h
<i>Reserved</i>																																																1B8h –	1BCh															

**Register 11-63. 178h Port Arbitration Table Phases 0 to 3
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
4:0	Port Arbitration Table Phase 0	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	Reserved	RsvdP	No	000b
12:8	Port Arbitration Table Phase 1	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	Reserved	RsvdP	No	000b
20:16	Port Arbitration Table Phase 2	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	Reserved	RsvdP	No	000b
28:24	Port Arbitration Table Phase 3	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	Reserved	RsvdP	No	000b

**Register 11-64. 17Ch Port Arbitration Table Phases 4 to 7
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
4:0	Port Arbitration Table Phase 4	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	Reserved	RsvdP	No	000b
12:8	Port Arbitration Table Phase 5	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	Reserved	RsvdP	No	000b
20:16	Port Arbitration Table Phase 6	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	Reserved	RsvdP	No	000b
28:24	Port Arbitration Table Phase 7	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	Reserved	RsvdP	No	000b

**Register 11-65. 180h Port Arbitration Table Phases 8 to 11
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 8	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 9	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 10	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 11	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-66. 184h Port Arbitration Table Phases 12 to 15
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 12	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 13	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 14	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 15	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-67. 188h Port Arbitration Table Phases 16 to 19
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 16	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 17	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 18	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 19	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-68. 18Ch Port Arbitration Table Phases 20 to 23
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 20	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 21	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 22	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 23	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-69. 190h Port Arbitration Table Phases 24 to 27
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 24	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 25	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 26	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 27	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-70. 194h Port Arbitration Table Phases 28 to 31
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 28	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 29	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 30	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 31	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-71. 198h Port Arbitration Table Phases 32 to 35
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 32	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 33	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 34	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 35	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-72. 19Ch Port Arbitration Table Phases 36 to 39
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 36	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 37	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 38	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 39	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-73. 1A0h Port Arbitration Table Phases 40 to 43
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 40	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 41	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 42	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 43	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-74. 1A4h Port Arbitration Table Phases 44 to 47
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 44	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 45	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 46	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 47	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-75. 1A8h Port Arbitration Table Phases 48 to 51
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
4:0	Port Arbitration Table Phase 48	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	Reserved	RsvdP	No	000b
12:8	Port Arbitration Table Phase 49	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	Reserved	RsvdP	No	000b
20:16	Port Arbitration Table Phase 50	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	Reserved	RsvdP	No	000b
28:24	Port Arbitration Table Phase 51	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	Reserved	RsvdP	No	000b

**Register 11-76. 1ACh Port Arbitration Table Phases 52 to 55
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
4:0	Port Arbitration Table Phase 52	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	Reserved	RsvdP	No	000b
12:8	Port Arbitration Table Phase 53	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	Reserved	RsvdP	No	000b
20:16	Port Arbitration Table Phase 54	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	Reserved	RsvdP	No	000b
28:24	Port Arbitration Table Phase 55	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	Reserved	RsvdP	No	000b

**Register 11-77. 1B0h Port Arbitration Table Phases 56 to 59
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 56	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 57	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 58	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 59	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

**Register 11-78. 1B4h Port Arbitration Table Phases 60 to 63
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
4:0	Port Arbitration Table Phase 60	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	<i>Reserved</i>	RsvdP	No	000b
12:8	Port Arbitration Table Phase 61	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	<i>Reserved</i>	RsvdP	No	000b
20:16	Port Arbitration Table Phase 62	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Port Arbitration Table Phase 63	RW	Yes	Value is based upon the Port's Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	<i>Reserved</i>	RsvdP	No	000b

11.16 Device-Specific Registers (Offsets 1C0h – A74h)

This section details the Device-Specific registers located at offsets 1C0h through A74h. Device-Specific registers are unique to the PEX 8747 and not referenced in the *PCI Express Base r3.0*. [Table 11-16](#) defines the register map.

Other Device-Specific registers are detailed in:

- [Section 11.18, “Device-Specific Registers \(Offsets B70h – DFCh\)”](#)
- [Section 11.21, “Device-Specific Registers \(Offsets F30h – FB0h\)”](#)

Note: *It is recommended that these registers not be changed from their default values.*

Table 11-16. Device-Specific Register Map (Offsets 1C0h – A74h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
<i>Reserved</i>		1C0h – 1CCh
Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)		1D0h
		...
		1D8h
Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1E4h)		1DCh
		...
		1E4h
Device-Specific Registers – Read Pacing (Offset 1E8h)		1E8h
<i>Reserved</i>		1ECh – 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)		200h
		...
		25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 270h)		260h
		...
		270h
<i>Reserved</i>		274h – 28Ch
Device-Specific Registers – I2C and SMBus Slave Interfaces (Offsets 290h – 2FCh)		290h
		...
		2FCh
Device-Specific Registers – Port Configuration and Lane Status (Offsets 300h – 350h)		300h
		...
		350h
Device-Specific Registers – Port Configuration (Offsets 354h – 46Ch)		354h
		...
		46Ch

**Table 11-16. Device-Specific Register Map
(Offsets 1C0h – A74h) (Cont.)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<i>Factory Test Only/Reserved</i>																470h – 5FCh															
Device-Specific Registers – General-Purpose Input/Output (Offsets 600h – 68Ch)																600h															
																...															
																68Ch															
<i>Factory Test Only</i>																690h – 69Ch															
Device-Specific Registers – PORT_GOOD Selector (Offsets 6A0h – 6A8h)																6A0h															
																...															
																6A8h															
<i>Reserved</i>																6ACh – 6FCh															
Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)																700h															
																...															
																75Ch															
Device-Specific Registers – Control (Offsets 760h – 774h)																760h															
																...															
																774h															
Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)																778h															
																...															
																8FCh															
<i>Reserved</i>																900h – 9E8h															
Device-Specific Registers – Ingress Credit Handler (Offsets 9ECh – A2Ch)																9ECh															
																...															
																A2Ch															
Device-Specific Registers – Debug (Offsets A30h – A74h)																A30h															
																...															
																A74h															

11.16.1 Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)

Note: Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and enabling both concurrently can result in Fatal errors.

This section details the Device-Specific Read Pacing registers located at offsets 1D0h through 1D8h. [Table 11-17](#) defines the register map.

Another Device-Specific Read Pacing register is detailed in [Section 11.16.3, “Device-Specific Registers – Read Pacing \(Offset 1E8h\).”](#)

Read Pacing is described, in detail, in [Section 8.5, “Read Pacing.”](#)

Table 11-17. Device-Specific Read Pacing Register Map (Offsets 1D0h – 1D8h) (Ports 0, 8, and 16)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Read Pacing Control		1D0h
Read Pacing Threshold 1		1D4h
Read Pacing Threshold 2		1D8h

**Register 11-79. 1D0h Read Pacing Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name.</p> <p>Read Pacing and Source Queuing should not be concurrently enabled. The two features are incompatible and enabling both concurrently can result in Fatal errors.</p> <p>Read Pacing must be enabled for Read Spreading to be enabled. (That is, for a Port to have Read Spreading enabled, the corresponding Port bits within this register, for both Read Pacing and Read Spreading, must both be Cleared.)</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Port x Read Pacing Disable 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	0, 8, 9, 16, 17	RWS	Yes	1
2:1	Factory Test Only		RsvdP	No	00b
3	Reserved		ROS	No	1
11:4	Reserved		RsvdP	No	00h
12	Port x Memory Read Outstanding Counter Reset Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. Read returns a value of 0. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	0, 8, 9, 16, 17	RZ	Yes	0
14:13	Factory Test Only		RsvdP	No	00b
15	Reserved		RZ	Yes	0

**Register 11-79. 1D0h Read Pacing Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
16	Port x Memory Read Spreading Disable 0 = Memory Read Spreading is enabled for this Port 1 = Memory Read Spreading is disabled for this Port	0, 8, 9, 16, 17	RWS	Yes	0
18:17	Factory Test Only		RsvdP	No	00b
19	Reserved		ROS	No	0
27:20	Reserved		RsvdP	No	00h
31:28	Maximum Read Response Time 0h = Disabled 1h = 5 ms (default) 2h = 10 ms 3h = 15 ms 4h = 100 ms 5h = 200 ms 6h = 300 ms 7h = 500 ms 8h = 1.0s 9h = 2.0s All other encodings are Reserved .		RWS	Yes	1h

**Register 11-80. 1D4h Read Pacing Threshold 1
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
12:0	x16 Port Memory Read Outstanding Threshold Specified in DWords. Default value of 800h programs the threshold to 8 KB.	RWS	Yes	800h
15:13	Reserved	RsvdP	No	000b
28:16	x8 Port Memory Read Outstanding Threshold <i>Valid only for Stations 1 and 2.</i> Specified in DWords. Default value of 600h programs the threshold to 6 KB.	RWS	Yes	600h
31:29	Reserved	RsvdP	No	000b

**Register 11-81. 1D8h Read Pacing Threshold 2
(Ports 0, 8, and 16)**

Bit(s)	Descriptions	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
12:0	x4 Port Memory Read Outstanding Threshold Specified in DWords. Default value of 400h programs the threshold to 4 KB.	RWS	Yes	400h
15:13	Reserved	RsvdP	No	000b
28:16	x2 Port Memory Read Outstanding Threshold Specified in DWords. Default value of 200h programs the threshold to 2 KB.	RWS	Yes	200h
31:29	Reserved	RsvdP	No	000b

11.16.2 Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1E4h)

This section details the Device-Specific Captured Bus and Device Numbers register. [Table 11-18](#) defines the register map.

Table 11-18. Device-Specific Captured Bus and Device Numbers Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Captured Bus and Device Numbers		1DCh
Reserved		1E0h
Factory Test Only		1E4h

Register 11-82. 1DCh Captured Bus and Device Numbers (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
7:0	Captured Bus Number Captured Bus Number value for the Port. The value of this field can be overwritten, if bit 31 (<i>Captured BusDev Number Override</i>) is Set prior to changing the Captured Bus Number. <i>Note: Overwriting the Captured Bus Number value is not recommended.</i>		RW	Yes	00h
12:8	Captured Device Number Captured Device Number value for the Port. The value of this field can be overwritten, if bit 31 (<i>Captured BusDev Number Override</i>) is Set prior to changing the Captured Device Number. <i>Note: Overwriting the Captured Device Number value is not recommended.</i>	Upstream	RW	Yes	0-0h
		Downstream	RO	No	0-0h
30:13	Reserved		RsvdP	No	0-0h
31	Captured BusDev Number Override 1 = Enables the Captured Bus Number and Device Number to be overridden		RW	Yes	0

11.16.3 Device-Specific Registers – Read Pacing (Offset 1E8h)

Note: Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and enabling both concurrently can result in Fatal errors.

This section details one of the Device-Specific Read Pacing registers, at offset 1E8h. [Table 11-19](#) defines the register map.

Other Device-Specific Read Pacing registers are detailed in [Section 11.16.1, “Device-Specific Registers – Read Pacing \(Offsets 1D0h – 1D8h\).”](#)

Read Pacing is described, in detail, in [Section 8.5, “Read Pacing.”](#)

Table 11-19. Device-Specific Read Pacing Register Map (Offset 1E8h) (Port 0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Pacing Watermark																															

1E8h

Register 11-83. 1E8h Read Pacing Watermark (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12:0	Memory Read Outstanding Upper Watermark	ROS	No	000h
15:13	<i>Reserved</i>	RsvdP	No	000b
28:16	Memory Read Outstanding Lower Watermark	ROS	No	0-0h
30:29	Memory Read Outstanding Counter Selection	RWS	Yes	00b
31	Memory Read Outstanding Threshold Reset	RW	Yes	0

11.16.4 Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets 200h through 25Ch. [Table 11-20](#) defines the register map.

Other Device-Specific PHY registers are detailed in [Section 11.18.2, “Device-Specific Registers – Physical Layer \(Offsets B80h – C88h\).”](#)

**Table 11-20. Device-Specific PHY Register Map
(Offsets 200h – 25Ch) (Ports 0, 8, and 16)**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																	
Physical Layer Receiver Detect Status																Physical Layer Electrical Idle for Compliance Mask																200h	
Physical Layer Receiver Not Detected Mask																Physical Layer Electrical Idle Detect Mask																204h	
Port Control																																208h	
Physical Layer User Test Pattern, Bytes 0 through 3																																20Ch	
Physical Layer User Test Pattern, Bytes 4 through 7																																210h	
Physical Layer User Test Pattern, Bytes 8 through 11																																214h	
Physical Layer User Test Pattern, Bytes 12 through 15																																218h	
Physical Layer Command and Status																																21Ch	
Physical Layer Function Control																																220h	
Physical Layer Test 0																																224h	
Physical Layer Test 1																								Reserved								228h	
Physical Layer Safety Bits																																22Ch	
Reserved								Factory Test Only																Physical Layer Port Command								230h	
SKIP Ordered-Set Interval																																234h	
SerDes Quad 0 Diagnostic Data																																238h	
SerDes Quad 1 Diagnostic Data																																23Ch	
SerDes Quad 2 Diagnostic Data																																240h	
SerDes Quad 3 Diagnostic Data																																244h	
Factory Test Only																Target Link Width																248h	
Factory Test Only																																24Ch –	250h
Physical Layer Additional Status																																254h	
Factory Test Only/Reserved																Physical Layer Additional Control																258h	
Reserved								Factory Test Only																Physical Layer Error Injection Control								25Ch	

Register 11-84. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Ports 0, 8, and 16)

Bit(s)	Description	SerDes x/Lane x	Type	Serial EEPROM and I ² C	Default
<p>This register is used for specifying the pre-determined quantity of Lanes that detected a Receiver during an LTSSM <i>Detect</i> state, but never detected an exit from Electrical Idle. Because the PEX 8747 has various Port configurations, a Mask register is used, rather than programming a specific quantity. When multiple bits are Set, and they correspond to Lanes that belong to the same Port, any of those specified Lanes can cause entry into the LTSSM <i>Polling.Compliance</i> substate.</p> <p>Notes: The <i>SerDes x/Lane x</i> column is provided to indicate the SerDes/Lane Number associated with bits/fields that include “SerDes x” or “Lane x” in their name.</p> <p><i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
Physical Layer Electrical Idle for Compliance Mask					
This register allows masking that specifies which Lanes must never exit Electrical Idle, for entry to the LTSSM <i>Polling.Compliance</i> substate to occur.					
0	Electrical Idle on SerDes x Causes Entry to Compliance State When all the bits are Cleared, the LTSSM <i>Polling.Compliance</i> substate cannot be entered, due to the Electrical Idle condition. 1 = Lane must have detected a Receiver during an LTSSM <i>Detect</i> state, and must not see an exit from Electrical Idle during the <i>Polling.Active</i> substate, to cause entry to the <i>Polling.Compliance</i> substate	0, 16, or 32	RWS	Yes	1
1		1, 17, or 33	RWS	Yes	1
2		2, 18, or 34	RWS	Yes	1
3		3, 19, or 35	RWS	Yes	1
4		4, 20, or 36	RWS	Yes	1
5		5, 21, or 37	RWS	Yes	1
6		6, 22, or 38	RWS	Yes	1
7		7, 23, or 39	RWS	Yes	1
8		8, 24, or 40	RWS	Yes	1
9		9, 25, or 41	RWS	Yes	1
10		10, 26, or 42	RWS	Yes	1
11		11, 27, or 43	RWS	Yes	1
12		12, 28, or 44	RWS	Yes	1
13		13, 29, or 45	RWS	Yes	1
14		14, 30, or 46	RWS	Yes	1
15		15, 31, or 47	RWS	Yes	1

Register 11-84. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Ports 0, 8, and 16) (Cont.)

Bit(s)	Description	SerDes <i>x</i> /Lane <i>x</i>	Type	Serial EEPROM and I ² C	Default
Physical Layer Receiver Detect Status					
This register returns the Receiver's LTSSM <i>Detect</i> state status for all Lanes within the Station.					
16	Receiver Detected on Lane <i>x</i> Reads back as 1 when a Receiver is detected on the Lane.	0, 16, or 32	ROS	No	Set by SerDes
17		1, 17, or 33	ROS	No	Set by SerDes
18		2, 18, or 34	ROS	No	Set by SerDes
19		3, 19, or 35	ROS	No	Set by SerDes
20		4, 20, or 36	ROS	No	Set by SerDes
21		5, 21, or 37	ROS	No	Set by SerDes
22		6, 22, or 38	ROS	No	Set by SerDes
23		7, 23, or 39	ROS	No	Set by SerDes
24		8, 24, or 40	ROS	No	Set by SerDes
25		9, 25, or 41	ROS	No	Set by SerDes
26		10, 26, or 42	ROS	No	Set by SerDes
27		11, 27, or 43	ROS	No	Set by SerDes
28		12, 28, or 44	ROS	No	Set by SerDes
29		13, 29, or 45	ROS	No	Set by SerDes
30		14, 30, or 46	ROS	No	Set by SerDes
31		15, 31, or 47	ROS	No	Set by SerDes

**Register 11-85. 204h Electrical Idle Detect/Receiver Detect Mask
(Ports 0, 8, and 16)**

Bit(s)	Description	SerDes x	Type	Serial EEPROM and I ² C	Default
Masking Electrical Idle detect will not affect the inferred Electrical Idle detection.					
Notes: Use this register with caution.					
The SerDes x column is provided to indicate the Port Number associated with bits/fields that include “SerDes x” in their name.					
Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.					
The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.					
Physical Layer Electrical Idle Detect Mask					
Never Detect Electrical Idle mask. This register allows masking of the Electrical Idle Detect function, on a per-SerDes basis. When the bits in this register are Set, the Lane’s Electrical Idle Condition flag does not assert, regardless of the actual presence of Electrical Idle. Masking Electrical Idle detect does not affect the inferred Electrical Idle detection.					
0	SerDes x Mask Electrical Idle Detect 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle	0, 16, or 32	RWS	Yes	0
1		1, 17, or 33	RWS	Yes	0
2		2, 18, or 34	RWS	Yes	0
3		3, 19, or 35	RWS	Yes	0
4		4, 20, or 36	RWS	Yes	0
5		5, 21, or 37	RWS	Yes	0
6		6, 22, or 38	RWS	Yes	0
7		7, 23, or 39	RWS	Yes	0
8		8, 24, or 40	RWS	Yes	0
9		9, 25, or 41	RWS	Yes	0
10		10, 26, or 42	RWS	Yes	0
11		11, 27, or 43	RWS	Yes	0
12		12, 28, or 44	RWS	Yes	0
13		13, 29, or 45	RWS	Yes	0
14		14, 30, or 46	RWS	Yes	0
15		15, 31, or 47	RWS	Yes	0

**Register 11-85. 204h Electrical Idle Detect/Receiver Detect Mask
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	SerDes x	Type	Serial EEPROM and I ² C	Default
Physical Layer Receiver Not Detected Mask					
Always Detect a Receiver mask. This register allows masking of the Receiver Detect function, on a per SerDes basis. When the bits in this register are Set, the PHY functions as if the Lane detected a Receiver, regardless of the actual presence of a Receiver.					
16	SerDes x Mask Receiver Not Detected 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver	0, 16, or 32	RWS	Yes	0
17		1, 17, or 33	RWS	Yes	0
18		2, 18, or 34	RWS	Yes	0
19		3, 19, or 35	RWS	Yes	0
20		4, 20, or 36	RWS	Yes	0
21		5, 21, or 37	RWS	Yes	0
22		6, 22, or 38	RWS	Yes	0
23		7, 23, or 39	RWS	Yes	0
24		8, 24, or 40	RWS	Yes	0
25		9, 25, or 41	RWS	Yes	0
26		10, 26, or 42	RWS	Yes	0
27		11, 27, or 43	RWS	Yes	0
28		12, 28, or 44	RWS	Yes	0
29		13, 29, or 45	RWS	Yes	0
30		14, 30, or 46	RWS	Yes	0
31		15, 31, or 47	RWS	Yes	0

**Register 11-86. 208h Port Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>This register is used to disable or enable the LTSSM within individual Ports. The Port Control bits are intended to be used in lieu of placing the Port into the <i>Loopback.Active</i> substate as a Loopback Master. These bits enable the test patterns to be transmitted, with or without a device attached at the far end. Recommended usage is as follows:</p> <ol style="list-style-type: none"> Set the Port's <i>Disable Port x</i> and <i>Hold Port x Quiet</i> bits (bits [1:0 and 9:8], respectively). <ul style="list-style-type: none"> Setting the Port's <i>Disable Port x</i> bit forces the Port into the <i>Detect.Quiet</i> substate. If no device is attached, it is not necessary to Set the Port's <i>Disable Port x</i> bit. If 8.0 GT/s is needed, also Set the Port's <i>Port x Test Pattern x Rate</i> bit (bit 24). If Set, Clear the Port's <i>Disable Port x</i> bit. Load the UTP registers and enable UTP transmission, or just enable PRBS transmission. <p>Notes: The <i>Port x</i> column is provided to indicate the Port Number associated with bits/fields that include "Port x" in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bits [17, 9, and 1], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Disable Port x While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state. Note: Software should not Set a Port's <i>Disable Port x</i> bit while that Port's Link is in the L2/L3 Ready Link PM state. 0 = Enables the Port's Link Training operation. 1 = LTSSM remains in the <i>Detect.Quiet</i> substate on the Port if it is currently in, or returns to, that substate. Unconditionally disables the Port. This is different from an LTSSM <i>Disabled</i> state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the <i>Detect.Quiet</i> substate and remains there. No EIOS is sent, which could force any connected device to the <i>Recovery</i> state, and then to an LTSSM <i>Detect</i> state. The Port remains disabled until its <i>Disable Port x</i> bit is Cleared.	0, 8, 16	RWS	Yes	0
1		9, 17	RWS	Yes	0
5:2	Factory Test Only		RsvdP	No	0h
7:6	Reserved		RsvdP	No	00b

**Register 11-86. 208h Port Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
8	Hold Port x Quiet 0 = No effect on the LTSSM. 1 = Port remains in the <i>Detect.Quiet</i> substate once it returns there. These bits do not force the LTSSM into the <i>Detect.Quiet</i> substate. (Refer to the <i>Disable Port x</i> bits.) After entering the <i>Detect.Quiet</i> substate, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. The Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the <i>Loopback.Active</i> substate. <i>Note: Use these bits when it is necessary to transmit some data pattern, without first entering the Loopback.Active substate as a Loopback Master.</i>	0, 8, 16	RWS	Yes	0
9		9, 17	RWS	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Port x Bypass UTP Alignment Pattern Must be Set when the following conditions are met: <ul style="list-style-type: none"> Link width of the Port being tested is wider than x4, and Port being tested is a Loopback Master transmitting the User Test Pattern, and Loopback Slave is in a different clock domain 	0, 8, 16	RWS	Yes	0
17		9, 17	RWS	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
23:22	Reserved		RsvdP	No	00b
24	Port x Test Pattern x Rate The Port transmits the selected test pattern (PRBS or UTP) at 8.0 GT/s, if the Port's <i>Hold Port x Quiet</i> bit (bits [9:8]) is also Set (manual rate selection is enabled only when the Port's <i>Hold Port x Quiet</i> bit is Set). Set when the Link must transmit at Gen 3 Link speed. 0 = UTP is transmitted at the Link's current speed 1 = UTP is transmitted at a rate of 8.0 GT/s <i>Note: If the Port's Port x Bypass UTP Alignment Pattern bit (bits [17:16]) is Set, this bit (for that Port) cannot be used.</i>	0, 8, 9, 16, 17	RWS	Yes	0

**Register 11-86. 208h Port Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
26:25	Factory Test Only		RsvdP	No	00b
27	Reserved		RsvdP	No	0
28	Test Pattern x Rate Port x Select When Set along with the Port's <i>Hold Port x Quiet</i> bit (bits [9:8]), the selected test pattern is transmitted at 5.0 GT/s, on the selected Port. Only values 000b through 101b are valid. If 110b or 111b is written to this field, uninitialized values are returned in the Port's <i>Port x Test Pattern x Rate</i> bit (bits [9:8]) when this register is read.	0, 8, 9, 16, 17	RWS	Yes	0
30:29	Factory Test Only		RsvdP	No	00b
31	Reserved		RsvdP	No	0

**Register 11-87. 20Ch Physical Layer User Test Pattern, Bytes 0 through 3
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>UTP Bytes 0 through 3. Used for Digital Far-End Loopback testing.</p> <p>A 16-byte test pattern can be written to register offsets 20Ch through 218h. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 20Ch is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 218h is transmitted last. (Refer to Section 12.2.4, “Digital Loopback Master Mode,” for further details.) In Gen 1 and Gen 2 modes, every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified. In Gen 3 mode, the UTP generator sends a Data block (Sync Header 10b), with the UTP register data as the content.</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
7:0	Byte 0 of the UTP. This is the first byte transferred.	RWS	Yes	00h
15:8	Byte 1 of the UTP.	RWS	Yes	00h
23:16	Byte 2 of the UTP.	RWS	Yes	00h
31:24	Byte 3 of the UTP.	RWS	Yes	00h

**Register 11-88. 210h Physical Layer User Test Pattern, Bytes 4 through 7
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>UTP Bytes 4 through 7. Used for Digital Far-End Loopback testing.</p> <p>A 16-byte test pattern can be written to register offsets 20Ch through 218h. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 20Ch is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 218h is transmitted last. (Refer to Section 12.2.4, “Digital Loopback Master Mode,” for further details.) In Gen 1 and Gen 2 modes, every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified. In Gen 3 mode, the UTP generator sends a Data block (Sync Header 10b), with the UTP register data as the content.</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
7:0	Byte 4 of the UTP. This is the fifth byte transferred.	RWS	Yes	00h
15:8	Byte 5 of the UTP.	RWS	Yes	00h
23:16	Byte 6 of the UTP.	RWS	Yes	00h
31:24	Byte 7 of the UTP.	RWS	Yes	00h

**Register 11-89. 214h Physical Layer User Test Pattern, Bytes 8 through 11
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
UTP Bytes 8 through 11. Used for Digital Far-End Loopback testing. A 16-byte test pattern can be written to register offsets 20Ch through 218h. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 20Ch is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 218h is transmitted last. (Refer to Section 12.2.4, “Digital Loopback Master Mode,” for further details.) In Gen 1 and Gen 2 modes, every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified. In Gen 3 mode, the UTP generator sends a Data block (Sync Header 10b), with the UTP register data as the content. Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
7:0	Byte 8 of the UTP. This is the ninth byte transferred.	RWS	Yes	00h
15:8	Byte 9 of the UTP.	RWS	Yes	00h
23:16	Byte 10 of the UTP.	RWS	Yes	00h
31:24	Byte 11 of the UTP.	RWS	Yes	00h

**Register 11-90. 218h Physical Layer User Test Pattern, Bytes 12 through 15
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
UTP Bytes 12 through 15. Used for Digital Far-End Loopback testing. A 16-byte test pattern can be written to register offsets 20Ch through 218h. When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 20Ch is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 218h is transmitted last. (Refer to Section 12.2.4, “Digital Loopback Master Mode,” for further details.) In Gen 1 and Gen 2 modes, every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified. In Gen 3 mode, the UTP generator sends a Data block (Sync Header 10b), with the UTP register data as the content. Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
7:0	Byte 12 of the UTP. This is the thirteenth byte transferred.	RWS	Yes	00h
15:8	Byte 13 of the UTP.	RWS	Yes	00h
23:16	Byte 14 of the UTP.	RWS	Yes	00h
31:24	Byte 15 of the UTP.	RWS	Yes	00h

**Register 11-91. 21Ch Physical Layer Command and Status
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register provides various Command and Status bits for Physical Layer operation.</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
3:0	Number of Ports Available in the Station Returns the quantity of enabled Ports within this Station, based upon the selected Port configuration.	ROS	No	Defined by STRAP_STNx_PORTCFG0 input states, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station x</i> field(s) (Port 0, offset 300h[8:6, 5:3, and/or 2:0])
4	Upstream Cross-Link Enable 0 = Disables Upstream cross-link, Upstream Port cannot be connected to another Upstream Port 1 = Enables Upstream cross-link, Upstream Port can be connected to another Upstream Port	ROS	Yes	1
5	Downstream Cross-Link Enable 0 = Disables Downstream cross-link, Downstream Ports cannot be connected to other Downstream Ports 1 = Enables Downstream cross-link, Downstream Ports can be connected to other Downstream Ports	ROS	Yes	1
6	Lane Reversal Disable 0 = Enables Lane reversal on all Ports 1 = Disables Lane reversal on all Ports	ROS	Yes	0
7	Reserved	RsvdP	No	0
15:8	LTSSM Watch Dog Timer Disable Disables the Port's LTSSM Watchdog Timer.	RWS	Yes	00h
31:16	User Test Pattern Control/Data The UTP generators send out a set of 16 bytes of User Programmable data. For Gen 1 and Gen 2 Link speeds (2.5 and 5.0 GT/s, respectively), a k-code bit can be Set for each byte. Bit 16 corresponds to Byte 0 of the User Test Pattern. ... Bit 31 corresponds to Byte 15 of the User Test Pattern. 0 = Corresponding byte of the User Test Pattern is transmitted as a Data character 1 = Corresponding byte of the User Test Pattern is transmitted as a Control character Notes: <i>Use caution when Setting bits within this field, because UTP logic does not check the validity of Control characters.</i> <i>In Gen 3 mode, the UTP generator sends a Data block (Sync Header 10b), with the UTP register data as the content.</i>	RWS	Yes	0000h

**Register 11-92. 220h Physical Layer Function Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>This register allows for the configuration of various functions within the PHY logic.</p> <p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bits [25 and 17], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
3:0	<p>Configuration Fail Count</p> <p>This field is used only if the SPARE2 input is Low, to modify Link training for a non-compliant Gen 1 device, that would otherwise fail Link training if the <i>Data Rate</i> bits in the TS are Set.</p> <p>Specifies the quantity of times that Link training fails (in either of the LTSSM <i>Polling</i> or <i>Configuration</i> states), after which the Port re-starts Link training (from the <i>Detect</i> state), advertising only a Gen 1 data rate.</p> <p>The initial value of this register is determined by the Strap Configuration register <i>Gen 1 Compatible Disable Status</i> bit (Port 0, offset 46Ch[10]) value, which defaults to the inverse state of the SPARE2 input. If the bit value is 0 when reset de-asserts, the initial value of this field is 1h; otherwise, the initial value is 0h.</p>		RWS	Yes	<p>0h (offset 46Ch[10]=1)</p> <p>1h (offset 46Ch[10]=0)</p>
7:4	Reserved		RsvdP	No	0h
9:8	<p>Detect.Quiet Wait Time Select Code [1:0]</p> <p>Selects the amount of time to wait during the <i>Detect.Quiet</i> substate, before starting the Receiver Detect operation, when a break from Electrical Idle is detected. If Electrical Idle is detected on all Lanes, the wait time is 12 ms.</p> <p>00b = 0 ms 01b = 4 ms (default) 10b = 8 ms 11b = 12 ms</p>		RWS	Yes	01b
11:10	Reserved		RsvdP	No	00b

**Register 11-92. 220h Physical Layer Function Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
12	Elastic Buffer Sync Reset Enable 1 = Enable Elastic Buffer Reset upon entry to the <i>Recovery</i> state (if bit 14 (<i>Elastic Buffer Sync Reset on Rx Recovery Enable</i>) is Set) or entry to the <i>Configuration</i> state from the <i>Recovery</i> state for upconfigure		RWS	Yes	1
13	Symbol-Block Align Sync Reset Enable 1 = Enable Block and Symbol Aligner Sync Reset with Elastic Buffer Sync Reset		RWS	Yes	1
14	Elastic Buffer Sync Reset on Rx Recovery Enable 1 = Reset Elastic buffer when Receivers are detected entering the <i>Recovery</i> state		RWS	Yes	1
15	Inferred Electrical Idle Exit Type Selects the method used to detect exit from Electrical Idle, after Electrical Idle has been inferred. 0 = Fast Method – Type 0 Exit mode is used, which uses conventional analog Electrical Idle Exit Detection circuitry 1 = Slow Method – Type 1 Exit mode is used, which uses the Symbol Framing Detection Time Select Code and Inferred Electrical Idle Exit Time Select Code Timers		RWS	Yes	0
16	Port x Electrical Idle Inference on EIOS Receipt Enable Electrical Idle Inference on Electrical Idle Ordered-Set (EIOS) Receipt enable, for the Port. 0 = Electrical Idle inference is enabled upon EIOS receipt, if the Physical Layer Electrical Idle Detect Mask register <i>SerDes x Mask Electrical Idle Detect</i> bits (Port 0, 8, or 16, offset 204h[15:0]) are Set, for the SerDes associated with the Port 1 = Electrical Idle will be inferred as soon as an EIOS is received on any Lane of the Port	0, 8, 16	RWS	Yes	0
17		9, 17	RWS	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
23:22	Reserved		RsvdP	No	00b
24	Port x Electrical Idle Inference Disable 0 = Electrical Idle inference is enabled, if the Physical Layer Electrical Idle Detect Mask register <i>SerDes x Mask Electrical Idle Detect</i> bits (Port 0, 8, or 16, offset 204h[15:0]) are Set, for the SerDes associated with the Port. 1 = Port's overall Electrical Idle inference logic is disabled. Electrical Idle inference during the <i>Recovery.Speed</i> substate is not affected and will continue to operate.	0, 8, 16	RWS	Yes	0
25		9, 17	RWS	Yes	0
30:26	Factory Test Only		RsvdP	No	0-0h
31	Reserved		RsvdP	No	0

Register 11-93. 224h Physical Layer Test 0
(Ports 0, 8, and 16)

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>This register provides controls to enable various PHY test modes.</p> <p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bit 1, is Factory Test Only, RsvdP, not serial EEPROM-writable, and has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Port x Timer Test Mode Enable 0 = Normal PHY Timer parameters are used	0, 8, 16	RWS	Yes	0
1	1 = Millisecond scale timers in the Port’s LTSSM are reduced to microsecond scale	9, 17	RWS	Yes	0
5:2	Factory Test Only		RsvdP	No	0h
7:6	Reserved		RsvdP	No	00b
8	SKIP Timer Test Mode Enable 0 = Disables Skip Timer Test mode. 1 = Enables Skip Timer Test mode. SKIP Ordered-Sets are transmitted every 256 symbol times, on all Ports, regardless of the SKIP Ordered-Set Interval register <i>SKIP Ordered-Set Interval in Clocks</i> (Gen 1 and Gen 2 Link speeds) or <i>SKIP Ordered-Set Interval in Blocks</i> (Gen 3 Link speeds) field (offset 234h[11:0 or 27:16], respectively) value.		RW	Yes	0
9	Ignore Compliance Receive TCB Ignore the <i>Compliance Receive</i> Training Control Bit (TCB) field in Training Sets. 1 = Causes the PHY to ignore the <i>Compliance Receive</i> TCB when it is Set in received Training Sets		RWS	Yes	0
10	Analog Loopback Enable 0 = PEX 8747 enters Digital Loopback Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the <i>Loopback</i> bit exclusively Set in the TS1 Training Control symbol. The PEX 8747 then loops back data through the Elastic buffer, and decoder and encoder (8b/10b for Gen 1 and Gen 2 Link speeds, or 128b/130b for Gen 3 Link speed). 1 = When operating as a Loopback Slave, the Loopback point of all Ports will be before the Elastic buffer in the Recovered Receive Clock domain.		RWS	Yes	0
11	Factory Test Only		RW	Yes	0
19:12	Factory Test Only		RWS	Yes	00h
31:20	Reserved		RsvdP	No	000h

**Register 11-94. 228h Physical Layer Test 1
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x or SerDes Quad x/SerDes Pair x	Type	Serial EEPROM and I ² C	Default
<p>This register provides controls to enable various PHY test modes.</p> <p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. The SerDes Quad x/SerDes Pair x column is provided to indicate the SerDes quad and SerDes pair(s) associated with bits/fields that include “SerDes Quad x/SerDes Pair x” in their name.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p> <p>Port 0, bits [17 and 9], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
7:0	Reserved		RWS	No	00h
8	Port x Serial Loopback Path Enable 1 = Enables serial loopback (NES) on the Port	0, 8, 16	RWS	Yes	0
9		9, 17	RWS	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Port x Parallel Loopback Path Enable 1 = Enables the Parallel loopback (LB) path on the Port (analog loopback = 0 LB_PIPE, analog loopback = 1 LB_FEP)	0, 8, 16	RWS	Yes	0
17		9, 17	RWS	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
23:22	Reserved		RsvdP	No	00b

**Register 11-94. 228h Physical Layer Test 1
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x or SerDes Quad x/SerDes Pair x	Type	Serial EEPROM and I ² C	Default
24	SerDes Quad x Pair x User Test Pattern Enable Enables the User Test Pattern generator for SerDes Pair x, by Station. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (Physical Layer User Test Pattern, Bytes x through y registers (Port 0, 8, or 16, offsets 20Ch through 218h)) on SerDes Pair x, by Station, in Digital Far-End Loopback Master mode <i>Notes: UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet substate and the Port's Port Control register Hold Port x Quiet bit (Port 0, 8, or 16, offset 208h[9:8]) is Set.</i> <i>The Port's Port Control register Port x Bypass UTP Alignment Pattern bit (Port 0, 8, or 16, offset 208h[17:16]) must be Set if the Link width of the Port under test is wider than x4, the Port under test is a Loopback Master, and the Loopback Slave is in a different clock domain.</i>	SerDes Quad 0 (Lower Pair) SerDes[0, 1]/[16, 17]/[32, 33]	RWS	Yes	0
25		SerDes Quad 0 (Upper Pair) SerDes[2, 3]/[18, 19]/[34, 35]	RWS	Yes	0
26		SerDes Quad 1 (Lower Pair) SerDes[4, 5]/[20, 21]/[36, 37]	RWS	Yes	0
27		SerDes Quad 1 (Upper Pair) SerDes[6, 7]/[22, 23]/[38, 39]	RWS	Yes	0
28		SerDes Quad 2 (Lower Pair) SerDes[8, 9]/[24, 25]/[40, 41]	RWS	Yes	0
29		SerDes Quad 2 (Upper Pair) SerDes[10, 11]/[26, 27]/[42, 43]	RWS	Yes	0
30		SerDes Quad 3 (Lower Pair) SerDes[12, 13]/[28, 29]/[44, 45]	RWS	Yes	0
31		SerDes Quad 3 (Upper Pair) SerDes[14, 15]/[30, 31]/[46, 47]	RWS	Yes	0

**Register 11-95. 22Ch Physical Layer Safety Bits
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
4:0	Factory Test Only	RWS	Yes	0-0h
5	Reserved	RWS	Yes	0
6	Upconfigure Capability Disable 0 = Upconfigure capability is advertised on all Ports 1 = Upconfigure capability is not advertised on all Ports	RWS	Yes	0
19:7	Reserved	RWS	Yes	0-0h
24:20	Factory Test Only	RWS	Yes	0-0h
27:25	Reserved	RWS	Yes	000b
30:28	Factory Test Only	RWS	Yes	111b
31	Reserved	RWS	Yes	1

**Register 11-96. 230h Physical Layer Port Command
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register provides the Loopback, Scrambler Disable, and Compliance Receive commands, and Ready as Loopback Master status, for each Port.</p> <p>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bits [7:4], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>				
0	Port 0, 8, 16 Loopback Command 0 = Port is not enabled to go to the <i>Loopback</i> Master state. 1 = Port attempts to enter the <i>Loopback</i> state as a Loopback Master. If this bit is Set before the <i>Configuration</i> state is reached, the <i>Configuration.Linkwidth.Start</i> to <i>Loopback</i> path is used. If this bit is Set later, the <i>Recovery.Idle</i> to <i>Loopback</i> path is used.	RWS	Yes	0
1	Port 0, 8, 16 Scrambler Disable Command When Set, unconditionally disables the data scramblers on the Port's Lane(s), and causes the <i>Scramble Disable</i> Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a <i>Configuration.Complete</i> substate. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through <i>Configuration</i> again. The Upstream/Downstream device scrambler will not be disabled. 0 = Port's scrambler is enabled 1 = Port's scrambler is disabled	RWS	Yes	0
2	Port 0, 8, 16 Compliance Receive Command 0 = When the Port transmits TS1 Ordered-Sets, the <i>Compliance Receive</i> Training Control Bit within these Ordered-Sets is not Set during the <i>Polling.Active</i> nor <i>Loopback.Entry</i> substate 1 = When the Port transmits TS1 Ordered-Sets, the <i>Compliance Receive</i> Training Control Bit within these Ordered-Sets is Set during the <i>Polling.Active</i> or <i>Loopback.Entry</i> substate	RWS	Yes	0
3	Port 0, 8, 16 Ready as Loopback Master Link Training and Status State Machine (LTSSM) established Loopback as a Master for the Port. 0 = Port is not in Loopback Master mode. 1 = Indicates that the Port has successfully transitioned to the <i>Loopback.Active</i> substate as a Loopback Master. The LTSSM remains in this substate, until bit 0 (Port 0, 8, 16 Loopback Command) is Cleared. This bit is Cleared when the PEX 8747 exits the <i>Loopback.Active</i> substate.	ROS	No	0

**Register 11-96. 230h Physical Layer Port Command
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4	Port 9, 17 Loopback Command 0 = Port is not enabled to go to the <i>Loopback</i> Master state. 1 = Port attempts to enter the <i>Loopback</i> state as a Loopback Master. If this bit is Set before the <i>Configuration</i> state is reached, the <i>Configuration.Linkwidth.Start</i> to <i>Loopback</i> path is used. If this bit is Set later, the <i>Recovery.Idle</i> to <i>Loopback</i> path is used.	ROS	Yes	0
5	Port 9, 17 Scrambler Disable Command When Set, unconditionally disables the data scramblers on the Port's Lane(s), and causes the <i>Scramble Disable</i> Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a <i>Configuration.Complete</i> substate. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through <i>Configuration</i> again. The Upstream/Downstream device scrambler will not be disabled. 0 = Port's scrambler is enabled 1 = Port's scrambler is disabled	ROS	Yes	0
6	Port 9, 17 Compliance Receive Command 0 = When the Port transmits TS1 Ordered-Sets, the <i>Compliance Receive</i> Training Control Bit within these Ordered-Sets is not Set during the <i>Polling.Active</i> nor <i>Loopback.Entry</i> substate 1 = When the Port transmits TS1 Ordered-Sets, the <i>Compliance Receive</i> Training Control Bit within these Ordered-Sets is Set during the <i>Polling.Active</i> or <i>Loopback.Entry</i> substate	ROS	Yes	0
7	Port 9, 17 Ready as Loopback Master LTSSM established Loopback as a Master for the Port. 0 = Port is not in Loopback Master mode. 1 = Indicates that the Port has successfully transitioned to the <i>Loopback.Active</i> substate as a Loopback Master. The LTSSM remains in this substate, until bit 4 (<i>Port 9, 17 Loopback Command</i>) is Cleared. This bit is Cleared when the PEX 8747 exits the <i>Loopback.Active</i> substate.	ROS	No	0
23:8	Factory Test Only	ROS	No	0000h
31:24	Reserved	ROS	No	00h

**Register 11-97. 234h SKIP Ordered-Set Interval
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register is used to adjust the distance between SKIP Ordered-Sets.</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
11:0	<p>SKIP Ordered-Set Interval in Clocks Valid only for Gen 1 and Gen 2 Link speeds (2.5 and 5.0 GT/s, respectively).</p> <p>Specifies the SKIP Ordered-Set interval (in symbol times). When a value of 000h is written, SKIP Ordered-Set transmission is disabled.</p> <p>000h = SKIP Ordered-Set transmission is disabled 49Ch = Minimum interval (1,180 symbol times) 602h = Maximum interval (1,538 symbol times)</p> <p>Notes: <i>A high value (such as FFFh) can cause the Link to fail.</i> <i>For Gen 3 Link speed, refer to field [27:16] (SKIP Ordered-Set Interval in Blocks).</i></p>	RWS	Yes	49Ch
15:12	Reserved	RsvdP	No	0h
27:16	<p>SKIP Ordered-Set Interval in Blocks Valid only for Gen 3 Link speed (8.0 GT/s).</p> <p>Specifies the SKIP Ordered-Set interval (in block times). When a value of 000h is written, SKIP Ordered-Set transmission is disabled.</p> <p>000h = SKIP Ordered-Set transmission is disabled 173h = Minimum interval (371 block times) TBD = Maximum interval (TBD block times)</p> <p>Notes: <i>A high value (such as FFFh) can cause the Link to fail.</i> <i>For Gen 1 and Gen 2 Link speeds, refer to field [11:0] (SKIP Ordered-Set Interval in Clocks).</i></p>	RWS	Yes	173h
31:28	Reserved	RsvdP	No	0h

**Register 11-98. 238h SerDes Quad 0 Diagnostic Data
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>There are four SerDes Quad x Diagnostic Data (Diagnostic Data) registers, one per SerDes quad, at offsets 238h through 244h, in each Station. The Diagnostic Data register contents reflect the performance of the SerDes that are selected by the registers' <i>SerDes Diagnostic Data Select</i> bits (field [25:24]). For example, if offset 23Ch[25:24] is programmed to 10b, the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 22, or 38 in Stations 0, 1, and 2, respectively).</p> <p>This register is used to retrieve Diagnostic Test results for SerDes[0-3]/[16-19]/[32-35].</p> <p>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>				
7:0	UTP Expected Data When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	ROS	No	00h
15:8	UTP Actual Data When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	ROS	No	00h
23:16	UTP/PRBS Error Counter <i>The PRBS function of this field is not used.</i> Receiver Detected flags. Returns the quantity of errors detected by the UTP Data Checker. The Error Counter saturates at 255, and is Cleared when UTP is disabled. To Clear the Counter, disable UTP mode by Clearing the SerDes Quad 0 Physical Layer Test 1 register <i>SerDes Quad x Pair x User Test Pattern Enable</i> bits (Port 0, 8, or 16, offset 228h[25:24]).	ROS	No	00h
25:24	SerDes Diagnostic Data Select Used to select the SerDes (SerDes[0-3]/[16-19]/[32-35]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 0 Lanes. The test results for physical device Lanes [0-3]/[16-19]/[32-35] are selected with corresponding binary codes from 0-3. <i>Note:</i> To obtain diagnostic data on all SerDes within the quad, run a test, then cycle these bits.	RW	Yes	00b
29:26	Reserved	ROS	No	0h
30	PRBS Counter/-UTP Counter <i>The PRBS function of this bit is not used.</i> 0 = Indicates that field [23:16] (<i>UTP/PRBS Error Counter</i>) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Reserved	ROS	No	0
31	UTP Sync UTP Sync indicator.	ROS	No	0

**Register 11-99. 23Ch SerDes Quad 1 Diagnostic Data
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>There are four SerDes Quad x Diagnostic Data (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' <i>SerDes Diagnostic Data Select</i> bits (field [25:24]). <i>For example</i>, if field [25:24] of this register is programmed to 10b, the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 22, or 38 in Stations 0, 1, and 2, respectively).</p> <p>This register is used to retrieve Diagnostic Test results for SerDes[4-7]/[20-23]/[36-39].</p> <p>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>				
7:0	UTP Expected Data When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	ROS	No	00h
15:8	UTP Actual Data When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	ROS	No	00h
23:16	UTP/PRBS Error Counter <i>The PRBS function of this field is not used.</i> Receiver Detected flags. Returns the quantity of errors detected by the UTP Data Checker. The Error Counter saturates at 255, and is Cleared when UTP is disabled. To Clear the Counter, disable UTP mode by Clearing the SerDes Quad 1 Physical Layer Test 1 register <i>SerDes Quad x Pair x User Test Pattern Enable</i> bits (Port 0, 8, or 16, offset 228h [27:26]).	ROS	No	00h
25:24	SerDes Diagnostic Data Select Used to select the SerDes (SerDes[4-7]/[20-23]/[36-39]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 1 Lanes. The test results for physical device Lanes [4-7]/[20-23]/[36-39] are selected with corresponding binary codes from 0-3. Note: To obtain diagnostic data on all SerDes within the quad, run a test, then cycle these bits.	RW	Yes	00b
29:26	Reserved	ROS	No	0h
30	PRBS Counter/-UTP Counter <i>The PRBS function of this bit is not used.</i> 0 = Indicates that field [23:16] (<i>UTP/PRBS Error Counter</i>) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Reserved	ROS	No	0
31	UTP Sync UTP Sync indicator.	ROS	No	0

**Register 11-100. 240h SerDes Quad 2 Diagnostic Data
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>There are four SerDes Quad x Diagnostic Data (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' <i>SerDes Diagnostic Data Select</i> bits (field [25:24]). <i>For example</i>, if offset 23Ch[25:24] is programmed to 10b, the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 22, or 38 in Stations 0, 1, and 2, respectively).</p> <p>This register is used to retrieve Diagnostic Test results for SerDes[8-11]/[24-27]/[40-43].</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
7:0	UTP Expected Data When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	ROS	No	00h
15:8	UTP Actual Data When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	ROS	No	00h
23:16	UTP/PRBS Error Counter <i>The PRBS function of this field is not used.</i> Receiver Detected flags. Returns the quantity of errors detected by the UTP Data Checker. The Error Counter saturates at 255, and is Cleared when UTP is disabled. To Clear the Counter, disable UTP mode by Clearing the SerDes Quad 2 Physical Layer Test 1 register <i>SerDes Quad x Pair x User Test Pattern Enable</i> bits (Port 0, 8, or 16, offset 228h [29:28]).	ROS	No	00h
25:24	SerDes Diagnostic Data Select Used to select the SerDes (SerDes[8-11]/[24-27]/[40-43]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 2 Lanes. The test results for physical device Lanes [8-11]/[24-27]/[40-43] are selected with corresponding binary codes from 0-3. <i>Note:</i> To obtain diagnostic data on all SerDes within the quad, run a test, then cycle these bits.	RW	Yes	00b
29:26	Reserved	ROS	No	0h
30	PRBS Counter/-UTP Counter <i>The PRBS function of this bit is not used.</i> 0 = Indicates that field [23:16] (<i>UTP/PRBS Error Counter</i>) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Reserved	ROS	No	0
31	UTP Sync UTP Sync indicator.	ROS	No	0

**Register 11-101. 244h SerDes Quad 3 Diagnostic Data
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>There are four SerDes Quad x Diagnostic Data (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station. The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' <i>SerDes Diagnostic Data Select</i> bits (field [25:24]). <i>For example</i>, if offset 23Ch[25:24] is programmed to 10b, the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 22, or 38 in Stations 0, 1, and 2, respectively).</p> <p>This register is used to retrieve Diagnostic Test results for SerDes[12-15]/[28-31]/[44-47].</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
7:0	UTP Expected Data When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	ROS	No	00h
15:8	UTP Actual Data When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	ROS	No	00h
23:16	UTP/PRBS Error Counter <i>The PRBS function of this field is not used.</i> Receiver Detected flags. Returns the quantity of errors detected by the UTP Data Checker. The Error Counter saturates at 255, and is Cleared when UTP is disabled. To Clear the Counter, disable UTP mode by Clearing the SerDes Quad 3 Physical Layer Test 1 register <i>SerDes Quad x Pair x User Test Pattern Enable</i> bits (Port 0, 8, or 16, offset 228h [31:30]).	ROS	No	00h
25:24	SerDes Diagnostic Data Select Used to select the SerDes (SerDes[12-15]/[28-31]/[44-47]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 3 Lanes. The test results for physical device Lanes [12-15]/[28-31]/[44-47] are selected with corresponding binary codes from 0-3. <i>Note:</i> To obtain diagnostic data on all SerDes within the quad, run a test, then cycle these bits.	RW	Yes	00b
29:26	Reserved	ROS	No	0h
30	PRBS Counter/-UTP Counter <i>The PRBS function of this bit is not used.</i> 0 = Indicates that field [23:16] (<i>UTP/PRBS Error Counter</i>) is the UTP Error Counter (diagnostic data is from the UTP Data Checker) 1 = Reserved	ROS	No	0
31	UTP Sync UTP Sync indicator.	ROS	No	0

**Register 11-102. 248h Target Link Width
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register is provided to provide software with the ability to direct Link Width Up/Down configuration.</p> <p>The Port's <i>Target Link Width</i> field in this register is initially loaded with the Port's <i>Negotiated Link Width</i> (offset 78h[25:20]), the first time that the Port's LTSSM transitions from the <i>Configuration</i> state to the L0 Link PM state. The value remains 0 for Ports that are not enabled.</p> <p>Software can be used to retrain a Link to a wider or narrower width than the current width, <i>such as</i> to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets.</p> <p>If the Port's <i>Upconfigure Capability Received</i> bit is Set (indicating that during the previous Link training, the Port received Upconfigure Capability notification from the connected device), software can cause the Port to:</p> <ul style="list-style-type: none"> • Upconfigure the Link to a previously negotiated Link width, –or– • Downconfigure the Link to a narrower width <p>by writing the needed Target Link Width value to this register, followed by Setting the Port's <i>Link Control</i> register <i>Retrain Link</i> bit (Downstream Ports, offset 78h[5]). If the Target Link Width is not equal to the current Link width, the LTSSM transitions from <i>Recovery</i> to <i>Configuration</i>, then renegotiates the Link width.</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</i></p> <p><i>Port 0, bits [15 and 11:8], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
4:0	Port 0, 8, 16 Target Link Width Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, <i>such as</i> to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Port's Target Link width, to support Link Width Upconfiguration. The initial value of this field is the Port's <i>Negotiated Link Width</i> (offset 78h[25:20]).	RWS	No	Defined by STRAP_STNx_PORTCFG0 input states, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station x</i> field(s) (Port 0, offset 300h[8:6, 5:3, and/or 2:0])
6:5	Reserved	RsvdP	No	00b
7	Port 0, 8, 16 Upconfigure Capability Received Set during Link training, if the Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's <i>Link Control</i> register <i>Retrain Link</i> bit (Downstream Ports, offset 78h[5]).	ROS	No	0

**Register 11-102. 248h Target Link Width
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
11:8	Port 9, 17 Target Link Width Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, <i>such as</i> to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Port's Target Link width, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RWS	No	Defined by STRAP_STNx_PORTCFG0 input states, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station x</i> field(s) (Port 0, offset 300h[8:6 and/or 5:3])
14:12	Reserved	RsvdP	No	000b
15	Port 9, 17 Upconfigure Capability Received Set during Link training, if the Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's Link Control register <i>Retrain Link</i> bit (Downstream Ports, offset 78h[5]).	RO	No	0
31:16	Factory Test Only	RsvdP	No	0000h

**Register 11-103. 254h Physical Layer Additional Status
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bits [25 and 1], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Port x Loopback Master Entry Failed 1 = Indicates that the Port failed to enter the Loopback state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the <i>Detect</i> state	0, 8, 16	RW1C	Yes	0
1	Note: If this bit and the Port's Physical Layer Port Command register Port x Ready as Loopback Master bit (Port 0, 8, or 16, offset 230h[3 or 7]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.	9, 17	RW1C	Yes	0
5:2	Factory Test Only		RsvdP	No	0h
7:6	Reserved		RsvdP	No	00b
9:8	Link Speed 27 x 27 mm² Package Reflects the STRAP_GEN1_GEN2 input state, which indicates the Link speed.		ROS	No	STRAP_GEN1_GEN2 input state
	Field Value	STRAP_GEN1_GEN2 Input State			
	00b	0			
	01b	Z			
	10b	1			
	11b	–			
	19 x 21 mm² Package Value is always 10b, to reflect Gen 3 Link speed (8.0 GT/s).		RO	No	10 b
11:10	Reserved		RsvdP	No	00b
14:12	Link Speed Status Port Select Selects the Port within the Station for which to return Link speed status, in the Link Speed bits (bits [9:8]). 000b = Port 0 of the Station 001b = Port 1 of the Station (Stations 1 and 2 only) All other encodings are Reserved . Note: If Port 1 of the Station is not enabled, 001b is Reserved .		RW	No	000b
15	Reserved		RsvdP	No	0

**Register 11-103. 254h Physical Layer Additional Status
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
22:16	Received Modified Compliance Error Counter Returns the value received in the Modified Compliance Pattern's <i>ERR</i> field, for the Lane(s) selected by the <i>Port x Received Modified Compliance Lane Select</i> bits (bits [25:24]).		RO	No	0-0h
23	Received Modified Compliance Pattern Lock 1 = Indicates that the Modified Compliance Pattern has been locked onto by the Lane(s) selected by the <i>Port x Received Modified Compliance Lane Select</i> bits (bits [25:24]).		RO	No	0
24	Port x Received Modified Compliance Lane Select Selects which Lane receives the Modified Compliance Error Counter. Status is read from the <i>Received Modified Compliance Pattern Lock</i> bit and <i>Received Modified Compliance Error Counter</i> field (bits [23 and 22:16], respectively).	0, 8, 16	RW	Yes	0
25		9, 17	RW	Yes	0
27:26	Factory Test Only		RsvdP	No	00b
31:28	Reserved		RsvdP	No	0h

**Register 11-104. 258h Physical Layer Additional Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. <i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bits [9 and 1], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Port x External Loopback Enable 1 = Allows the Port to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when a Port’s Receivers are directly connected, externally, to its Transmitters.	0, 8, 16	RWS	No	0
1		9, 17	RWS	No	0
5:2	Factory Test Only		RsvdP	No	0h
7:6	Reserved		RsvdP	No	00b
8	Port x 2nd Receiver Detect Disable 1 = Prevents the Port from waiting 12 ms and Retrying the Receiver Detect operation, when Receivers are detected on a subset of Lanes after the first Receiver Detect operation. Instead, the LTSSM progresses to the <i>Polling</i> state, and operates only on the Lanes that detected Receivers.	0, 8, 16	RWS	Yes	0
9		9, 17	RWS	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Factory Test Only		RWS	Yes	0
17	Reserved		RsvdP	No	0
19:18	Tx Idle Minimum Time Select 00b = 20 ns (default) 01b = 30 ns 10b = 40 ns 11b = 80 ns		RWS	Yes	00b
31:20	Reserved		RsvdP	No	000h

**Register 11-105. 25Ch Physical Layer Error Injection Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register provides 1-bit error injection control.</p> <p>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, fields [7:6 and 5:4], are Factory Test Only, RsvdP, not serial EEPROM-writable, and each has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>				
1:0	Port 0, 8, 16 1-Bit Error/DLLP Error Injection 00b = Disabled (default) 01b = 1-bit error every 1 μ s 10b = 1-bit error every 1 ms 11b = Error is in the next DLLP (this value self-Clears after an error is injected in a DLLP)	RW	Yes	00b
3:2	Port 0, 8, 16 TLP Error Injection 00b = Disabled (default) 01b = Every TLP 10b = Every other TLP 11b = Every third TLP	RW	Yes	00b
5:4	Port 9, 17 1-Bit Error/DLLP Error Injection 00b = Disabled (default) 01b = 1-bit error every 1 μ s 10b = 1-bit error every 1 ms 11b = Error is in the next DLLP (this value self-Clears after an error is injected in a DLLP)	RW	Yes	00b
7:6	Port 9, 17 TLP Error Injection 00b = Disabled (default) 01b = Every TLP 10b = Every other TLP 11b = Every third TLP	RW	Yes	00b
23:8	Factory Test Only	RW	Yes	0000h
31:24	Reserved	RsvdP	No	00h

11.16.5 Device-Specific Registers – Serial EEPROM (Offsets 260h – 270h)

This section details the Device-Specific Serial EEPROM registers. [Table 11-21](#) defines the register map.

Table 11-21. Device-Specific Serial EEPROM Register Map (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
Status Data from Serial EEPROM								Serial EEPROM Status								Serial EEPROM Control																260h
Serial EEPROM Buffer																																264h
Reserved																Serial EEPROM Clock Frequency																268h
Reserved																								Serial EEPROM 3rd Address Byte								26Ch
Serial EEPROM CRC Value																																270h

Register 11-106. 260h Serial EEPROM Status and Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM	Default
Serial EEPROM Control				
12:0	EepBlkAddr Serial EEPROM Block Address for 32 KB.	RW	Yes	000h
15:13	EepCmd[2:0] Commands to the Serial EEPROM Controller. 000b = <i>Reserved</i> 001b = Data from bits [31:24] (Status Data from Serial EEPROM register) is written to the serial EEPROM's internal Status register 010b = Write four bytes of data from the EepBuf into the memory location pointed to by field [12:0] (<i>EepBlkAddr</i>) 011b = Read four bytes of data from the memory location pointed to by field [12:0] (<i>EepBlkAddr</i>) into the EepBuf 100b = Reset Write Enable latch 101b = Data from the serial EEPROM's internal Status register is written to bits [31:24] (Status Data from Serial EEPROM register) 110b = Set Write Enable latch 111b = <i>Reserved</i> <i>Note: For value of 001b, only bits [31, 27:26] can be written into the serial EEPROM's internal Status register.</i>	RW	Yes	000b

**Register 11-106. 260h Serial EEPROM Status and Control
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM	Default	
Serial EEPROM Status					
17:16	EepPrsnt[1:0] Serial EEPROM Present status. 00b = Not present 01b = Serial EEPROM is present – Validation Signature is verified 10b = <i>Reserved</i> 11b = Serial EEPROM is present – Validation Signature is not verified	ROS	No	00b	
18	EepCmdStatus Serial EEPROM Command status. 0 = Serial EEPROM Command is complete 1 = Serial EEPROM Command is not complete	ROS	No	0	
19	EepCRCErr CRC error detected status.	RW1CS	No	0	
20	EepBlkAddr Upper Bit Serial EEPROM Block Address upper bit 13. Extends the serial EEPROM to 64 KB.	RW	Yes	0	
21	EepAddrWidth Override 0 = Field [23:22] (<i>EepAddrWidth</i>) is RO 1 = Field [23:22] (<i>EepAddrWidth</i>) is software-writable	RW	Yes	0	
23:22	EepAddrWidth Serial EEPROM Address width. If the addressing width cannot be determined, 00b is returned. A non-zero value is reported only if the Validation Signature (5Ah) is successfully read from the first serial EEPROM location. This field is usually ROS; however, it is RW if bit 21 (<i>EepAddrWidth Override</i>) is Set. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	Bit 21 = 0	ROS	No	00b
	Bit 21 = 1	RW	No	00b	

**Register 11-106. 260h Serial EEPROM Status and Control
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM	Default					
Status Data from Serial EEPROM ^a									
24	EepRdy Serial EEPROM RDY#. 0 = Serial EEPROM is ready to transmit data 1 = Write cycle is in-progress	RW	Yes	0					
25	EepWen Serial EEPROM Write enable. 0 = Serial EEPROM Write is disabled 1 = Serial EEPROM Write is enabled	RW	Yes	0					
27:26	EepBp[1:0] Serial EEPROM Block-Write Protect bits. Block Protection options protect the top ¼, top ½, or the entire serial EEPROM. PEX 8747 Configuration data is stored in the lower addresses; therefore, when using Block Protection, the entire serial EEPROM should be protected with BP[1:0]=11b.		RW	Yes	00b				
	BP[1:0]	Level				Array Addresses Protected, by Device Size			
						8 KB	16 KB	32 KB	64 KB
	00b	0				None	None	None	None
	01b	1 (top ¼)				1800h – 1FFFh	3000h – 3FFFh	6000h – 7FFFh	–
	10b	2 (top ½)				1000h – 1FFFh	2000h – 3FFFh	4000h – 7FFFh	–
	11b	3 (All)	0000h – 1FFFh	0000h – 3FFFh	0000h – 7FFFh	–			

Register 11-106. 260h Serial EEPROM Status and Control (Port 0) (Cont.)

Bit(s)	Description	Type	Serial EEPROM	Default
30:28	EepWrStatus Serial EEPROM Write status. Value is 000b when the serial EEPROM is not in an internal Write cycle. <i>Note: The definition of this field varies among serial EEPROM manufacturers. Reads of the serial EEPROM's internal Status register can return a value of 000b or 111b, depending upon the serial EEPROM that is used.</i>	RW	No	000b
31	EepWpen Serial EEPROM Write Protect enable. Overrides the internal serial EEPROM Write Protect WP# input and enables/disables Writes to the Serial EEPROM Status register (bits [23:16] of this register): <ul style="list-style-type: none"> When WP#=H or this bit is Cleared, and bit 25 (<i>EepWen</i>) is Set, the Serial EEPROM Status register is writable When WP#=L and this bit is Set, or bit 25 (<i>EepWen</i>) is Cleared, the Serial EEPROM Status register is write-protected <i>Notes: If the internal serial EEPROM Write Protect WP# input is Low, after software Sets the EepWen bit to write-protect the Serial EEPROM Status register, the EepWen value cannot be Cleared, nor can the <i>EepBp[1:0]</i> field be Cleared to disable Block Protection, until the WP# input is High.</i> <i>This bit is not implemented in certain serial EEPROMs. Refer to the serial EEPROM manufacturer's data sheet.</i>	RW	Yes	0

a. Within the serial EEPROM's internal **Status** register, only bits [31, 27:26] can be written.

Register 11-107. 264h Serial EEPROM Buffer (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	EepBuf Serial EEPROM RW buffer. Read/Write command to the Serial EEPROM Control register (Port 0, offset 260h) results in a 4-byte Read/Write from/to the serial EEPROM device.	RW	Yes	0000_0000h

Register 11-108. 268h Serial EEPROM Clock Frequency (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
2:0	EepFreq[2:0] Serial EEPROM clock (EE_SK) frequency control. 000b = 1 MHz (default) 001b = 1.98 MHz 010b = 5 MHz 011b = 9.62 MHz 100b = 12.5 MHz 101b = 15.6 MHz 110b = 17.86 MHz 111b = Reserved	RW	Yes	000b
7:3	Reserved	RsvdP	No	0-0h
10:8	EepCsStHld[2:0] CS to SCLK setup and hold timing, provided as a quantity of ½ EE_SK Clock cycles. 000b = Use default timing for EE_CS# setup and EE_CS# hold timing to the serial EEPROM, for EE_CS# active to EE_SK active delay, and EE_SK inactive to EE_CS# inactive delay, respectively 001b = Non-zero value adds that quantity of ½ EE_SK clocks delay to the default setup and hold timing, between EE_CS# active and EE_SK active, and between EE_SK inactive and EE_CS# inactive	RW	Yes	000b
31:11	Reserved	RsvdP	No	0-0h

Register 11-109. 26Ch Serial EEPROM 3rd Address Byte (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	Serial EEPROM 3rd Address Byte Contains the upper Byte address when reading from or writing to a 3-address byte serial EEPROM.	RW	Yes	00h
31:8	<i>Reserved</i>	RsvdP	No	0000_00h

Register 11-110. 270h Serial EEPROM CRC Value (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	EepCRCValue Calculated serial EEPROM CRC value. There is an optional CRC checking at the end of serial EEPROM auto load. Bit 7 of the second byte (after the 5Ah Validation Signature) determines whether CRC checking is to be performed. The calculated CRC value is always placed into this register after serial EEPROM auto load. If CRC checking is enabled, and the stored 32-bit CRC value read from the end the serial EEPROM content does not match the calculated value, an Uncorrectable Internal error is triggered at Port 0 of Station 0.	HwInit	Yes	FFFF_FFFFh

11.16.6 Device-Specific Registers – I²C and SMBus Slave Interfaces (Offsets 290h – 2FCh)

This section details the Device-Specific I²C and SMBus Slave Interface registers. [Table 11-22](#) defines the register map.

The I²C and SMBus Slave Interfaces are described, in detail, in [Chapter 7, “I²C/SMBus Slave Interface Operation.”](#)

Table 11-22. Device-Specific I²C and SMBus Slave Interfaces Register Map (Port 0)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<i>Factory Test Only</i>																290h															
<i>I²C Configuration</i>																294h															
<i>Factory Test Only</i>																298h – 2C4h															
<i>SMBus Configuration</i>																2C8h															
<i>Reserved</i>																2CCh – 2FCh															

Register 11-111. 294h I²C Configuration (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default								
6:0	<p>Slave Address</p> <p>Default I²C Slave/SMBus Device address, which is dependent upon the I2C_ADDR0 input state.</p> <table><thead><tr><th>I2C_ADDR0 Input State</th><th>I²C Slave/SMBus Device Address</th></tr></thead><tbody><tr><td>0</td><td>0111_000b</td></tr><tr><td>Z</td><td>0111_001b</td></tr><tr><td>1</td><td>0111_010b</td></tr></tbody></table> <p>Other values can be programmed as well, by serial EEPROM or Memory Write. Additionally, Silicon Revision CA supports access to this field, through Configuration Requests.</p> <p><i>Note: The I²C Slave/SMBus Device address must not be changed by an I²C/SMBus Write command.</i></p>	I2C_ADDR0 Input State	I ² C Slave/SMBus Device Address	0	0111_000b	Z	0111_001b	1	0111_010b	RWS	Yes	Refer to Table
I2C_ADDR0 Input State	I ² C Slave/SMBus Device Address											
0	0111_000b											
Z	0111_001b											
1	0111_010b											
9:7	Reserved	RsvdP	No	000b								
10	Factory Test Only	RWS	Yes	0								
30:11	Reserved	RWS	Yes	0-0h								
31	Factory Test Only	ROS	No	0								

Register 11-112. 2C8h SMBus Configuration (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
0	SMBus Enable Initially loaded from the STRAP_I2C_SMBUS_EN input state. The value can later be changed by software, serial EEPROM, I ² C, and/or SMBus. 0 = Disables SMBus for device configuration (I ² C mode is enabled) 1 = Enables SMBus for device configuration (SMBus mode is enabled)	RWS	Yes	0 (STRAP_I2C_SMBUS_EN=Z or 1) 1 (STRAP_I2C_SMBUS_EN=0)
7:1	SMBus Device Address Defined by the Address Resolution Protocol (ARP) Master, if ARP is enabled. Defaults to 0011_100b if ARP is disabled (STRAP_I2C_SMBUS_EN=0 and bit 8 (ARP Disable) is Set). When disabled, the serial EEPROM should simultaneously: <ul style="list-style-type: none"> Set bits [15, 11, and 10 (SMBus Parameter Reload, AR Flag, and AV Flag, respectively), and, Program this field to the SMBus address for this device (<i>such as</i> to 70h, to match the I²C Slave Address (I2C Configuration register Slave Address field (Port 0, offset 294h[6:0])) default value) An 8 th bit is transmitted immediately following the 7-bit address, to signal whether the instruction is Write (0) or Read (1). Therefore, when accessing the default I ² C Slave address 0111_000b , the transmitted byte value is 70h for a Write instruction and 71h for a Read instruction.	RWS	Yes	0000_000b (STRAP_I2C_SMBUS_EN=Z or 1) 0011_100b (STRAP_I2C_SMBUS_EN=0 and bit 8 (ARP Disable) is Set)
8	ARP Disable 0 = Device under test is able to respond to ARP commands 1 = Device under test is unable to respond to ARP commands	RWS	Yes	1
9	PEC Check Disable 0 = Enable PEC checking on all packets 1 = Disables Packet Error Checks (PECs) checking on all packets; packets with the wrong PECs are accepted	RWS	Yes	0
10	AV Flag Address Valid (AV) flag. Set, by default, when ARP is disabled (STRAP_I2C_SMBUS_EN=0 and bit 8 (ARP Disable) is Set).	RWS	Yes	1
11	AR Flag Address Resolved (AR) flag.	RWS	Yes	0

**Register 11-112. 2C8h SMBus Configuration
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
13:12	UDID Address Type Unique Device Identifier (UDID) Address type. 00b = ARP is disabled (STRAP_I2C_SMBUS_EN=0 and bit 8 (<i>ARP Disable</i>) is Set) 10b = ARP is enabled (STRAP_I2C_SMBUS_EN=Z or 1) All other encodings are <i>Reserved</i> .	RWS	Yes	00b (STRAP_I2C_SMBUS_EN=0 and bit 8 (<i>ARP Disable</i>) is Set) 10b (STRAP_I2C_SMBUS_EN=Z or 1)
14	UDID PEC Support 1 = Sets the <i>PEC Support</i> bit in the UDID	RWS	Yes	1
15	SMBus Parameter Reload Software must Set this bit if bits [10, 8, and/or 7:1] (<i>AV Flag</i> , <i>ARP Disable</i> , and/or <i>SMBus Device Address</i> , respectively) at runtime. Effective only when bit 28 (<i>SMBus Command In-Progress</i>) is Cleared.	ROS	No	0
23:16	UDID Vendor-Specific ID Defines the MSB of the UDID Vendor-Specific ID. Bits [23:20] of this field are defined by the <i>I2C_ADDR0</i> input state, which provides the following ID values. 0 = 7000_0000h Z = B000_0000h 1 = D000_0000h	RWS	Yes	Defined by <i>I2C_ADDR0</i> input state
26:24	UDID Version UDID version defined for the <i>SMBus v2.0</i> .	RWS	Yes	001b
27	Factory Test Only	RWS	Yes	0
28	SMBus Command In-Progress 0 = SMBus state machine is idle 1 = SMBus state machine is active (not idle)	ROS	No	0
29	PEC Check Failed 0 = PEC check successfully completed when receiving a packet 1 = PEC check failed when receiving a packet	RW1C	No	0
30	Unsupported SMBus Command 0 = Command received from SMBus is a supported command 1 = Command received from SMBus is an unsupported command	RW1C	No	0
31	SMBus Error Detected 0 = No error detected in STOP condition (as generated by the SMBus Master, to terminate the Data transfer) 1 = STOP detected was not on a byte boundary	RW1C	Yes	0

11.16.7 Device-Specific Registers – Port Configuration and Lane Status (Offsets 300h – 350h)

This section details Device-Specific Port Configuration and Lane Status registers at offsets 300h through 350h. Table 11-23 defines the register map.

Other Device-Specific Port Configuration and Lane Status registers are detailed in Section 11.16.8, “Device-Specific Registers – Port Configuration (Offsets 354h – 46Ch).”

Table 11-23. Device-Specific Port Configuration and Lane Status Register Map (Offsets 300h – 350h) (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Port Configuration																																				300h
Reserved																																				304h – 308h
Factory Test Only																																				30Ch – 310h
Clock Enable																																				314h
Factory Test Only																																				318h – 32Ch
Station 0/1 Lane Status																																				330h
Reserved																Station 2 Lane Status																				334h
Factory Test Only																																				338h – 350h

Register 11-113. 300h Port Configuration (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>Notes: <i>Table 11-5 lists the Port configurations for each Station. The table also indicates which Ports and SerDes/Lanes are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i></p> <p><i>In the values listed for each field, the second value is the Port Configuration Number, as listed in Table 11-5 (for example, 001b is equivalent to Port Configuration 1).</i></p>				
2:0	<p>Port Configuration for Station 0</p> <p>Port Configuration Link width for Station 0, Port 0. This register is reset only by a Fundamental Reset (PEX_PERST# assertion).</p> <p>001b = 1 = x16</p> <p>All other encodings are <i>Reserved</i>.</p>	ROS	Yes	001b
5:3	<p>Port Configuration for Station 1</p> <p>Port Configuration Link width, per Port, for Station 1. The serial EEPROM bit values always override the STRAP_STN1_PORTCFG0 input states (if the serial EEPROM values are loaded; refer to Table 11-5).</p> <p>This register is reset only by a Fundamental Reset (PEX_PERST# assertion).</p> <p>001b = 1 = x16</p> <p>010b = 2 = x8x8</p> <p>All other encodings are <i>Reserved</i>.</p>	ROS	Yes	Defined by STRAP_STN1_PORTCFG0 input states
8:6	<p>Port Configuration for Station 2</p> <p>Port Configuration Link width, per Port, for Station 2. The serial EEPROM bit values always override the STRAP_STN2_PORTCFG0 input state (if the serial EEPROM values are loaded; refer to Table 11-5).</p> <p>This register is reset only by a Fundamental Reset (PEX_PERST# assertion).</p> <p>001b = 1 = x16</p> <p>010b = 2 = x8x8</p> <p>All other encodings are <i>Reserved</i>.</p>	ROS	Yes	Defined by STRAP_STN2_PORTCFG0 input state
31:9	<i>Reserved</i>	RsvdP	No	0-0h

**Register 11-114. 314h Clock Enable
(Port 0)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>Ports and Stations are automatically enabled, according to the Port configuration defined by the STRAP_STNx_PORTCFG0 3-state inputs, which can be overridden by programming the Station's Port Configuration register <i>Port Configuration for Station x</i> field (Port 0, offset 300h[8:6, 5:3, and/or 2:0]).</p> <p>An enabled Port can be selectively disabled, however, by Clearing the Port's <i>Port x Clock Enable</i> bit within this register. Port 0 must always remain enabled, and Ports 8 and 16 (containing Station-specific registers) must remain enabled, if other Ports within their respective Stations are enabled.</p> <p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include "Port x" in their name. <i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p> <p><i>It is not possible to enable more Ports than the maximum specified for the device.</i></p>					
0	Port x Clock Enable 0 = Disables 1 = Enables	0	RWS	Yes	1
5:1	Factory Test Only		RsvdP	No	0-0h
7:6	Reserved		RsvdP	No	00b
8	Port x Clock Enable 0 = Disables 1 = Enables	8	RWS	Yes	Defined by STRAP_STN1_PORTCFG0 input state, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station 1</i> field (Port 0, offset 300h[5:3])
9		9	RWS	Yes	
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Port x Clock Enable 0 = Disables 1 = Enables	16	RWS	Yes	Defined by STRAP_STN2_PORTCFG0 input state, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station 2</i> field (Port 0, offset 300h[8:6])
17		17	RWS	Yes	
21:18	Factory Test Only		RsvdP	No	0h
23:22	Reserved		RsvdP	No	00b
24	Station 1 Root Clock Enable		RWS	Yes	Defined by STRAP_STN1_PORTCFG0 input state, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station 1</i> field (Port 0, offset 300h[5:3])
25	Station 2 Root Clock Enable		RWS	Yes	Defined by STRAP_STN2_PORTCFG0 input state, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station 2</i> field (Port 0, offset 300h[8:6])
31:26	Factory Test Only/Reserved		RsvdP	No	0-0h

**Register 11-115. 330h Station 0/1 Lane Status
(Port 0)**

Bit(s)	Description	Lane x	Type	Serial EEPROM and I ² C	Default
<i>Notes: The Lane x column is provided to indicate the Lane Number associated with each bit.</i> <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Ports, SerDes modules, and Lanes.</i>					
0	Lane x Up Status 0 = Lane is Down 1 = Lane is Up	0	ROS	Yes	1
1		1	ROS	Yes	1
2		2	ROS	Yes	1
3		3	ROS	Yes	1
4		4	ROS	Yes	1
5		5	ROS	Yes	1
6		6	ROS	Yes	1
7		7	ROS	Yes	1
8		8	ROS	Yes	1
9		9	ROS	Yes	1
10		10	ROS	Yes	1
11		11	ROS	Yes	1
12		12	ROS	Yes	1
13		13	ROS	Yes	1
14		14	ROS	Yes	1
15		15	ROS	Yes	1

**Register 11-115. 330h Station 0/1 Lane Status
(Port 0) (Cont.)**

Bit(s)	Description	Lane x	Type	Serial EEPROM and I ² C	Default
16	Lane x Up Status 0 = Lane is Down 1 = Lane is Up	16	ROS	Yes	1
17		17	ROS	Yes	1
18		18	ROS	Yes	1
19		19	ROS	Yes	1
20		20	ROS	Yes	1
21		21	ROS	Yes	1
22		22	ROS	Yes	1
23		23	ROS	Yes	1
24		24	ROS	Yes	1
25		25	ROS	Yes	1
26		26	ROS	Yes	1
27		27	ROS	Yes	1
28		28	ROS	Yes	1
29		29	ROS	Yes	1
30		30	ROS	Yes	1
31		31	ROS	Yes	1

**Register 11-116. 334h Station 2 Lane Status
(Port 0)**

Bit(s)	Description	Lane x	Type	Serial EEPROM and I ² C	Default
<i>Notes: The Lane x column is provided to indicate the Lane Number associated with each bit.</i> <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Ports, SerDes modules, and Lanes.</i>					
0	Lane x Up Status 0 = Lane is Down 1 = Lane is Up	32	ROS	Yes	1
1		33	ROS	Yes	1
2		34	ROS	Yes	1
3		35	ROS	Yes	1
4		36	ROS	Yes	1
5		37	ROS	Yes	1
6		38	ROS	Yes	1
7		39	ROS	Yes	1
8		40	ROS	Yes	1
9		41	ROS	Yes	1
10		42	ROS	Yes	1
11		43	ROS	Yes	1
12		44	ROS	Yes	1
13		45	ROS	Yes	1
14		46	ROS	Yes	1
15		47	ROS	Yes	1
31:16	Reserved		RsvdP	No	0000h

11.16.8 Device-Specific Registers – Port Configuration (Offsets 354h – 46Ch)

This section details the Device-Specific Port Configuration registers located at offsets 354h through 46Ch. [Table 11-24](#) defines the register map.

Other Device-Specific Port Configuration registers are detailed in [Section 11.16.7, “Device-Specific Registers – Port Configuration and Lane Status \(Offsets 300h – 350h\).”](#)

Table 11-24. Device-Specific Port Configuration Register Map (Offsets 354h – 46Ch)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
<i>Reserved</i>																354h – 35Ch																
Upstream Port																360h																
<i>Factory Test Only</i>																364h – 37Ch																
Port Vector																380h																
<i>Reserved</i>																384h – 39Ch																
Port Reset																3A0h																
<i>Reserved</i>																3A4h – 3A8h																
Configuration Release																3ACh																
<i>Factory Test Only/Reserved</i>																3B0h – 468h																
Strap Configuration																46Ch																

Register 11-117. 360h Upstream Port (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default																		
This register defines the Upstream Port, and can be programmed, prior to linkup, using any of the following methods:																						
<ul style="list-style-type: none">Serial EEPROMI²C, if STRAP_I2C_SMBUS_CFG_EN#=L, followed by an I²C Write that Sets the Configuration Release register Initiate Configuration bit (Port 0, offset 3ACh[0])Software, followed by a Hot Reset																						
Note: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.																						
4:0	Upstream Port 27 x 27 mm² Package Identifies the Upstream Port, based upon the STRAP_UPSTRM_PORTSEL[2:0] input states.	RWS	Yes	Defined by STRAP_UPSTRM_PORTSEL[2:0] input states																		
	<table><thead><tr><th>Field Value</th><th>STRAP_UPSTRM_PORTSEL[2:0] Input States</th><th>Port Number</th></tr></thead><tbody><tr><td>0_0000b</td><td>000</td><td>0</td></tr><tr><td>0_1000b</td><td>011</td><td>8</td></tr><tr><td>0_1001b</td><td>Z00</td><td>9</td></tr><tr><td>1_0000b</td><td>Z1Z</td><td>16</td></tr><tr><td>1_0001b</td><td>Z11</td><td>17</td></tr></tbody></table> 19 x 21 mm² Package Identifies the Upstream Port, based upon the STRAP_UPSTRM_PORTSEL[1:0] input states.				Field Value	STRAP_UPSTRM_PORTSEL[2:0] Input States	Port Number	0_0000b	000	0	0_1000b	011	8	0_1001b	Z00	9	1_0000b	Z1Z	16	1_0001b	Z11	17
Field Value	STRAP_UPSTRM_PORTSEL[2:0] Input States	Port Number																				
0_0000b	000	0																				
0_1000b	011	8																				
0_1001b	Z00	9																				
1_0000b	Z1Z	16																				
1_0001b	Z11	17																				
	<table><thead><tr><th>Field Value</th><th>STRAP_UPSTRM_PORTS EL[1:0] Input States^a</th><th>Port Number</th></tr></thead><tbody><tr><td>0_0000b</td><td>00</td><td>0</td></tr><tr><td>0_1000b</td><td>11</td><td>8</td></tr><tr><td>0_1001b</td><td>–</td><td>9</td></tr><tr><td>1_0000b</td><td>–</td><td>16</td></tr><tr><td>1_0001b</td><td>–</td><td>17</td></tr></tbody></table> <i>a. The STRAP_UPSTRM_PORTSEL[1:0] inputs select either Port 0 or Port 8 as the Upstream Port; if Port 9, 16, or 17 is needed as the Upstream Port, use the serial EEPROM (if present) and/or I²C/SMBus (when STRAP_I2C_SMBUS_CFG_EN# input is asserted), to program this field accordingly.</i> All other encodings are Reserved .	Field Value	STRAP_UPSTRM_PORTS EL[1:0] Input States ^a	Port Number	0_0000b	00	0	0_1000b	11	8	0_1001b	–	9	1_0000b	–	16	1_0001b	–	17			
Field Value	STRAP_UPSTRM_PORTS EL[1:0] Input States ^a	Port Number																				
0_0000b	00	0																				
0_1000b	11	8																				
0_1001b	–	9																				
1_0000b	–	16																				
1_0001b	–	17																				
7:5	Factory Test Only	RWS	Yes	000b																		

**Register 11-117. 360h Upstream Port
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
23:8	<i>Factory Test Only</i>	RWS	Yes	1A1Ah
25:24	<i>Factory Test Only</i>	RWS	Yes	00b
29:26	<i>Reserved</i>	RsvdP	No	0h
31:30	<i>Factory Test Only</i>	RWS	Yes	00b

**Register 11-118. 380h Port Vector
(Port 0)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>This register can be programmed, prior to linkup, using any of the following methods:</p> <ul style="list-style-type: none"> Serial EEPROM I²C, if STRAP_I2C_SMBUS_CFG_EN#=L, followed by an I²C Write that Sets the Configuration Release register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]) Software, followed by a Hot Reset <p>The default value of this register is 00FF_FFFFh.</p> <p>Note: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name.</p>					
0	Active Port x	0	RWS	Yes	Based upon STRAP_TESTMODE0 input state
5:1	Factory Test Only		RsvdP	No	0-0h
7:6	Reserved		RsvdP	No	00b
8	Active Port x	8	RWS	Yes	Based upon STRAP_TESTMODE0 input state
9		9	RWS	Yes	
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Active Ports	16	RWS	Yes	Based upon STRAP_TESTMODE0 input state
17		17	RWS	Yes	
21:18	Factory Test Only		RsvdP	No	0h
31:22	Reserved		RsvdP	No	0-0h

**Register 11-119. 3A0h Port Reset
(Port 0)**

Bit(s)	Description	Downstream Port <i>x</i>	Type	Serial EEPROM and I ² C	Default
When driven with a value of 1, this register holds the Port in reset, including the Port PCI-to-PCI bridge and the hierarchy below it. A value of 0 indicates to un-reset the PCI-to-PCI bridge and the hierarchy below it.					
<i>Notes:</i> The Downstream Port <i>x</i> column is provided to indicate the Port Number associated with bits/fields that include “Port <i>x</i> ” in their name.					
<i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i>					
0	Reset Port <i>x</i> Vector 0 = Port is not reset 1 = Port is reset	0	RWS	Yes	0
5:1	Factory Test Only		RsvdP	No	0-0h
7:6	Reserved		RsvdP	No	00b
8	Reset Port <i>x</i> Vector 0 = Port is not reset 1 = Port is reset	8	RWS	Yes	0
9		9	RWS	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Reset Port <i>x</i> Vector 0 = Port is not reset 1 = Port is reset	16	RWS	Yes	0
17		17	RWS	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
31:22	Reserved		RsvdP	No	0-0h

**Register 11-120. 3ACh Configuration Release
(Port 0)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
0	Initiate Configuration If the STRAP_I2C_SMBUS_CFG_EN# input is pulled or tied Low to VSS (Ground), I ² C is being used to configure the PEX 8747. After I ² C has completed its configuration, it must write to this bit, to release the hold that is preventing the Links from coming up. 0 = STRAP_I2C_SMBUS_CFG_EN# =0 1 = STRAP_I2C_SMBUS_CFG_EN# =1, releases the hold that prevents the Links from coming up	HwInit	Yes	0
31:1	Reserved	RsvdP	No	0-0h

Register 11-121. 46Ch Strap Configuration (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4:0	Factory Test Only	HwInit	Yes	0-0h
5	I²C Configuration Enable Status 0 = I ² C/SMBus Configuration is disabled (STRAP_I2C_SMBUS_CFG_EN#=H) 1 = I ² C/SMBus Configuration is enabled (STRAP_I2C_SMBUS_CFG_EN#=L)	ROS	Yes	PCFG
6	SMBus Enable Status 0 = I ² C protocol is enabled (STRAP_I2C_SMBUS_EN=0) 1 = SMBus protocol is enabled (STRAP_I2C_SMBUS_EN=Z or 1)	ROS	Yes	PCFG
7	Reserved	RsvdP	No	0
9:8	Factory Test Only	ROS	Yes	11b
10	Gen 1 Compatible Disable Status Value is dependent upon the SPARE2 input. 0 = Enable Gen 1 Compatible mode, to accommodate a connected, non-compliant Gen 1 device (SPARE2=L) 1 = Disable Gen 1 Compatible mode, for non-compliant Gen 1 device (SPARE2=H)	ROS	Yes	0 (SPARE2=L) 1 (SPARE2=H)
11	Gen 1 Mode Status 27 x 27 mm² Package Value is dependent upon the STRAP_GEN1_GEN2 input. 0 = Link speed is 2.5 GT/s (STRAP_GEN1_GEN2=0) 1 = Maximum Link speed is 5.0 or 8.0 GT/s (STRAP_GEN1_GEN2=Z or 1, respectively) 19 x 21 mm² Package Value is always 1, to enable Gen 3 Link speed (8.0 GT/s).	ROS	Yes	PCFG
12	Gen 2 Mode Status 27 x 27 mm² Package Value is dependent upon the STRAP_GEN1_GEN2 input. 0 = Maximum Link speed is 5.0 GT/s (STRAP_GEN1_GEN2=Z) 1 = Maximum Link speed is 8.0 GT/s (STRAP_GEN1_GEN2=1) 19 x 21 mm² Package Value is always 1, to enable Gen 3 Link speed (8.0 GT/s).	ROS	Yes	PCFG
15:13	Reserved	RsvdP	No	000b

**Register 11-121. 46Ch Strap Configuration
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
20:16	<i>Factory Test Only</i>	ROS	No	PCFG
23:21	<i>Reserved</i>	RsvdP	No	000b
28:24	Strap Test Mode Status Reflects the STRAP_TESTMODE0 input state. 00000b = 0 00010b = 1 Encoding 00001b is <i>Factory Test Only</i> . Encodings 00011b and above are <i>Reserved</i> .	ROS	No	Based upon STRAP_TESTMODE0 input state
31:29	<i>Reserved</i>	RsvdP	No	000b

This section details the Device-Specific General-Purpose Input/Output (GPIO) registers. [Table 11-25](#) defines the register map.

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

GPIO 0_9 Direction Control	600h
GPIO 10 Direction Control	604h
<i>Reserved</i>	608h –
GPIO 0_10 Input De-Bounce	614h
<i>Reserved</i>	618h
GPIO 0_10 Input Data	61Ch
<i>Reserved</i>	620h
GPIO 0_10 Output Data	624h
<i>Reserved</i>	628h
GPIO 0_10 Interrupt Polarity	62Ch
<i>Reserved</i>	630h
GPIO 0_10 Interrupt Status	634h
<i>Reserved</i>	638h
GPIO 0_10 Interrupt Mask	63Ch
<i>Reserved</i>	640h – 68Ch

Register 11-122. 600h GPIO 0_9 Direction Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The GPIO 0_9 Direction Control registers control the direction, source, and destination of the PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], and PORT_GOOD[8:9]# signals, respectively.</p> <p>Notes: Register offsets 61Ch and 624h, referenced within this register, are located as follows – Port 0.</p> <p>PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>				
1:0	PORT_GOOD0# Source/Destination As Input: 00b = To PORT_GOOD0# Input Data register (offset 61Ch [0]) 01b = General interrupt (INTx, MSI, or PEX_INTA)# 10b, 11b = Reserved As Output: 00b = From PORT_GOOD0# Output Data register (offset 624h [0]) 01b = PORT_GOOD0# 10b, 11b = Reserved	RWS	Yes	TBD
2	PORT_GOOD0# Direction Control 0 = Input 1 = Output	RWS	Yes	TBD
4:3	GPIO1 Source/Destination As Input: 00b = To GPIO1 Input Data register (offset 61Ch [1]) 01b = General interrupt (INTx, MSI, or PEX_INTA)# 10b, 11b = Reserved As Output: 00b = From GPIO1 Output Data register (offset 624h [1]) 01b = GPIO1 10b, 11b = Reserved	RWS	Yes	TBD
5	GPIO1 Direction Control 0 = Input 1 = Output	RWS	Yes	TBD

Register 11-122. 600h GPIO 0_9 Direction Control (Port 0) (Cont.)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:6	GPIO2 Source/Destination As Input: 00b = To GPIO2 Input Data register (offset 61Ch[2]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From GPIO2 Output Data register (offset 624h[2]) 01b = GPIO2 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
8	GPIO2 Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
10:9	GPIO3 Source/Destination As Input: 00b = To GPIO3 Input Data register (offset 61Ch[3]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From GPIO3 Output Data register (offset 624h[3]) 01b = GPIO3 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
11	GPIO3 Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
13:12	PORT_GOOD4# Source/Destination As Input: 00b = To PORT_GOOD4# Input Data register (offset 61Ch[4]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From PORT_GOOD4# Output Data register (offset 624h[4]) 01b = PORT_GOOD4# 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
14	PORT_GOOD4# Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>

**Register 11-122. 600h GPIO 0_9 Direction Control
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
16:15	PORT_GOOD5# Source/Destination As Input: 00b = To PORT_GOOD5# Input Data register (offset 61Ch[5]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From PORT_GOOD5# Output Data register (offset 624h[5]) 01b = PORT_GOOD5# 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
17	PORT_GOOD5# Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
19:18	GPIO6 Source/Destination As Input: 00b = To GPIO6 Input Data register (offset 61Ch[6]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From GPIO6 Output Data register (offset 624h[6]) 01b = GPIO6 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
20	GPIO6 Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
22:21	GPIO7 Source/Destination As Input: 00b = To GPIO7 Input Data register (offset 61Ch[7]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From GPIO7 Output Data register (offset 624h[7]) 01b = GPIO7 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
23	GPIO7 Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>

Register 11-122. 600h GPIO 0_9 Direction Control (Port 0) (Cont.)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
25:24	PORT_GOOD8# Source/Destination As Input: 00b = To PORT_GOOD8# Input Data register (offset 61Ch[8]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From PORT_GOOD8# Output Data register (offset 624h[8]) 01b = PORT_GOOD8# 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
26	PORT_GOOD8# Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
28:27	PORT_GOOD9# Source/Destination As Input: 00b = To PORT_GOOD9# Input Data register (offset 61Ch[9]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From PORT_GOOD9# Output Data register (offset 624h[9]) 01b = PORT_GOOD9# 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
29	PORT_GOOD9# Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
31:30	<i>Reserved</i>	RsvdP	No	00b

Register 11-123. 604h GPIO 10 Direction Control (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The GPIO 10 Direction Control register controls the direction, source, and destination of the GPIO10 signal.</p> <p><i>Notes:</i> Register offsets 61Ch and 624h, referenced within this register, are located as follows – Port 0.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>				
1:0	GPIO10 Source/Destination As Input: 00b = To GPIO10 Input Data register (offset 61Ch [10]) 01b = General interrupt (INTx, MSI, or PEX_INTA#) 10b, 11b = <i>Reserved</i> As Output: 00b = From GPIO10 Output Data register (offset 624h [10]) 01b = GPIO10 10b, 11b = <i>Reserved</i>	RWS	Yes	<i>TBD</i>
2	GPIO10 Direction Control 0 = Input 1 = Output	RWS	Yes	<i>TBD</i>
31:3	<i>Reserved</i>	RsvdP	No	0-0h

Register 11-124. 614h GPIO 0_10 Input De-Bounce (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], PORT_GOOD[8:9]#, and GPIO10 signals are de-bounced, using the GPIO 0_10 Input De-Bounce registers, respectively.</p> <p><i>Notes: Register offsets 600h and 604h, referenced within this register, are located as follows – Port 0.</i></p> <p><i>PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h).</i></p> <p><i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i></p>				
0	<p>PORT_GOOD0# Input De-Bounce Control</p> <p>Controls de-bounce when PORT_GOOD0# is configured as an input (offset 600h[2], is Cleared).</p> <p>0 = PORT_GOOD0# input is not de-bounced</p> <p>1 = PORT_GOOD0# input is de-bounced; de-bounce time is approximately 1.3 ms</p>	RWS	Yes	0
1	<p>GPIO1 Input De-Bounce Control</p> <p>Controls de-bounce when GPIO1 is configured as an input (offset 600h[5], is Cleared).</p> <p>0 = GPIO1 input is not de-bounced</p> <p>1 = GPIO1 input is de-bounced; de-bounce time is approximately 1.3 ms</p>	RWS	Yes	0
2	<p>GPIO2 Input De-Bounce Control</p> <p>Controls de-bounce when GPIO2 is configured as an input (offset 600h[8], is Cleared).</p> <p>0 = GPIO2 input is not de-bounced</p> <p>1 = GPIO2 input is de-bounced; de-bounce time is approximately 1.3 ms</p>	RWS	Yes	0
3	<p>GPIO3 Input De-Bounce Control</p> <p>Controls de-bounce when GPIO3 is configured as an input (offset 600h[11], is Cleared).</p> <p>0 = GPIO3 input is not de-bounced</p> <p>1 = GPIO3 input is de-bounced; de-bounce time is approximately 1.3 ms</p>	RWS	Yes	0

**Register 11-124. 614h GPIO 0_10 Input De-Bounce
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4	PORT_GOOD4# Input De-Bounce Control Controls de-bounce when PORT_GOOD4# is configured as an input (offset 600h[14], is Cleared). 0 = PORT_GOOD4# input is not de-bounced 1 = PORT_GOOD4# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
5	PORT_GOOD5# Input De-Bounce Control Controls de-bounce when PORT_GOOD5# is configured as an input (offset 600h[17], is Cleared). 0 = PORT_GOOD5# input is not de-bounced 1 = PORT_GOOD5# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
6	GPIO6 Input De-Bounce Control Controls de-bounce when GPIO6 is configured as an input (offset 600h[20], is Cleared). 0 = GPIO6 input is not de-bounced 1 = GPIO6 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
7	GPIO7 Input De-Bounce Control Controls de-bounce when GPIO7 is configured as an input (offset 600h[23], is Cleared). 0 = GPIO7 input is not de-bounced 1 = GPIO7 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
8	PORT_GOOD8# Input De-Bounce Control Controls de-bounce when PORT_GOOD8# is configured as an input (offset 600h[26], is Cleared). 0 = PORT_GOOD8# input is not de-bounced 1 = PORT_GOOD8# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
9	PORT_GOOD9# Input De-Bounce Control Controls de-bounce when PORT_GOOD9# is configured as an input (offset 600h[29], is Cleared). 0 = PORT_GOOD9# input is not de-bounced 1 = PORT_GOOD9# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
10	GPIO10 Input De-Bounce Control Controls de-bounce when GPIO10 is configured as an input (offset 604h[2], is Cleared). 0 = GPIO10 input is not de-bounced 1 = GPIO10 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
31:11	<i>Reserved</i>	RsvdP	No	0-0h

Register 11-125. 61Ch GPIO 0_10 Input Data (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], PORT_GOOD[8:9]#, and GPIO10 input values are updated into the GPIO 0_10 Input Data registers, respectively.</p> <p><i>Notes:</i> Register offsets 600h and 604h, referenced within this register, are located as follows – Port 0.</p> <p><i>PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h).</i></p> <p><i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i></p>				
0	PORT_GOOD0# Input Data If PORT_GOOD0# is configured as an output (offset 600h[2], is Set), Reads return a value of 0. If PORT_GOOD0# is configured as an input (offset 600h[2], is Cleared), Reads return the logic value of the voltage on PORT_GOOD0#.	ROS	No	0
1	GPIO1 Input Data If GPIO1 is configured as an output (offset 600h[5], is Set), Reads return a value of 0. If GPIO1 is configured as an input (offset 600h[5], is Cleared), Reads return the logic value of the voltage on GPIO1.	ROS	No	0
2	GPIO2 Input Data If GPIO2 is configured as an output (offset 600h[8], is Set), Reads return a value of 0. If GPIO2 is configured as an input (offset 600h[8], is Cleared), Reads return the logic value of the voltage on GPIO2.	ROS	No	0
3	GPIO3 Input Data If GPIO3 is configured as an output (offset 600h[11], is Set), Reads return a value of 0. If GPIO3 is configured as an input (offset 600h[11], is Cleared), Reads return the logic value of the voltage on GPIO3.	ROS	No	0

**Register 11-125. 61Ch GPIO 0_10 Input Data
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4	PORT_GOOD4# Input Data If PORT_GOOD4# is configured as an output (offset 600h[14], is Set), Reads return a value of 0. If PORT_GOOD4# is configured as an input (offset 600h[14], is Cleared), Reads return the logic value of the voltage on PORT_GOOD4#.	ROS	No	0
5	PORT_GOOD5# Input Data If PORT_GOOD5# is configured as an output (offset 600h[17], is Set), Reads return a value of 0. If PORT_GOOD5# is configured as an input (offset 600h[17], is Cleared), Reads return the logic value of the voltage on PORT_GOOD5#.	ROS	No	0
6	GPIO6 Input Data If GPIO6 is configured as an output (offset 600h[20], is Set), Reads return a value of 0. If GPIO6 is configured as an input (offset 600h[20], is Cleared), Reads return the logic value of the voltage on GPIO6.	ROS	No	0
7	GPIO7 Input Data If GPIO7 is configured as an output (offset 600h[23], is Set), Reads return a value of 0. If GPIO7 is configured as an input (offset 600h[23], is Cleared), Reads return the logic value of the voltage on GPIO7.	ROS	No	0
8	PORT_GOOD8# Input Data If PORT_GOOD8# is configured as an output (offset 600h[26], is Set), Reads return a value of 0. If PORT_GOOD8# is configured as an input (offset 600h[26], is Cleared), Reads return the logic value of the voltage on PORT_GOOD8#.	ROS	No	0
9	PORT_GOOD9# Input Data If PORT_GOOD9# is configured as an output (offset 600h[29], is Set), Reads return a value of 0. If PORT_GOOD9# is configured as an input (offset 600h[29], is Cleared), Reads return the logic value of the voltage on PORT_GOOD9#.	ROS	No	0
10	GPIO10 Input Data If GPIO10 is configured as an output (offset 604h[2], is Set), Reads return a value of 0. If GPIO10 is configured as an input (offset 604h[2], is Cleared), Reads return the logic value of the voltage on GPIO10.	ROS	No	0
31:11	Reserved	RsvdP	No	0-0h

Register 11-126. 624h GPIO 0_10 Output Data (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The GPIO 0_10 Output Data registers control the PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], PORT_GOOD[8:9]#, and GPIO10 outputs, respectively.</p> <p>Notes: Register offsets 600h and 604h, referenced within this register, are located as follows – Port 0.</p> <p>PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>				
0	PORT_GOOD0# Output Data If PORT_GOOD0# is configured as an output (offset 600h [2], is Set), the value written to this bit is immediately driven to the PORT_GOOD0# output. Reads return the value written.	RWS	Yes	0
1	GPIO1 Output Data If GPIO1 is configured as an output (offset 600h [5], is Set), the value written to this bit is immediately driven to the GPIO1 output. Reads return the value written.	RWS	Yes	0
2	GPIO2 Output Data If GPIO2 is configured as an output (offset 600h [8], is Set), the value written to this bit is immediately driven to the GPIO2 output. Reads return the value written.	RWS	Yes	0
3	GPIO3 Output Data If GPIO3 is configured as an output (offset 600h [11], is Set), the value written to this bit is immediately driven to the GPIO3 output. Reads return the value written.	RWS	Yes	0
4	PORT_GOOD4# Output Data If PORT_GOOD4# is configured as an output (offset 600h [14], is Set), the value written to this bit is immediately driven to the PORT_GOOD4# output. Reads return the value written.	RWS	Yes	0
5	PORT_GOOD5# Output Data If PORT_GOOD5# is configured as an output (offset 600h [17], is Set), the value written to this bit is immediately driven to the PORT_GOOD5# output. Reads return the value written.	RWS	Yes	0
6	GPIO6 Output Data If GPIO6 is configured as an output (offset 600h [20], is Set), the value written to this bit is immediately driven to the GPIO6 output. Reads return the value written.	RWS	Yes	0
7	GPIO7 Output Data If GPIO7 is configured as an output (offset 600h [23], is Set), the value written to this bit is immediately driven to the GPIO7 output. Reads return the value written.	RWS	Yes	0

**Register 11-126. 624h GPIO 0_10 Output Data
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
8	PORT_GOOD8# Output Data If PORT_GOOD8# is configured as an output (offset 600h[26], is Set), the value written to this bit is immediately driven to the PORT_GOOD8# output. Reads return the value written.	RWS	Yes	0
9	PORT_GOOD9# Output Data If PORT_GOOD9# is configured as an output (offset 600h[29], is Set), the value written to this bit is immediately driven to the PORT_GOOD9# output. Reads return the value written.	RWS	Yes	0
10	GPIO10 Output Data If GPIO10 is configured as an output (offset 604h[2], is Set), the value written to this bit is immediately driven to the GPIO10 output. Reads return the value written.	RWS	Yes	0
31:11	Reserved	RsvdP	No	0-0h

Register 11-127. 62Ch GPIO 0_10 Interrupt Polarity (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The GPIO 0_10 Interrupt Polarity registers control the PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], PORT_GOOD[8:9]#, and GPIO10 Interrupt input polarities, respectively.</p> <p>Notes: PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h).</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>				
0	PORT_GOOD0# Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PORT_GOOD0# Interrupt input is Active-Low 1 = PORT_GOOD0# Interrupt input is Active-High	RWS	Yes	0
1	GPIO1 Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO1 Interrupt input is Active-Low 1 = GPIO1 Interrupt input is Active-High	RWS	Yes	0
2	GPIO2 Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO2 Interrupt input is Active-Low 1 = GPIO2 Interrupt input is Active-High	RWS	Yes	0
3	GPIO3 Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO3 Interrupt input is Active-Low 1 = GPIO3 Interrupt input is Active-High	RWS	Yes	0
4	PORT_GOOD4# Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PORT_GOOD4# Interrupt input is Active-Low 1 = PORT_GOOD4# Interrupt input is Active-High	RWS	Yes	0
5	PORT_GOOD5# Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PORT_GOOD5# Interrupt input is Active-Low 1 = PORT_GOOD5# Interrupt input is Active-High	RWS	Yes	0
6	GPIO6 Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO6 Interrupt input is Active-Low 1 = GPIO6 Interrupt input is Active-High	RWS	Yes	0
7	GPIO7 Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO7 Interrupt input is Active-Low 1 = GPIO7 Interrupt input is Active-High	RWS	Yes	0

**Register 11-127. 62Ch GPIO 0_10 Interrupt Polarity
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
8	PORT_GOOD8# Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PORT_GOOD8# Interrupt input is Active-Low 1 = PORT_GOOD8# Interrupt input is Active-High	RWS	Yes	0
9	PORT_GOOD9# Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PORT_GOOD9# Interrupt input is Active-Low 1 = PORT_GOOD9# Interrupt input is Active-High	RWS	Yes	0
10	GPIO10 Interrupt Polarity Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO10 Interrupt input is Active-Low 1 = GPIO10 Interrupt input is Active-High	RWS	Yes	0
31:11	Reserved	RsvdP	No	0-0h

Register 11-128. 634h GPIO 0_10 Interrupt Status (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], PORT_GOOD[8:9]#, and GPIO10 Interrupt input status values are updated into the GPIO 0_10 Interrupt Status registers, respectively.</p> <p>Interrupt status remains Set, as long the corresponding PORT_GOODx# or GPIOx signal is asserted, and Clears on its own when the corresponding PORT_GOODx# or GPIOx input de-asserts to the inactive state.</p> <p>The active state of each interrupt is controlled by its respective GPIO 0_10 Interrupt Polarity register bits (Port 0. offset 62Ch).</p> <p>Notes: The bits in this register can be masked by their respective GPIO 0_10 Interrupt Mask register bits (Port 0. offset 63Ch).</p> <p>PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h).</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>				
0	PORT_GOOD0# Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = PORT_GOOD0# interrupt is inactive 1 = PORT_GOOD0# interrupt is active	ROS	No	0
1	GPIO1 Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = GPIO1 interrupt is inactive 1 = GPIO1 interrupt is active	ROS	No	0
2	GPIO2 Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = GPIO2 interrupt is inactive 1 = GPIO2 interrupt is active	ROS	No	0
3	GPIO3 Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = GPIO3 interrupt is inactive 1 = GPIO3 interrupt is active	ROS	No	0

**Register 11-128. 634h GPIO 0_10 Interrupt Status
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4	PORT_GOOD4# Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = PORT_GOOD4# interrupt is inactive 1 = PORT_GOOD4# interrupt is active	ROS	No	0
5	PORT_GOOD5# Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = PORT_GOOD5# interrupt is inactive 1 = PORT_GOOD5# interrupt is active	ROS	No	0
6	GPIO6 Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = GPIO6 interrupt is inactive 1 = GPIO6 interrupt is active	ROS	No	0
7	GPIO7 Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = GPIO7 interrupt is inactive 1 = GPIO7 interrupt is active	ROS	No	0
8	PORT_GOOD8# Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = PORT_GOOD8# interrupt is inactive 1 = PORT_GOOD8# interrupt is active	ROS	No	0
9	PORT_GOOD9# Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = PORT_GOOD9# interrupt is inactive 1 = PORT_GOOD9# interrupt is active	ROS	No	0
10	GPIO10 Interrupt Status Indicates whether the GPIO interrupt is inactive or active. 0 = GPIO10 interrupt is inactive 1 = GPIO10 interrupt is active	ROS	No	0
31:11	Reserved	RsvdP	No	0-0h

Register 11-129. 63Ch GPIO 0_10 Interrupt Mask (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>The PORT_GOOD0#, GPIO[1:3], PORT_GOOD[4:5]#, GPIO[6:7], PORT_GOOD[8:9]#, and GPIO10 Interrupt inputs are masked, using the GPIO 0_10 Interrupt Mask registers, respectively.</p> <p><i>Notes: The bits in this register can be used to mask their respective GPIO 0_10 Interrupt Status register bits (Port 0, offset 634h). PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h). Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i></p>				
0	PORT_GOOD0# Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = PORT_GOOD0# interrupt is not masked. 1 = PORT_GOOD0# interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
1	GPIO1 Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = GPIO1 interrupt is not masked. 1 = GPIO1 interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
2	GPIO2 Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = GPIO2 interrupt is not masked. 1 = GPIO2 interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
3	GPIO3 Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = GPIO3 interrupt is not masked. 1 = GPIO3 interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1

**Register 11-129. 63Ch GPIO 0_10 Interrupt Mask
(Port 0) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4	PORT_GOOD4# Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = PORT_GOOD4# interrupt is not masked. 1 = PORT_GOOD4# interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
5	PORT_GOOD5# Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = PORT_GOOD5# interrupt is not masked. 1 = PORT_GOOD5# interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
6	GPIO6 Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = GPIO6 interrupt is not masked. 1 = GPIO6 interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
7	GPIO7 Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = GPIO7 interrupt is not masked. 1 = GPIO7 interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
8	PORT_GOOD8# Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = PORT_GOOD8# interrupt is not masked. 1 = PORT_GOOD8# interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
9	PORT_GOOD9# Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = PORT_GOOD9# interrupt is not masked. 1 = PORT_GOOD9# interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
10	GPIO10 Interrupt Mask Indicates whether the GPIO interrupt is masked or not masked. 0 = GPIO10 interrupt is not masked. 1 = GPIO10 interrupt is masked. When an interrupt is masked, the corresponding Interrupt Status register bit is not updated.	RWS	Yes	1
31:11	Reserved	RsvdP	No	0-0h

11.16.10 Device-Specific Registers – PORT_GOOD Selector (Offsets 6A0h – 6A8h)

This section details the Device-Specific PORT_GOOD Selector registers. Table 11-26 defines the register map.

Table 11-26. Device-Specific PORT_GOOD Selector Register Map (Offsets 6A0h – 6A8h) (Port 0)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
PORT_GOOD Selector 0		6A0h
PORT_GOOD Selector 1		6A4h
PORT_GOOD Selector 2		6A8h

Register 11-130. 6A0h PORT_GOOD Selector 0 (Port 0)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register assigns PORT_GOOD_x#/GPIO_x signal(s) that are enabled for PORT_GOOD output functionality (in the GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and/or 604h), in which default values are globally defined, according to the STRAP_TESTMODE0 input state), to designated Port(s). This register has no effect on PORT_GOOD_x#/GPIO_x signals that are enabled for GPIO functionality.</p> <p>0_0000b = Port 0 0_1000b = Port 8 0_1001b = Port 9 1_0000b = Port 16 1_0001b = Port 17</p> <p>All other <i>Port Up Select x</i> field encodings are Reserved.</p> <p>Notes: PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOOD_x# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h.</p> <p><i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STN_x_PORTCFG0 input states and/or serial EEPROM programming.</p>				
4:0	Port Up Select 0 Use this field to program a different Port to be associated with PORT_GOOD0#. The default for PORT_GOOD0# is Port 0.	RWS	Yes	0_0000b
31:5	Factory Test Only	RsvdP	No	0-0h

**Register 11-131. 6A4h PORT_GOOD Selector 1
(Port 0)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register assigns PORT_GOOD_x/GPIO_x signal(s) that are enabled for PORT_GOOD output functionality (in the GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and/or 604h), in which default values are globally defined, according to the STRAP_TESTMODE0 input state), to designated Port(s). This register has no effect on PORT_GOOD_x/GPIO_x signals that are enabled for GPIO functionality.</p> <p>0_0000b = Port 0 0_1000b = Port 8 0_1001b = Port 9 1_0000b = Port 16 1_0001b = Port 17</p> <p>All other <i>Port Up Select x</i> field encodings are Reserved.</p> <p>Notes: PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOOD_x signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h.</p> <p><i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>				
4:0	Port Up Select 4 Use this field to program a different Port to be associated with PORT_GOOD4#. The default for PORT_GOOD4# is Port 8.	RWS	Yes	0_1000b
7:5	Reserved	RsvdP	No	000b
12:8	27 x 27 mm² Package Port Up Select 5 Use this field to program a different Port to be associated with PORT_GOOD5#. The default for PORT_GOOD5# is Port 9.	RWS	Yes	0_1010b
	19 x 21 mm² Package Reserved	RsvdP	No	0-0h
31:13	Factory Test Only/Reserved	RsvdP	No	0-0h

**Register 11-132. 6A8h PORT_GOOD Selector 2
(Port 0)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register assigns PORT_GOODx#/GPIOx signal(s) that are enabled for PORT_GOOD output functionality (in the GPIO 0_x Direction Control register <i>Direction Control</i> bit(s) (Port 0, offset(s) 600h and 604h), in which default values are globally defined, according to the STRAP_TESTMODE0 input state), to designated Port(s). This register has no effect on PORT_GOODx#/GPIOx signals that are enabled for GPIO functionality.</p> <p>0_0000b = Port 0 0_1000b = Port 8 0_1001b = Port 9 1_0000b = Port 16 1_0001b = Port 17</p> <p>All other <i>Port Up Select x</i> field encodings are Reserved.</p> <p>Notes: <i>PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively, by default. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h).</i></p> <p><i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</i></p>				
4:0	Port Up Select 8 Use this field to program a different Port to be associated with PORT_GOOD8#. The default for PORT_GOOD8# is Port 16.	RWS	Yes	1_0000b
7:5	Reserved	RsvdP	No	000b
12:8	27 x 27 mm² Package Port Up Select 9 Use this field to program a different Port to be associated with PORT_GOOD9#. The default for PORT_GOOD9# is Port 17.	RWS	Yes	1_0001b
	19 x 21 mm² Package Reserved	RsvdP	No	0-0h
31:13	Factory Test Only/Reserved	RsvdP	No	0-0h

11.16.11 Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)

This section details the Device-Specific Error Checking and Debug registers located at offsets 700h through 75Ch. [Table 11-27](#) defines the register map.

Other Device-Specific Error Checking and Debug registers are detailed in [Section 11.21.3](#), “Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h).”

Table 11-27. Device-Specific Error Checking and Debug Register Map (Offsets 700h – 75Ch) (Ports^a)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
Device-Specific Error Status 1																																700h
Device-Specific Error Mask 1																																704h
Device-Specific Error Status 2																																708h
Device-Specific Error Mask 2																																70Ch
<i>Reserved</i>								Device-Specific Error Status 3																								710h
<i>Reserved</i>								Device-Specific Error Mask 3																								714h
<i>Reserved</i>								Device-Specific Error Status 4																								718h
<i>Reserved</i>								Device-Specific Error Mask 4																								71Ch
ECC Error Check Disable																																720h
<i>Reserved</i>																Gen 3 Framing Error Status																724h
<i>Reserved</i>																Gen 3 Framing Error Mask																728h
<i>Reserved</i>																Gen 3 Framing Error Disable																72Ch
<i>Reserved</i>																																730h – 75Ch

a. Certain registers are Port-specific, others are Station-specific or Chip-specific; all are Device-specific.

**Register 11-133. 700h Device-Specific Error Status 1
(Ports 0, 8, and 16)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. <i>For example</i>, when Port 8 receives a packet, the data is stored in Station 1 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 1 RAM, the error is flagged in the Port 0 register bit that reflects Station 1 error status.</p> <p>Notes: The bits in this register can be masked by their respective <i>Device-Specific Error Mask 1</i> register bits (Port 0, 8, or 16, offset 704h).</p> <p>All errors in this register generate <i>ERR_FATAL</i> or <i>ERR_NONFATAL</i> Messages, if enabled by the following:</p> <ul style="list-style-type: none"> • <i>Device-Specific Error Mask 1</i> register • <i>Uncorrectable Error Status</i> register <i>Uncorrectable Internal Error Status</i> bit (Port 0, 8, or 16, offset FB8h[22], is Set) • Port's <i>Device Status</i> register <i>Fatal Error Reporting Enable</i> and <i>Non-Fatal Error Reporting Enable</i> bits (offset 70h[2:1], respectively) <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>					
0	Factory Test Only		RW1CS	Yes	0
1	Factory Test Only	0	RW1CS	No	0
2	Station 0 Egress Packet Link List RAM 1-Bit ECC Error Detected 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
3	Station 1 Egress Packet Link List RAM 1-Bit ECC Error Detected 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
4	Station 2 Egress Packet Link List RAM 1-Bit ECC Error Detected 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
7:5	Factory Test Only		RW1CS	Yes	000b
8	Station 0 Header RAM0 Instance 0 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
9	Station 1 Header RAM0 Instance 0 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
10	Station 2 Header RAM0 Instance 0 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
11	Station 0 Header RAM0 Instance 1 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0

**Register 11-133. 700h Device-Specific Error Status 1
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
12	Station 1 Header RAM0 Instance 1 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
13	Station 2 Header RAM0 Instance 1 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
14	Station 0 Header RAM1 Instance 0 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
15	Station 1 Header RAM1 Instance 0 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
16	Station 2 Header RAM1 Instance 0 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
17	Station 0 Header RAM1 Instance 1 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
18	Station 1 Header RAM1 Instance 1 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
19	Station 2 Header RAM1 Instance 1 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
22:20	Factory Test Only		RsvdP	No	000b
23	Destination Queue Link List RAM 1-Bit ECC Error Detected 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0

**Register 11-133. 700h Device-Specific Error Status 1
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
24	Source Queue Link List RAM 1-Bit ECC Error Detected 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
25	Retry Buffer 1-Bit ECC Error Detected 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
26	Ingress Link List RAM Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
27	Source Queue Link List RAM2 Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
28	Destination Queue Data RAM Soft Error Counter Overflow Detected 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
31:29	Reserved		RsvdP	No	000b

**Register 11-134. 704h Device-Specific Error Mask 1
(Ports 0, 8, and 16)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Notes: The bits in this register can be used to mask their respective <i>Device-Specific Error Status 1</i> register bits (Port 0, 8, or 16, offset 700h).</p> <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>					
0	Factory Test Only		RWS	Yes	1
1	Factory Test Only	0	RWS	Yes	1
2	Station 0 Egress Packet Link List RAM 1-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Egress Packet Link List RAM 1-Bit ECC Error Detected</i> bit is masked/disabled		RWS	Yes	1
3	Station 1 Egress Packet Link List RAM 1-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Egress Packet Link List RAM 1-Bit ECC Error Detected</i> bit is masked/disabled		RWS	Yes	1
4	Station 2 Egress Packet Link List RAM 1-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Egress Packet Link List RAM 1-Bit ECC Error Detected</i> bit is masked/disabled		RWS	Yes	1
7:5	Factory Test Only		RWS	Yes	000b
8	Station 0 Header RAM0 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM0 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
9	Station 1 Header RAM0 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM0 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
10	Station 2 Header RAM0 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM0 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
11	Station 0 Header RAM0 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM0 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1

Register 11-134. 704h Device-Specific Error Mask 1
(Ports 0, 8, and 16) (Cont.)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
12	Station 1 Header RAM0 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM0 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
13	Station 2 Header RAM0 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM0 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
14	Station 0 Header RAM1 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM1 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
15	Station 1 Header RAM1 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM1 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
16	Station 2 Header RAM1 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM1 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
17	Station 0 Header RAM1 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM1 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
18	Station 1 Header RAM1 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM1 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
19	Station 2 Header RAM1 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM1 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
22:20	Factory Test Only		RsvdP	No	000b
23	Destination Queue Link List RAM 1-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Destination Queue Link List RAM 1-Bit ECC Error Detected</i> bit is masked/disabled		RWS	Yes	1

**Register 11-134. 704h Device-Specific Error Mask 1
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
24	Source Queue Link List RAM 1-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Source Queue Link List RAM 1-Bit ECC Error Detected</i> bit is masked/disabled		RWS	Yes	1
25	Retry Buffer 1-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Retry Buffer 1-Bit ECC Error Detected</i> bit is masked/disabled		RWS	Yes	1
26	Ingress Link List RAM Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Ingress Link List RAM Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
27	Source Queue Link List RAM2 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Source Queue Link List RAM2 Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
28	Destination Queue Data RAM Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Destination Queue Data RAM Soft Error Counter Overflow Detected</i> bit is masked/disabled		RWS	Yes	1
31:29	Reserved		RsvdP	No	000b

**Register 11-135. 708h Device-Specific Error Status 2
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. <i>For example</i>, when Port 8 receives a packet, the data is stored in Station 1 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 1 RAM, the error is flagged in the Port 0 register bit that reflects Station 1 error status.</p> <p>Notes: The bits in this register can be masked by their respective <i>Device-Specific Error Mask 2</i> register bits (Port 0, 8, or 16, offset 70Ch).</p> <p>All errors in this register generate <i>ERR_FATAL</i> or <i>ERR_NONFATAL</i> Messages, if enabled by the following:</p> <ul style="list-style-type: none"> • <i>Device-Specific Error Mask 2</i> register • <i>Uncorrectable Error Status</i> register <i>Uncorrectable Internal Error Status</i> bit (Port 0, 8, or 16, offset FB8h[22], is Set) • Port's <i>Device Status</i> register <i>Fatal Error Reporting Enable</i> and <i>Non-Fatal Error Reporting Enable</i> bits (offset 70h[2:1], respectively) <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>				
0	Reserved	RsvdP	No	0
1	Ingress Freelist Underrun Error Detected 0 = No error is detected 1 = Underrun error is detected	RW1CS	Yes	0
2	Station 0 Egress Packet Link List RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
3	Station 1 Egress Packet Link List RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
4	Station 2 Egress Packet Link List RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
7:5	Factory Test Only	RW1CS	Yes	000b
8	Station 0 Header RAM0 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
9	Station 1 Header RAM0 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
10	Station 2 Header RAM0 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
11	Station 0 Header RAM0 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0

**Register 11-135. 708h Device-Specific Error Status 2
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12	Station 1 Header RAM0 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
13	Station 2 Header RAM0 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
14	Station 0 Header RAM1 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
15	Station 1 Header RAM1 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
16	Station 2 Header RAM1 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
17	Station 0 Header RAM1 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
18	Station 1 Header RAM1 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
19	Station 2 Header RAM1 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
22:20	Factory Test Only	RsvdP	No	000b
23	Destination Queue Link List RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0

**Register 11-135. 708h Device-Specific Error Status 2
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
24	Source Queue Link List RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
25	Retry Buffer 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
26	Ingress Link List RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
27	Source Queue Link List RAM2 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
28	Destination Queue Data RAM 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
29	Ingress Parity Error Detected 0 = No error is detected 1 = Ingress Parity error detected	RW1CS	Yes	0
30	Egress Parity Error Detected 0 = No error is detected 1 = Egress Parity error detected	RW1CS	Yes	0
31	Reserved	RsvdP	No	0

**Register 11-136. 70Ch Device-Specific Error Mask 2
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>Notes: The bits in this register can be used to mask their respective <i>Device-Specific Error Status 2</i> register bits (Port 0, 8, or 16, offset 708h).</p> <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>				
0	Reserved	RsvdP	No	0
1	Ingress Freelist Underrun Error Mask 0 = No effect on reporting activity 1 = <i>Ingress Freelist Underrun Error Detected</i> bit is masked/disabled	RWS	Yes	1
2	Station 0 Egress Packet Link List RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Egress Packet Link List RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
3	Station 1 Egress Packet Link List RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Egress Packet Link List RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
4	Station 2 Egress Packet Link List RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Egress Packet Link List RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
7:5	Factory Test Only	RWS	Yes	000b
8	Station 0 Header RAM0 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM0 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
9	Station 1 Header RAM0 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM0 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
10	Station 2 Header RAM0 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM0 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
11	Station 0 Header RAM0 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM0 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1

Register 11-136. 70Ch Device-Specific Error Mask 2
(Ports 0, 8, and 16) (Cont.)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12	Station 1 Header RAM0 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM0 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
13	Station 2 Header RAM0 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM0 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
14	Station 0 Header RAM1 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM1 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
15	Station 1 Header RAM1 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM1 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
16	Station 2 Header RAM1 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM1 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
17	Station 0 Header RAM1 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Header RAM1 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
18	Station 1 Header RAM1 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Header RAM1 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
19	Station 2 Header RAM1 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Header RAM1 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
22:20	Factory Test Only	RsvdP	No	000b
23	Destination Queue Link List RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Destination Queue Link List RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1

**Register 11-136. 70Ch Device-Specific Error Mask 2
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
24	Source Queue Link List RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Source Queue Link List RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
25	Retry Buffer 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Retry Buffer 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
26	Ingress Link List RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Ingress Link List RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
27	Source Queue Link List RAM2 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Source Queue Link List RAM2 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
28	Destination Queue Data RAM 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Destination Queue Data RAM 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
29	Ingress Parity Error Mask 0 = No effect on reporting activity 1 = <i>Ingress Parity Error Detected</i> bit is masked/disabled	RWS	Yes	1
30	Egress Parity Error Mask 0 = No effect on reporting activity 1 = <i>Egress Parity Error Detected</i> bit is masked/disabled	RWS	Yes	1
31	Reserved	RsvdP	No	0

**Register 11-137. 710h Device-Specific Error Status 3
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. <i>For example</i>, when Port 8 receives a packet, the data is stored in Station 1 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 1 RAM, the error is flagged in the Port 0 register bit that reflects Station 1 error status.</p> <p>Notes: The bits in this register can be masked by their respective <i>Device-Specific Error Mask 3</i> register bits (Port 0, 8, or 16, offset 714h).</p> <p>All errors in this register generate <i>ERR_FATAL</i> or <i>ERR_NONFATAL</i> Messages, if enabled by the following:</p> <ul style="list-style-type: none"> • <i>Device-Specific Error Mask 3</i> register • <i>Uncorrectable Error Status</i> register <i>Uncorrectable Internal Error Status</i> bit (Port 0, 8, or 16, offset FB8h[22], is Set) • Port's <i>Device Status</i> register <i>Fatal Error Reporting Enable</i> and <i>Non-Fatal Error Reporting Enable</i> bits (offset 70h[2:1], respectively) <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>				
0	Station 0 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
1	Station 1 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
2	Station 2 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
5:3	Factory Test Only	RW1CS	Yes	000b
6	Station 0 Packet RAM0 Instance 1 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
7	Station 1 Packet RAM0 Instance 1 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
8	Station 2 Packet RAM0 Instance 1 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
11:9	Factory Test Only	RW1CS	Yes	000b

**Register 11-137. 710h Device-Specific Error Status 3
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12	Station 0 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
13	Station 1 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
14	Station 2 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
17:15	Factory Test Only	RW1CS	Yes	000b
18	Station 0 Packet RAM1 Instance 1 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
19	Station 1 Packet RAM1 Instance 1 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
20	Station 2 Packet RAM1 Instance 1 Soft Error Counter Overflow Detected 0 = No error is detected 1 = Soft error is detected	RW1CS	Yes	0
23:21	Factory Test Only	RsvdP	No	000b
31:24	Reserved	RsvdP	No	00h

**Register 11-138. 714h Device-Specific Error Mask 3
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>Notes: The bits in this register can be used to mask their respective <i>Device-Specific Error Status 3</i> register bits (Port 0, 8, or 16, offset 710h).</p> <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>				
0	Station 0 Packet RAM0 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
1	Station 1 Packet RAM0 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
2	Station 2 Packet RAM0 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
5:3	Factory Test Only	RWS	Yes	000b
6	Station 0 Packet RAM0 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM0 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
7	Station 1 Packet RAM0 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM0 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
8	Station 2 Packet RAM0 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM0 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
11:9	Factory Test Only	RWS	Yes	000b

**Register 11-138. 714h Device-Specific Error Mask 3
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12	Station 0 Packet RAM1 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
13	Station 1 Packet RAM1 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
14	Station 2 Packet RAM1 Instance 0 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
17:15	Factory Test Only	RWS	Yes	000b
18	Station 0 Packet RAM1 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM1 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
19	Station 1 Packet RAM1 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM1 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
20	Station 2 Packet RAM1 Instance 1 Soft Error Counter Overflow Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM1 Instance 1 Soft Error Counter Overflow Detected</i> bit is masked/disabled	RWS	Yes	1
23:21	Factory Test Only	RsvdP	No	000b
31:24	Reserved	RsvdP	No	00h

**Register 11-139. 718h Device-Specific Error Status 4
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. <i>For example</i>, when Port 8 receives a packet, the data is stored in Station 1 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 1 RAM, the error is flagged in the Port 0 register bit that reflects Station 1 error status.</p> <p>Notes: The bits in this register can be masked by their respective <i>Device-Specific Error Mask 4</i> register bits (Port 0, 8, or 16, offset 71Ch).</p> <p>All errors in this register generate <i>ERR_FATAL</i> or <i>ERR_NONFATAL</i> Messages, if enabled by the following:</p> <ul style="list-style-type: none"> • <i>Device-Specific Error Mask 4</i> register • <i>Uncorrectable Error Status</i> register <i>Uncorrectable Internal Error Status</i> bit (Port 0, 8, or 16, offset FB8h[22], is Set) • Port's <i>Device Status</i> register <i>Fatal Error Reporting Enable</i> and <i>Non-Fatal Error Reporting Enable</i> bits (offset 70h[2:1], respectively) <p>The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.</p>				
0	Station 0 Packet RAM0 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
1	Station 1 Packet RAM0 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
2	Station 2 Packet RAM0 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
5:3	Factory Test Only	RW1CS	Yes	000b
6	Station 0 Packet RAM0 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
7	Station 1 Packet RAM0 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
8	Station 2 Packet RAM0 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
11:9	Factory Test Only	RW1CS	Yes	000b

**Register 11-139. 718h Device-Specific Error Status 4
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12	Station 0 Packet RAM1 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
13	Station 1 Packet RAM1 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
14	Station 2 Packet RAM1 Instance 0 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
17:15	Factory Test Only	RW1CS	Yes	000b
18	Station 0 Packet RAM1 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
19	Station 1 Packet RAM1 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
20	Station 2 Packet RAM1 Instance 1 2-Bit ECC Error Detected 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
23:21	Factory Test Only	RsvdP	No	000b
31:24	Reserved	RsvdP	No	00h

**Register 11-140. 71Ch Device-Specific Error Mask 4
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: The bits in this register can be used to mask their respective <i>Device-Specific Error Status 4</i> register bits (Port 0, 8, or 16, offset 718h). The Stations are defined in Table 11-5. The Port 0 bits are for Station 0. The Port 8 bits are for Station 1. The Port 16 bits are for Station 2.				
0	Station 0 Packet RAM0 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM0 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
1	Station 1 Packet RAM0 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM0 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
2	Station 2 Packet RAM0 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM0 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
5:3	Factory Test Only	RWS	Yes	000b
6	Station 0 Packet RAM0 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM0 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
7	Station 1 Packet RAM0 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM0 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
8	Station 2 Packet RAM0 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM0 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
11:9	Factory Test Only	RWS	Yes	000b

**Register 11-140. 71Ch Device-Specific Error Mask 4
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
12	Station 0 Packet RAM1 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM1 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
13	Station 1 Packet RAM1 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM1 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
14	Station 2 Packet RAM1 Instance 0 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM1 Instance 0 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
17:15	Factory Test Only	RWS	Yes	000b
18	Station 0 Packet RAM1 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 0 Packet RAM1 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
19	Station 1 Packet RAM1 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 1 Packet RAM1 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
20	Station 2 Packet RAM1 Instance 1 2-Bit ECC Error Mask 0 = No effect on reporting activity 1 = <i>Station 2 Packet RAM1 Instance 1 2-Bit ECC Error Detected</i> bit is masked/disabled	RWS	Yes	1
23:21	Factory Test Only	RsvdP	No	000b
31:24	Reserved	RsvdP	No	00h

**Register 11-141. 720h ECC Error Check Disable
(Ports 0, 8, and 16)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>					
0	ECC 1-Bit Error Check Disable 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	0	RWS	Yes	0
1	ECC 2-Bit Error Check Disable 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	0	RWS	Yes	0
2	Software Force Error Enable 1 = Correctable Error Status and Uncorrectable Error Status registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW. Software Sets an Uncorrectable Error Status register bit when that register is Cleared, the Advanced Error Capabilities and Control register <i>First Error Pointer</i> field (offset FCCh[4:0]) is updated; however, the Header Log x registers (offsets FD0h through FDCh) remain unchanged.	Upstream	RsvdP	No	0
		Downstream	RWS	Yes	0
3	Software Force Non-Posted Request Used to select software-forced errors to be associated with Posted or Non-Posted TLPs, because some errors are handled differently, depending upon the TLP type (Posted or Non-Posted). 0 = Handle software-forced errors as if the errors are associated with Posted TLPs 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs		RWS	Yes	0

**Register 11-141. 720h ECC Error Check Disable
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
4	Enable PEX_INTA# Interrupt Output for Link State Event-Triggered Interrupts 0 = Link State Event Interrupt Requests send an INT _x Message (and do not assert PEX_INTA#) 1 = Link State Event Interrupt Requests assert PEX_INTA# (and do not send an INT _x Message)		RWS	Yes	0
5	Reserved		RsvdP	No	0
6	Enable PEX_INTA# Interrupt Output for GPIO-Generated Interrupts 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT _x Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT _x Message)		RWS	Yes	0
9:7	Reserved		RsvdP	No	000b
10	Disable Sending MSI if MSI Is Enabled after Interrupt Status Set 0 = Does not disable sending an MSI, if MSIs are enabled after an <i>Interrupt Status</i> bit is Set 1 = Disables sending an MSI, if MSIs are enabled after an <i>Interrupt Status</i> bit is Set <i>Note: This bit must remain Cleared, for compliance to specifications governing the MSI Capability.</i>		RWS	Yes	0
11	Egress Completion FIFO Overflow Mask <i>Note: This bit can be used to mask bit 12 (Egress Completion FIFO Overflow Status).</i>		RWS	Yes	1
12	Egress Completion FIFO Overflow Status <i>Note: This bit can be masked by bit 11 (Egress Completion FIFO Overflow Mask).</i>		RW1CS	Yes	0
31:13	Reserved		RsvdP	No	0-0h

**Register 11-142. 724h Gen 3 Framing Error Status
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<i>Note:</i> The bits in this register can be masked by their respective Gen 3 Framing Error Mask register bits (offset 728h).				
0	Invalid Sync Header Status	RW1CS	Yes	0
1	Sync Header Not Same on All Lanes Status	RW1CS	Yes	0
2	Bad Framing Symbol in Data Block Status	RW1CS	Yes	0
3	Second Symbol of DLLP Not ACh Status 1 = Second symbol of the Data Link Layer Packet (DLLP) is not ACh	RW1CS	Yes	0
4	EDB Not following TLP Status	RW1CS	Yes	0
5	Length CRC/Parity Error Status Length Cyclic Redundancy Check (CRC)/Parity Error status.	RW1CS	Yes	0
6	End of Data Stream Not Followed by Ordered-Set Block Status	RW1CS	Yes	0
7	End of Data Stream Not in Last DWord of Data Block Status	RW1CS	Yes	0
8	Ordered-Set Block Not Followed by Data Block Status	RW1CS	Yes	0
9	FTS Not Followed by Data Block Status	RW1CS	Yes	0
10	Invalid Skip Ordered-Set Status	RW1CS	Yes	0
11	Ordered-Set Not the Same on All Lanes Status	RW1CS	Yes	0
12	Not All Subsequent Lanes Have LIDL or End of Data Stream when LIDL Status	RW1CS	Yes	0
13	Last TLP or DLLP Has No LIDL Symbols Status For x8 or x16 Gen 3 Links, if a TLP or DLLP ends on Lane K, and is not followed by another TLP or DLLP, then subsequent Lanes should have LIDL symbols.	RW1CS	Yes	0
14	Frame Error 14 Status	RW1CS	Yes	0
15	Frame Error 15 Status	RW1CS	Yes	0
31:16	Reserved	RsvdP	No	0000h

**Register 11-143. 728h Gen 3 Framing Error Mask
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<i>Note:</i> The bits in this register can be used to mask their respective Gen 3 Framing Error Status register bits (offset 724h).				
0	Invalid Sync Header Mask	RWS	Yes	0
1	Sync Header Not Same on All Lanes Mask	RWS	Yes	0
2	Bad Framing Symbol in Data Block Mask	RWS	Yes	0
3	Second Symbol of DLLP Not ACh Mask	RWS	Yes	0
4	EDB Not following TLP Mask	RWS	Yes	0
5	Length CRC/Parity Error Mask Length Cyclic Redundancy Check (CRC)/Parity Error mask.	RWS	Yes	0
6	End of Data Stream Not Followed by Ordered-Set Block Mask	RWS	Yes	0
7	End of Data Stream Not in Last DWord of Data Block Mask	RWS	Yes	0
8	Ordered-Set Block Not Followed by Data Block Mask	RWS	Yes	0
9	FTS Not Followed by Data Block Mask	RWS	Yes	0
10	Invalid Skip Ordered-Set Mask	RWS	Yes	0
11	Ordered-Set Not the Same on All Lanes Mask	RWS	Yes	0
12	Not All Subsequent Lanes Have LIDL or End of Data Stream when LIDL Mask	RWS	Yes	0
13	Last TLP or DLLP Has No LIDL Symbols Mask For x8 or x16 Gen 3 Links, if TLP or DLLP ends on Lane K, and not followed by another TLP or DLLP, then subsequent Lanes should have LIDL symbols.	RWS	Yes	0
14	Frame Error 14 Mask	RWS	Yes	0
15	Frame Error 15 Mask	RWS	Yes	0
31:16	Reserved	RsvdP	No	0000h

**Register 11-144. 72Ch Gen 3 Framing Error Disable
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
0	Sync Header Not Same on All Lanes Disable	RWS	Yes	0
1	Invalid Block Type Disable	RWS	Yes	0
2	Not SKIP, EIOS, or EIEOS Ordered-Set in Block following EDS Disable	RWS	Yes	0
3	Any Ordered-Set Block following SDS Ordered-Set Disable	RWS	Yes	0
4	Ordered-Set Block Received Without EDS Token in Preceding Data Block Disable	RWS	Yes	0
5	Block Containing EDS Token Followed by Data Block Instead of Ordered-Set Disable	RWS	Yes	0
6	Ordered-Sets Not the Same on All Lanes Disable	RWS	Yes	1
7	TLP Length Field CRC/Parity Disable	RWS	Yes	0
8	All Four Symbols of EDB Token Not the Same Disable	RWS	Yes	0
9	EDB Token Not Immediately following a TLP Disable	RWS	Yes	0
10	TLP Length Field = 0 Disable	RWS	Yes	1
11	Received More than One STP Token in a Single Symbol Time Disable	RWS	Yes	1
12	Received More than One SDP Token in a Single Symbol Time Disable	RWS	Yes	1
13	Lanes between IDL and Next Potential Starting Lane are Not All IDL Disable	RWS	Yes	1
14	Invalid Framing Token Detected when Searching for Framing Tokens Disable	RWS	Yes	0
15	Frame Error 15 Disable	RWS	Yes	1
31:16	Reserved	RsvdP	No	0000h

11.16.12 **Device-Specific Registers – Control
(Offsets 760h – 774h)**

This section details the Device-Specific Control registers. [Table 11-28](#) defines the register map.

**Table 11-28. Device-Specific Control Register Map
(Ports 0, 8, and 16)**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Station-Based Control		760h
Ingress Chip Control		764h
Factory Test Only		768h – 774h

**Register 11-145. 760h Station-Based Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
0	Link List RAM 1-Bit Error Injection The ECC Counter for this bit is located in the Ingress PLL RAM ECC 1-Bit Counter register <i>1-Bit ECC Counter for PLL RAM Read from Ingress Block</i> field (Port 0, 8, or 16, offset 778h[7:0]).	RWS	Yes	0
1	Link List RAM 2-Bit Error Injection	RWS	Yes	0
2	Link List RAM Error Injection Field 0 = Error injection is in the <i>ECC Code</i> field 1 = Error injection is in the <i>Data</i> field	RWS	Yes	0
4:3	Link List RAM Port Selector for Error Injection	RWS	Yes	00b
5	Accumulator x12 Pointer Reset Disable 0 = Enables 1 = Disables	RWS	Yes	0
6	<i>Not used</i>	RWS	Yes	0
7	RAM Select for ECC Injection 0 = Select Payload RAM for ECC injection 0 = Select Header RAM for ECC injection	RWS	Yes	0
8	Header RAM 1-Bit Error Injection	RWS	Yes	0
9	Header RAM 2-Bit Error Injection	RWS	Yes	0
10	Header RAM Error Injection Field 0 = Error injection is in the <i>ECC Code</i> field 1 = Error injection is in the <i>Data</i> field	RWS	Yes	0
12:11	Header RAM Port Selector for Error Injection	RWS	Yes	00b
15:13	<i>Factory Test Only</i>	RWS	Yes	000b

**Register 11-145. 760h Station-Based Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
	Silicon Revision BA Payload RAM 1-Bit Error Injection	RWS	Yes	0
16	Silicon Revision CA Device-Specific Register Access by Extended Configuration Request Enable <i>Note: Although this bit exists within each Station; however, it is used only in the Station that has the Upstream Port.</i> This bit controls whether Extended Configuration Requests can access Device-Specific registers within the following Address ranges, of each Port: <ul style="list-style-type: none"> • 200h through AFCh • B0Ch through B6Ch • B80h through C30h Because this bit exists within the Device-Specific register range listed above, it cannot be Set by an Extended Configuration Request. Serial EEPROM, I ² C/SMBus, and Memory-Mapped access can initially Set this bit. 0 = Extended Configuration Requests cannot access Device-Specific registers (default) 1 = Extended Configuration Requests can access Device-Specific registers	RWS	Yes	0
20	Source Queue Link List RAM 1-Bit Error Injection	RWS	Yes	0
21	Source Queue Link List RAM 2-Bit Error Injection	RWS	Yes	0
22	Source Queue Link List RAM Error Injection Field 0 = Error injection is in the <i>ECC Code</i> field 1 = Error injection is in the <i>Data</i> field	RWS	Yes	0
23	Source Queue Link List RAM Selector for Error Injection 0 = Port-A, normal traffic 1 = Port-B, Read-Pacing traffic	RWS	Yes	0

**Register 11-145. 760h Station-Based Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
24	Disable Credit Re-Balancing 1 = No Credit re-balancing	RWS	Yes	0
25	Use Serial EEPROM Values for Ingress Credit Initialization Allow Configuration with a Device Number that is not 0, that is accessing Downstream devices, to be forwarded. When the Device Number is 0, the Configuration terminates in a UR. 0 = Use default values for ingress credit initialization 1 = Use serial EEPROM values for ingress credit initialization	RWS	Yes	0
26	INCH Credit Reserve Flag A transition from 0 to 1 indicates that I ² C has finished with all CSR to INCH Initialization registers, and credit reservation can proceed.	RWS	Yes	0
28:27	Factory Test Only	RWS	Yes	00b
29	No Special Treatment for Relaxed Ordering Traffic The PEX 8747 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit, in each Station. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to the egress block <i>Note: When Set, affects all Ports within the Station.</i>	RWS	Yes	0
30	Factory Test Only	RWS	Yes	0
31	Not used	RWS	Yes	0

**Register 11-146. 764h Ingress Chip Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
2:0	Reserved	RsvdP	No	000b
16:3	Factory Test Only	RWS	Yes	0-0h
18:17	Reserved	RsvdP	No	00b
19	Not used	RWS	Yes	0
20	Ingress MWr32 Counter Disable 0 = Enables Ingress Memory Write 32-Bit Counter 1 = Disables Ingress Memory Write 32-Bit Counter	RWS	Yes	0
21	Ingress MWr64 Counter Disable 0 = Enables Ingress Memory Write 64-Bit Counter 1 = Disables Ingress Memory Write 64-Bit Counter	RWS	Yes	0
22	Ingress MSG Counter Disable 0 = Enables Ingress Message Counter 1 = Disables Ingress Message Counter	RWS	Yes	0
23	Ingress MRd32 Counter Disable 0 = Enables Ingress Memory Read 32-Bit Counter 1 = Disables Ingress Memory Read 32-Bit Counter	RWS	Yes	0
24	Ingress MRd64 Counter Disable 0 = Enables Ingress Memory Read 64-Bit Counter 1 = Disables Ingress Memory Read 64-Bit Counter	RWS	Yes	0
25	Ingress Other Non-Posted Counter Disable 0 = Enables Ingress Other Non-Posted Counter 1 = Disables Ingress Other Non-Posted Counter	RWS	Yes	0
26	Ingress and Egress DLLP ACK Counter Disable 0 = Enables Ingress and Egress DLLP ACK Counter 1 = Disables Ingress and Egress DLLP ACK Counter	RWS	Yes	0
27	Ingress and Egress DLLP UpdateFC-P Counter Disable 0 = Enables Ingress and Egress DLLP UpdateFC-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Posted Counter	RWS	Yes	0
28	Ingress and Egress DLLP UpdateFC-NP Counter Disable 0 = Enables Ingress and Egress DLLP UpdateFC-Non-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Non-Posted Counter	RWS	Yes	0
29	Ingress and Egress DLLP UpdateFC-CPL Counter Disable 0 = Enables Ingress and Egress DLLP UpdateFC-Completion Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Completion Counter	RWS	Yes	0
30	Parity Error Inject on Sch Bus	RWS	Yes	0
31	Factory Test Only	RO	Yes	0

11.16.13 Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)

This section details the Device-Specific Soft Error registers. [Table 11-29](#) defines the register map.

**Table 11-29. Device-Specific Soft Error Register Map
(Ports 0, 8, and 16)**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
<i>Reserved</i>																Ingress PLL RAM ECC 1-Bit Counter																778h
Accumulator Debug NAK																																77Ch
Ingress Exerciser Completion Status																																780h
Ingress Exerciser Completion Data																																784h
<i>Reserved</i>																																788h – 7FCh
Egress Station 0 Payload RAM Soft Error Counters																																800h
Egress Station 1 Payload RAM Soft Error Counters																																804h
Egress Station 2 Payload RAM Soft Error Counters																																808h
<i>Factory Test Only</i>																																80Ch
<i>Reserved</i>				Egress Header RAM Soft Error Counters 1																												810h
<i>Reserved</i>				Egress Header RAM Soft Error Counters 2																												814h
<i>Reserved</i>				Egress Header RAM Soft Error Counters 3																												818h
<i>Reserved</i>				Egress Header RAM Soft Error Counters 4																												81Ch
<i>Reserved</i>				Egress PLL RAM Soft Error Counters 1																												820h
Egress PLL RAM Soft Error Counters 2																<i>Reserved</i>																824h
Egress Miscellaneous RAM Soft Error Counters																																828h
Soft Error Injection																																82Ch
<i>Reserved</i>																																830h – 8FCh

**Register 11-147. 778h Ingress PLL RAM ECC 1-Bit Counter
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	1-Bit ECC Counter for PLL RAM Read from Ingress Block A Write of 0 to bit 0 Clears the ECC Counter.	ROS	No	00h
31:8	<i>Reserved</i>	RsvdP	No	0000_00h

**Register 11-148. 77Ch Accumulator Debug NAK
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
Accumulator Debug NAK		RWS	Yes	0-0h
Bit(s)	Description/Function			
0	Initiate NAK Substitution for ACK			
18:0	Port Number for NAK Substitution 000b = Port 0 of the Station 001b = Port 1 of the Station (Stations 1 and 2 Only) All other encodings are <i>Reserved</i> . <i>Note: If Port 1 of the Station is not enabled, 001b is Reserved.</i>			
15:4	Sequence Number for NAK Substitution			
18:16	Number of NAK Substitutions to Perform	RWS	No	0-0h
31:19	<i>Not used</i>			

**Register 11-149. 780h Ingress Exerciser Completion Status
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
0	Received a Completion 1 = New Completion received	RW1C	Yes	0
1	Completion Received with EP	ROS	No	0
2	Completion Received with ECRC Error	ROS	No	0
3	Reserved	RsvdP	No	0
6:4	Completion Status 1 = Received Completion TLPs status	ROS	No	000b
31:7	Reserved	RsvdP	No	0-0h

**Register 11-150. 784h Ingress Exerciser Completion Data
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
31:0	Completion Data 1 = Received Completion data	ROS	No	0000_0000h

Register 11-151. 800h Egress Station 0 Payload RAM Soft Error Counters (Ports 0, 8, and 16)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Station 0 Payload RAM Bus 0 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 0 Payload RAM Bus 0 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 0 Payload RAM Bus 1 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	Station 0 Payload RAM Bus 1 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h

Register 11-152. 804h Egress Station 1 Payload RAM Soft Error Counters (Ports 0, 8, and 16)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Station 1 Payload RAM Bus 0 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 1 Payload RAM Bus 0 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 1 Payload RAM Bus 1 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	Station 1 Payload RAM Bus 1 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h

Register 11-153. 808h Egress Station 2 Payload RAM Soft Error Counters (Ports 0, 8, and 16)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Station 2 Payload RAM Bus 0 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 2 Payload RAM Bus 0 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 2 Payload RAM Bus 1 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	Station 2 Payload RAM Bus 1 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h

**Register 11-154. 810h Egress Header RAM Soft Error Counters 1
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Station 0 Header RAM Bus 0 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 1 Header RAM Bus 0 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 2 Header RAM Bus 0 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	<i>Reserved</i>	RsvdP	No	00h

**Register 11-155. 814h Egress Header RAM Soft Error Counters 2
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Station 0 Header RAM Bus 0 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 1 Header RAM Bus 0 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 2 Header RAM Bus 0 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	<i>Reserved</i>	RsvdP	No	00h

**Register 11-156. 818h Egress Header RAM Soft Error Counters 3
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
7:0	Station 0 Header RAM Bus 1 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 1 Header RAM Bus 1 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 2 Header RAM Bus 1 Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	<i>Reserved</i>	RsvdP	No	00h

**Register 11-157. 81Ch Egress Header RAM Soft Error Counters 4
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
7:0	Station 0 Header RAM Bus 1 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 1 Header RAM Bus 1 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 2 Header RAM Bus 1 Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	<i>Reserved</i>	RsvdP	No	00h

**Register 11-158. 820h Egress PLL RAM Soft Error Counters 1
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Station 0 PLL RAM 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Station 1 PLL RAM 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Station 2 PLL RAM 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	Reserved	RsvdP	No	00h

**Register 11-159. 824h Egress PLL RAM Soft Error Counters 2
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Source Queue Link List RAM Instance 1 1-Bit Soft Error Counter Value Reserved	RsvdP	No	00h
15:8	Reserved	RsvdP	No	00h
23:16	Destination Queue Link List RAM Instance 1 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	Destination Queue Link List RAM Instance 2 1-Bit Soft Error Counter Value	ROS	No	00h

**Register 11-160. 828h Egress Miscellaneous RAM Soft Error Counters
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
7:0	Destination Queue Data RAM 1-Bit Soft Error Counter Value	ROS	No	00h
15:8	Destination Queue Link List RAM Instance 0 1-Bit Soft Error Counter Value	ROS	No	00h
23:16	Source Queue Link List RAM 1-Bit Soft Error Counter Value	ROS	No	00h
31:24	Retry Buffer 1-Bit Soft Error Counter Value	ROS	No	00h

**Register 11-161. 82Ch Soft Error Injection
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
0	Destination Queue Data RAM 1-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
1	Destination Queue Data RAM 2-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
2	Destination Queue Data RAM Error Injection Select 0 = Inject Soft error in the <i>ECC Code</i> field 1 = Inject Soft error in the <i>Data</i> field	RWS	Yes	0
3	Destination Queue Link List RAM Instance 0 1-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
4	Destination Queue Link List RAM Instance 0 2-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
5	Destination Queue Link List RAM Instance 0 Error Injection Select 0 = Inject Soft error in the <i>ECC Code</i> field 1 = Inject Soft error in the <i>Data</i> field	RWS	Yes	0
6	Retry Buffer 1-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
7	Retry Buffer 2-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0

Register 11-161. 82Ch Soft Error Injection
(Ports 0, 8, and 16) (Cont.)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
8	Retry Buffer Error Injection Select 0 = Inject Soft error in the <i>ECC Code</i> field 1 = Inject Soft error in the <i>Data</i> field	RWS	Yes	0
9	Destination Queue Link List RAM Instance 1 1-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
10	Destination Queue Link List RAM Instance 1 2-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
11	Destination Queue Link List RAM Instance 1 Error Injection Select 0 = Inject Soft error in the <i>ECC Code</i> field 1 = Inject Soft error in the <i>Data</i> field	RWS	Yes	0
12	Destination Queue Link List RAM Instance 2 1-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
13	Destination Queue Link List RAM Instance 2 2-Bit Soft Error Injection Writing 1 injects one error.	RWS	Yes	0
14	Destination Queue Link List RAM Instance 2 Error Injection Select 0 = Inject Soft error in the <i>ECC Code</i> field 1 = Inject Soft error in the <i>Data</i> field	RWS	Yes	0
19:15	Reserved	RsvdP	No	0-0h

Register 11-161. 82Ch Soft Error Injection
(Ports 0, 8, and 16) (Cont.)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
20	Ingress Payload RAM0 Instance 0 ECC Counter Reset Writing 1 Clears the Counter in the Egress Station x Payload RAM Soft Error Counters register <i>Station x Payload RAM0 Instance 0 1-Bit Soft Error Counter Value</i> field(s) (Port 0, 8, or 16, offsets 800h , 804h , and 808h [7:0]). Reads always return a value of 0.	RZ	Yes	0
21	Ingress Payload RAM0 Instance 1 ECC Counter Reset Writing 1 Clears the Counter in the Egress Station x Payload RAM Soft Error Counters register <i>Station x Payload RAM0 Instance 1 1-Bit Soft Error Counter Value</i> field(s) (Port 0, 8, or 16, offsets 800h , 804h , and 808h [15:8]). Reads always return a value of 0.	RZ	Yes	0
22	Ingress Payload RAM1 Instance 0 ECC Counter Reset Writing 1 Clears the Counter in the Egress Station x Payload RAM Soft Error Counters register <i>Station x Payload RAM1 Instance 0 1-Bit Soft Error Counter Value</i> field(s) (Port 0, 8, or 16, offsets 800h , 804h , and 808h [23:16]). Reads always return a value of 0.	RZ	Yes	0
23	Ingress Payload RAM1 Instance 1 ECC Counter Reset Writing 1 Clears the Counter in the Egress Station x Payload RAM Soft Error Counters register <i>Station x Payload RAM1 Instance 1 1-Bit Soft Error Counter Value</i> field(s) (Port 0, 8, or 16, offsets 800h , 804h , and 808h [31:24]). Reads always return a value of 0.	RZ	Yes	0
24	Header RAM ECC Counter Reset Writing 1 Clears the Counter in the Egress Header RAM Soft Error Counters x register <i>Station x Header RAM 1-Bit Soft Error Counter Value</i> field(s) (Port 0, 8, or 16, offset 810h [7:0, 15:8, and 23:16], respectively). Reads always return a value of 0.	RZ	Yes	0
28:25	Factory Test Only	RZ	Yes	0h
31:29	Station Number to Reset the ECC Counter Selects the ECC Counter that corresponds to the Station Number. 000b = Station 0 (default) 001b = Station 1 010b = Station 2 All other encodings are Reserved .	RZ	Yes	000b

11.16.14 Device-Specific Registers – Ingress Credit Handler (Offsets 9ECh – A2Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) registers. Table 11-30 defines the register map.

Table 11-30. Device-Specific INCH Register Map (Ports^a)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Reserved																																9ECh	
INCH Station Pool Values																																9F0h	
Factory Test Only																																9F4h	
INCH Reserve Pool																																9F8h	
Reserved																								INCH Port Pool								9FCh	
INCH Threshold VC0 Posted																																A00h	
Factory Test Only								INCH Threshold VC0 Non-Posted																								A04h	
INCH Threshold VC0 Completion																																A08h	
Reserved																																A0Ch –	A2Ch

a. Certain registers are Port-specific, others are Station-specific; all are Device-specific.

**Register 11-162. 9F0h INCH Station Pool Values
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
INCH Reserve pool.				
<i>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i>				
<i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
8:0	Current Value of Header Pool for the Station	ROS	Yes	–
15:9	Reserved	RsvdP	No	0-0h
25:16	Current Value of Payload Link Pool for the Station	ROS	Yes	–
31:26	Reserved	RsvdP	No	0-0h

**Register 11-163. 9F8h INCH Reserve Pool
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<i>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i>				
<i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
7:0	Header Count to Remove from Station Header Pool Value of Header to remove from initial Header pool.	RW	Yes	00h
15:8	Reserved	RsvdP	No	00h
24:16	Payload Link Count to Remove from Station Payload Pool Value of Payload Links to remove from initial Payload Link pool.	RW	Yes	0-0h
31:25	Reserved	RsvdP	No	0-0h

**Register 11-164. 9FCh INCH Port Pool
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<i>Note: Consider the INCH Port Pool register to be Reserved and only change the credit Settings, using the INCH Threshold registers (offsets A00h through A08h). Do not change the INCH Port Pool register from its default value, unless directed otherwise by PLX Technical Support.</i>				
2:0	Port Payload Pool Payload credits (other than the initial credits) for Posted/Completion TLPs that are dedicated to the Port. 000b = 0 001b = 32 010b = 64 011b = 96 100b = 128 101b = 192 110b, 111b = 256	RWS	Yes	000b
3	Unused 0 Keep value at 0. Additional bit for the Port Payload Pool.	RWS	Yes	0
6:4	Port Header Pool Combined Header credits (other than the initial credits) that are dedicated to the Port. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
7	Unused 1 Keep value at 0. Additional bit for the Port Header Pool.	RWS	Yes	0
31:8	Reserved	RsvdP	No	0000_00h

Register 11-165. A00h INCH Threshold VC0 Posted (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Posted credits are used for VC0 Memory Write and Message transactions. <i>Note: Changing credit values from default register values must be done carefully; otherwise the PEX 8747 will not properly function.</i>				
2:0	<i>Reserved</i>	RsvdP	No	Upstream Payload (decimal): x16: 504 x8: 256 x4: 136 x2: 72
8:3	Posted Payload Credit Default advertised Posted Payload credit. Actual value is dependent upon Link width and Port configuration, and the advertised value can be 0 to 3 more Payload credits than the register value. Bit resolution is in units of 8. Each increment provides 8 Posted Payload credits (<i>for example</i> , Ah = 80 Posted Payload credits). Each credit means that 16 bytes of storage are reserved for Posted TLP Payload data.	RWS	Yes	Downstream Payload (decimal): x16: 504 x8: 256 x4: 136 x2: 72 Upstream: x16: C3F8h x8: 63000h x4: 3288h x2: 1A48h
15:9	Posted Header Credit Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Posted Header credit (<i>for example</i> , Ah = 10 Posted Header credits). Each credit means that storage is reserved for the entire Header of a Posted TLP.	RWS	Yes	Upstream Header (decimal): x16: 97 x8: 49 x4: 25 x2: 13 Downstream Header (decimal): x16: 124 x8: 113 x4: 57 x2: 29 Downstream: x16: F9F8h x8: E300h x4: 7288h x2: 3A48h

**Register 11-165. A00h INCH Threshold VC0 Posted
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
17:16	UpdateFC High-Priority Threshold for Posted Payload Credit 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	UpdateFC High-Priority Threshold for Posted Header Credit 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	Congested Port Weight If the effective rate Setting times the negotiated Port Link width equates to less than x1 or greater than x8, the internal Credit Allocation logic rounds to x1 or x8, respectively. 000b = Request is weighted, based upon the Port's Link width relative to the effective Link widths of the other Stations' Port(s) 001b = Increases the weight of a Request by 2x 010b = Increases the weight of a Request by 4x 011b = Increases the weight of a Request by 8x 100b = Port receives no credit out of the common pool, until a decongested state is reached 101b = Decreases the weight of a Request by 2x 110b = Decreases the weight of a Request by 4x 111b = Decreases the weight of a Request by 8x	RWS	Yes	000b
31:23	Reserved	RsvdP	No	0-0h

Register 11-166. A04h INCH Threshold VC0 Non-Posted (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Non-Posted credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions. <i>Note: Changing credit values from default register values must be done carefully; otherwise the PEX 8747 will not properly function.</i>				
7:0	Non-Posted Payload Credit The Non-Posted Payload is stored with the Non-Posted Header; therefore Non-Posted Payload credit is always available.	RWS	Yes	Upstream Payload (decimal): x16: 8 x8: 8 x4: 8 x2: 8 Downstream Payload (decimal): x16: 8 x8: 8 x4: 8 x2: 8
8	<i>Reserved</i>	RsvdP	No	0
15:9	Non-Posted Header Credit Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Non-Posted Header credit (<i>for example</i> , Ah = 10 Non-Posted Header credits). Each credit means that storage is reserved for the entire Header of a Non-Posted TLP.	RWS	Yes	Upstream Header (decimal): x16: 97 x8: 49 x4: 25 x2: 13 Downstream Header (decimal): x16: 124 x8: 62 x4: 31 x2: 15

**Register 11-166. A04h INCH Threshold VC0 Non-Posted
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
17:16	UpdateFC High-Priority Threshold for Non-Posted Payload Credit 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	UpdateFC High-Priority Threshold for Non-Posted Header Credit 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	<i>Not used</i>	RWS	Yes	000b
23	<i>Reserved</i>	RsvdP	No	0
29:24	<i>Factory Test Only</i>	RWS	Yes	0-0h
31:30	<i>Factory Test Only</i>	RW1C	No	00b

**Register 11-167. A08h INCH Threshold VC0 Completion
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Completion credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions. <i>Note: Changing credit values from default register values must be done carefully; otherwise the PEX 8747 will not properly function.</i>				
2:0	<i>Reserved</i>	RsvdP	No	Upstream Payload (decimal): x16: 480 x8: 240 x4: 136 x2: 72
8:3	Completion Payload Credit Default advertised Completion Payload credit. Actual value is dependent upon Link width and Port configuration, and the advertised value can be 0 to 3 more Payload credits than the register value. Bit resolution is in units of 8. Each increment provides 8 Completion Payload credits (<i>for example</i> , Ah = 80 Completion Payload credits). Each credit means that 16 bytes of storage are reserved for Completion TLP Payload data.	RWS	Yes	Downstream Payload (decimal): x16: 480 x8: 240 x4: 136 x2: 72 Upstream: x16: F9E0h x8: E2F0h x4: 7288h x2: 3A48h
15:9	Completion Header Credit Default advertised Completion Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Completion Header credit (<i>for example</i> , Ah = 10 Completion Header credits). Each credit means that storage is reserved for the entire Header of a Completion TLP.	RWS	Yes	Upstream Header (decimal): x16: 124 x8: 71 x4: 57 x2: 29 Downstream Header (decimal): x16: 70 x8: 36 x4: 19 x2: 11 Downstream: x16: 8DE0h x8: 48F0h x4: 2688h x2: 1648h

**Register 11-167. A08h INCH Threshold VC0 Completion
(All Ports) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
17:16	UpdateFC High-Priority Threshold for Completion Payload Credit 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
19:18	UpdateFC High-Priority Threshold for Completion Header Credit 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b
22:20	<i>Not used</i>	RWS	Yes	000b
31:23	<i>Reserved</i>	RsvdP	No	0-0h

11.16.15 **Device-Specific Registers – Debug
(Offsets A30h – A74h)**

This section details the Device-Specific Debug register. This register is implemented only in the Upstream Port. [Table 11-31](#) defines the register map.

**Table 11-31. Device-Specific Debug Register Map
(Offsets A30h – A74h) (Upstream Port)**

31 30 29 28 27 26 25 24																23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																
<i>Reserved</i>																<i>Debug</i>																																A30h
<i>Reserved</i>																																																A34h – A74h

**Register 11-168. A30h Debug
(Upstream Port)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
1:0	<p>Interrupt Fencing Mode Select</p> <p><i>Note:</i> A Fundamental Reset is needed to recover from Fencing errors.</p> <p>Mode 1 (Default)</p> <ol style="list-style-type: none"> When the PEX 8747 receives a packet with a Fatal error (Malformed, DLL Protocol error) from an external device, or the device detects a Credit Overflow, Receiver Overflow, or Surprise Link Down, the switch logs the Header on the corresponding Port, sends a Fatal Error Message to the Host, then asserts FATAL_ERR#. When the PEX 8747 detects an internal Fatal error (ECC failure), the switch sends a Fatal Interrupt Message to the Host and asserts FATAL_ERR#. In certain situations, delivery of the interrupt is not guaranteed; however, the signal is always asserted upon a Fatal event. <p>Mode 2 (Generate Internal Reset)</p> <p>Upon Fatal error (internal or external) detection, an internal Chip Level reset is asserted (equivalent to an In-Band Reset from the Upstream Port). No Error Messages are generated, and no attempt is made to block packets in transit.</p> <p>Mode 3 (Block All Packet Transmission)</p> <p>Upon Fatal error (internal or external) detection, the Port logs the error in the Uncorrectable Error Status register (offset FB8h), then asserts FATAL_ERR#. This Fatal error detection blocks all the Ports from sending out TLPs. No Error Messages are generated. If a packet is already in transmission, an EDB is inserted to cancel the packet.</p> <p>Mode 4 (Block All Packet Transmission and Create Surprise Down)</p> <p>In addition to the Mode 3 actions, the PEX 8747 forces the Upstream Link to go down, thus causing a Surprise Down event on the Link, so that the Host is notified.</p> <p>00b = Mode 1 (default) 01b = Mode 2 – Generate Internal Reset 10b = Mode 3 – Block All Packet Transmission 11b = Mode 4 – Block All Packet Transmission and Create Surprise Down</p>	RWS	Yes	00b
2	<p>Upstream Hot Reset Control</p> <p>0 = Reset all logic, except Sticky bits and Device-Specific registers 1 = Reset only the Configuration Space registers of all Ports defined by the <i>PCI Express Base r3.0</i></p> <p><i>Note:</i> Only a Fundamental Reset serial EEPROM load affects this bit.</p>	RWS	Yes	0
3	<p>Disable Serial EEPROM Load on Hot Reset</p> <p>0 = Enables serial EEPROM load upon Upstream Port Hot Reset or <i>DL_Down</i> state 1 = Disables serial EEPROM load upon Upstream Port Hot Reset or <i>DL_Down</i> state</p>	RWS	Yes	0

**Register 11-168. A30h Debug
(Upstream Port) (Cont.)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4	Upstream Port DL_Down Reset Propagation Disable Setting this bit: <ul style="list-style-type: none"> Enables the Upstream Port to ignore a Hot Reset training sequence, Blocks the PEX 8747 from manifesting an internal reset due to a DL_Down event, and Prevents the Downstream Ports from issuing a Hot Reset to Downstream devices when a Hot Reset or DL_Down event occurs on the Upstream Link 	RWS	Yes	0
5	Factory Test Only	RWS	Yes	0
23:6	Reserved	RsvdP	No	0-0h
31:24	Reserved	RsvdP	No	00h

11.17 Latency Tolerance Reporting Extended Capability Registers (Offsets B00h – B08h)

This section details the Latency Tolerance Reporting (LTR) Extended Capability registers. [Table 11-32](#) defines the register map.

Table 11-32. LTR Extended Capability Register Map (Upstream Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Next Capability Offset (B70h) (Upstream)																Capability Version (1h) (Upstream)				PCI Express Extended Capability ID (0018h) (Upstream)																B00h
<i>Reserved</i> (Downstream)																																				
Max No-Snoop Latency (Upstream) <i>Reserved</i> (Downstream)																Max Snoop Latency (Upstream) <i>Reserved</i> (Downstream)																B04h				
LTR Message Received Status (Upstream) <i>Reserved</i> (Downstream)																																B08h				

Register 11-169. B00h LTR Extended Capability Header (Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID Program to 0018h, as required by the <i>PCI Express Base r3.0</i> .	Upstream	ROS	Yes	0018h
	Reserved	Downstream	RsvdP	No	0000h
19:16	Capability Version Program to 1h, as required by the <i>PCI Express Base r3.0</i> .	Upstream	ROS	Yes	1h
	Reserved	Downstream	RsvdP	No	0h
31:20	Next Capability Offset Program to B70h, which addresses the Vendor-Specific Extended Capability 2 structure.	Upstream	ROS	Yes	B70h
	Reserved	Downstream	RsvdP	No	000h

Register 11-170. B04h Max Snoop/No-Snoop Latency (Upstream Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Max Snoop Latency					
9:0	Max Snoop LatencyValue Along with field [12:10] (<i>Max Snoop LatencyScale</i>), this register specifies the maximum Snoop latency that the PEX 8747 is allowed to request. Software should program this field to the platform's maximum supported latency, or less.	Upstream	RW	Yes	0-0h
	Reserved	Downstream	RsvdP	No	0-0h
12:10	Max Snoop LatencyScale Provides a scale for the value contained within field [9:0] (<i>Max Snoop LatencyValue</i>). The encoding is the same as the <i>LatencyScale</i> fields in the LTR Message. (Refer to the <i>PCI Express Base r3.0</i> , Section 6.18.) Hardware operation is undefined if software writes a Not Permitted value to this field.	Upstream	RW	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
15:13	Reserved		RsvdP	No	000b
Max No-Snoop Latency					
25:16	Max No-Snoop LatencyValue Along with field [28:26] (<i>Max No-Snoop LatencyScale</i>), this register specifies the maximum No-Snoop latency that the PEX 8747 is allowed to request. Software should program this field to the platform's maximum supported latency, or less.	Upstream	RW	Yes	0-0h
	Reserved	Downstream	RsvdP	No	0-0h
28:26	Max No-Snoop LatencyScale Provides a scale for the value contained within field [25:16] (<i>Max No-Snoop LatencyValue</i>). The encoding is the same as the <i>LatencyScale</i> fields in the LTR Message. (Refer to the <i>PCI Express Base r3.0</i> , Section 6.18.) Hardware operation is undefined if software writes a Not Permitted value to this field.	Upstream	RW	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
31:29	Reserved		RsvdP	No	000b

Register 11-171. B08h LTR Message Received Status (Upstream Port)

Bit(s)	Description	Upstream Port x	Type	Serial EEPROM and I ² C	Default
<p>When driven with a value of 1, this register holds the Port in reset, including the Port PCI-to-PCI bridge and the hierarchy below it. A value of 0 indicates to un-reset the PCI-to-PCI bridge and the hierarchy below it.</p> <p>Notes: The Downstream Port bits are Reserved, RsvdP, not serial EEPROM nor I²C writable, and have a default value of 0.</p> <p>The Upstream Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p>					
0	Port x LTR Initiate or Received	0	RO	Yes	0
5:1	Factory Test Only		RsvdP	No	0-0h
7:6	Reserved		RsvdP	No	00b
8	Port x LTR Initiate or Received	8	RO	Yes	0
9		9	RO	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Port x LTR Initiate or Received	16	RO	Yes	0
17		17	RO	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
31:22	Reserved		RsvdP	No	0-0h

11.18 Device-Specific Registers (Offsets B70h – DFCh)

This section details the Device-Specific registers located at offsets B70h through DFCh. Device-Specific registers are unique to the PEX 8747 and not referenced in the *PCI Express Base r3.0*. Table 11-16 defines the register map.

Other Device-Specific registers are detailed in:

- Section 11.16, “Device-Specific Registers (Offsets 1C0h – A74h)”
- Section 11.21, “Device-Specific Registers (Offsets F30h – FB0h)”

Note: *It is recommended that these registers not be changed from their default values.*

Table 11-33. Device-Specific Register Map (Offsets B70h – DFCh)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Next Capability Offset 2 (000h)																1h				PCI Express Extended Capability ID 2 (000Bh)																B70h
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)																																...				
Device-Specific Registers – Physical Layer (Offsets B80h – C88h)																																B7Ch				
																																B80h				
																																...				
																																C88h				
Reserved																																C8Ch – DFCh				

11.18.1 Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)

This section details the Device-Specific Vendor-Specific Extended Capability 2 registers. [Table 11-34](#) defines the register map.

Table 11-34. Device-Specific, Vendor-Specific Extended Capability 2 Register Map (All Ports)

<div> <div>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</div> <div>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</div> </div>																															
Next Capability Offset 2 (000h)															Capability Version 2 (1h)					PCI Express Extended Capability ID 2 (000Bh)											B70h
Vendor-Specific Header 2																															B74h
Hardwired Device ID															Hardwired Vendor ID																B78h
<i>Reserved</i>																				Hardwired Revision ID											B7Ch

Register 11-172. B70h Vendor-Specific Extended Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID 2 Program to 000Bh, to indicate that the Capability structure is the Vendor-Specific Extended Capability structure.	ROS	Yes	000Bh
19:16	Capability Version 2	ROS	Yes	1h
31:20	Next Capability Offset 2 000h = This extended capability is the last extended capability in the PEX 8747 Extended Capabilities list	ROS	Yes	000h

Register 11-173. B74h Vendor-Specific Header 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	Vendor-Specific ID 2 ID Number of this Extended Capability structure.	ROS	Yes	0001h
19:16	Vendor-Specific Rev 2 Version Number of this structure.	ROS	Yes	0h
31:20	Vendor-Specific Length 2 Quantity of bytes in the entire structure.	ROS	Yes	010h

**Register 11-174. B78h PLX Hardwired Configuration ID
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	Hardwired Vendor ID Always returns the PLX PCI-SIG-assigned Vendor ID value, 10B5h.	ROS	No	10B5h
31:16	Hardwired Device ID Always returns the PEX 8747 default Device ID value, 8747h.	ROS	No	8747h

**Register 11-175. B7Ch PLX Hardwired Revision ID
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
7:0	Hardwired Revision ID Always returns the PEX 8747 default Revision ID value – BAh.	ROS	No	Current Rev # (BAh)
31:8	Reserved	RsvdP	No	0000_00h

11.18.2 Device-Specific Registers – Physical Layer (Offsets B80h – C88h)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets B80h through C88h. [Table 11-35](#) defines the register map.

Other Device-Specific PHY registers are detailed in [Section 11.16.4, “Device-Specific Registers – Physical Layer \(Offsets 200h – 25Ch\).”](#)

Table 11-35. Device-Specific PHY Register Map (Offsets B80h – C88h) (Ports^a)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Factory Test Only/Reserved								SerDes Control																								B80h
Factory Test Only												Synchronous Advertised N_FTS																B84h				
Reserved																																B88h
Factory Test Only												Asynchronous Advertised N_FTS																B8Ch				
Reserved																																B90h
Reserved				Factory Test Only																PIPE Transmit Parameter Control								B94h				
2.5 GT/s -3.5 dB Transmit Parameters																																B98h
5.0 GT/s -6 dB Transmit Parameters																																B9Ch
5.0 GT/s -3.5 dB Transmit Parameters																																BA0h
8.0 GT/s 0 dB Transmit Parameters																																BA4h
Reserved																														BA8h –		BB4h
Reserved				DC Balance Control																												BB8h
Trained Coefficient Status																																BBCh
Port Accumulation Control																																BC0h
Recovery Diagnostic																																BC4h
Factory Test Only												User Lane Equalization Control																BC8h				
Reserved																														BCCh –		BD0h
Gen 3 Coefficient Values																																BD4h
Equalization Control																																BD8h
Factory Test Only/Reserved																				Signal Detect Level												BDCh
Gen 3 LFSR Seed																																BE0h
Factory Test Only																														BE4h –		BE8h
TLP Round Trip Timer Control																																BECh
Factory Test Only												Port Receiver Error Counter																BF0h				
Reserved																																BF4h
Factory Test Only																																BF8h
AHB Access Control																																BFCh
Reserved																														C00h –		C88h

a. Certain registers are Port-specific, others are Station-specific; all are Device-specific.

**Register 11-176. B80h SerDes Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register controls SerDes logic parameters.</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
2:0	Electrical Idle Inference Time Select Selects the amount of time to wait until no SKIP Ordered-Sets are detected, for Electrical Idle to be inferred. Does not affect Electrical Idle inference during the <i>Recovery.Speed</i> substate. 000b = 4 μ s 001b = 6 μ s 010b = 8 μ s 011b = 16 μ s 100b = 32 μ s 101b = 64 μ s 110b = 128 μ s (default) 111b = 256 μ s	RWS	Yes	110b
3	Reserved	RsvdP	No	0
5:4	Recovery.Speed Electrical Idle Inference Time Select	RWS	Yes	00b
7:6	Reserved	RsvdP	No	00b
8	Force SerDes Out Transmit Data (TD) [19:0] Force enable. 1 = All bits of the TD[19:0] inputs, of the SerDes in this Station, are forced to the state specified by bit 9 (<i>SerDes Out Data Force State</i>)	RWS	Yes	0
9	SerDes Out Data Force State TD[19:0] Force state. Specifies the state to which the TD[19:0] inputs are forced, when bit 8 (<i>Force SerDes Out</i>) is Set.	RWS	Yes	0
11:10	Reserved	RsvdP	No	00b
14:12	Tx Parameter Port Select Selects the Port to which the value written in the Tx Parameter Control registers will be applied.	RWS	Yes	000b
15	Reserved	RsvdP	No	0
21:16	Tx Margin Override	RWS	Yes	0-0h
23:22	Reserved	RsvdP	No	00b
27:24	Factory Test Only	RWS	Yes	0h
31:28	Reserved	RsvdP	No	0h

**Register 11-177. B84h Synchronous Advertised N_FTS
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
This register advertises the Number of Fast Training Sets (N_FTS) values for synchronous clocking. <i>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> Port 0, field [15:8], is Factory Test Only , RsvdP, not serial EEPROM-writable, and has a default value of 00h. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.					
7:0	Port x Synchronous Tx N_FTS When clocking is synchronous, specifies the N_FTS field value in Training Sets transmitted by the Port, when the Port's Link Control register <i>Common Clock Configuration</i> bit (offset 78h[6]) is Set.	0, 8, 16	RWS	Yes	80h
15:8		9, 17	RWS	Yes	80h
31:16	Factory Test Only		RsvdP	No	0000h

**Register 11-178. B8Ch Asynchronous Advertised N_FTS
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
This register advertises the Number of Fast Training Sets (N_FTS) values for asynchronous clocking. <i>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> Port 0, field [15:8], is Factory Test Only , RsvdP, not serial EEPROM-writable, and has a default value of 00h. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.					
7:0	Port x Asynchronous Tx N_FTS When clocking is asynchronous, specifies the N_FTS field value in Training Sets transmitted by the Port, when the Port's Link Control register <i>Common Clock Configuration</i> bit (offset 78h[6]) is Cleared.	9, 17	RWS	Yes	A0h
15:8		0, 8, 16	RWS	Yes	A0h
31:16	Factory Test Only		RsvdP	No	0000h

**Register 11-179. B94h PIPE Transmit Parameter Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p><i>Notes:</i> Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bits [7:4], are Factory Test Only, RsvdP, not serial EEPROM-writable, and have a default value of 0h.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>				
2:0	Port 0, 8, 16 Tx Margin Applied when TxMargin Override0 = 1.	RWS	Yes	000b
3	Port 0, 8, 16 Tx Swing	RWS	Yes	0
6:4	Port 9, 17 Tx Margin Applied when TxMargin Override1 = 1.	RWS	Yes	000b
7	Port 9, 17 Tx Swing	RWS	Yes	0
23:8	Factory Test Only	RsvdP	No	0000h
31:24	Reserved	RsvdP	No	00h

**Register 11-180. B98h 2.5 GT/s -3.5 dB Transmit Parameters
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
2:0	TX_PREDRV_DLY Pre-drive delay.	RWS	Yes	000b
5:3	TXEQ_D2 Transmit equalization.	RWS	Yes	000b
7:6	TX_EQ_E Transmit equalization.	RWS	Yes	00b
10:8	TXEQ_MODE Transmit equalization mode.	RWS	Yes	000b
13:11	TX_ETLEV	RWS	Yes	000b
16:14	TX_D2LEV	RWS	Yes	000b
20:17	TX_LEV Transmit amplitude control.	RWS	Yes	0h
23:21	TX_SR_SET	RWS	Yes	000b
26:24	TX_DTLEV Transmit de-emphasis control.	RWS	Yes	000b
28:27	TX_RT_SET	RWS	Yes	00b
30:29	<i>Reserved</i>	RsvdP	Yes	00b
31	Transmit Parameter Override Enable	RWS	Yes	0

**Register 11-181. B9Ch 5.0 GT/s -6 dB Transmit Parameters
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
2:0	TX_PREDRV_DLY Pre-drive delay.	RWS	Yes	000b
5:3	TXEQ_D2 Transmit equalization.	RWS	Yes	000b
7:6	TX_EQ_E Transmit equalization.	RWS	Yes	00b
10:8	TXEQ_MODE Transmit equalization mode.	RWS	Yes	000b
13:11	TX_ETLEV	RWS	Yes	000b
16:14	TX_D2LEV	RWS	Yes	000b
20:17	TX_LEV Transmit amplitude control.	RWS	Yes	0h
23:21	TX_SR_SET	RWS	Yes	000b
26:24	TX_DTLEV Transmit de-emphasis control.	RWS	Yes	000b
28:27	TX_RT_SET	RWS	Yes	00b
30:29	<i>Reserved</i>	RsvdP	Yes	00b
31	Transmit Parameter Override Enable	RWS	Yes	0

**Register 11-182. BA0h 5.0 GT/s -3.5 dB Transmit Parameters
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
2:0	TX_PREDRV_DLY Pre-drive delay.	RWS	Yes	000b
5:3	TXEQ_D2 Transmit equalization.	RWS	Yes	000b
7:6	TX_EQ_E Transmit equalization.	RWS	Yes	00b
10:8	TXEQ_MODE Transmit equalization mode.	RWS	Yes	000b
13:11	TX_ETLEV	RWS	Yes	000b
16:14	TX_D2LEV	RWS	Yes	000b
20:17	TX_LEV Transmit amplitude control.	RWS	Yes	0h
23:21	TX_SR_SET	RWS	Yes	000b
26:24	TX_DTLEV Transmit de-emphasis control.	RWS	Yes	000b
28:27	TX_RT_SET	RWS	Yes	00b
30:29	<i>Reserved</i>	RsvdP	Yes	00b
31	Transmit Parameter Override Enable	RWS	Yes	0

**Register 11-183. BA4h 8.0 GT/s 0 dB Transmit Parameters
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
2:0	TX_PREDRV_DLY Pre-drive delay.	RWS	Yes	000b
5:3	TXEQ_D2 Transmit equalization.	RWS	Yes	000b
7:6	TX_EQ_E Transmit equalization.	RWS	Yes	00b
10:8	TXEQ_MODE Transmit equalization mode.	RWS	Yes	000b
13:11	TX_ETLEV	RWS	Yes	000b
16:14	TX_D2LEV	RWS	Yes	000b
20:17	TX_LEV Transmit amplitude control.	RWS	Yes	0h
23:21	TX_SR_SET	RWS	Yes	000b
26:24	TX_DTLEV Transmit de-emphasis control.	RWS	Yes	000b
28:27	TX_RT_SET	RWS	Yes	00b
30:29	<i>Reserved</i>	RsvdP	Yes	00b
31	Transmit Parameter Override Enable	RWS	Yes	0

**Register 11-184. BB8h DC Balance Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
5:0	Port DC Balance Enable	RWS	Yes	3Fh
7:6	Reserved	RsvdP	No	00b
15:8	DC Balance Symbol 14 Threshold	RWS	Yes	20h
23:16	DC Balance Symbol 15 Threshold	RWS	Yes	10h
31:24	Reserved	RsvdP	No	00h

**Register 11-185. BBCh Trained Coefficient Status
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.				
5:0	Pre-Cursor Coefficient	ROS	No	0-0h
7:6	Reserved	RsvdP	No	00b
13:8	Main Cursor Coefficient	ROS	No	0-0h
15:14	Reserved	RsvdP	No	00b
21:16	Post-Cursor Coefficient	ROS	No	0-0h
23:22	Reserved	RsvdP	No	00b
24	Near-End/Far-End Select	RWS	Yes	0
27:25	Reserved	RsvdP	No	000b
31:28	Lane Select	RWS	Yes	0h

**Register 11-186. BC0h Port Accumulation Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<i>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
1:0	Lock Down Mode Selects the Station's Port 0 Lock Down mode. Bit 0 determines the final Port configuration. Bit 1 enables/disables PIPE Reversal mode.	RWS	Yes	00b
2	Lock Down Mode Enable Enables the Station's Port 0 Lock Down mode when Autonomous Port Accumulation mode is also enabled (bit 7 (<i>Autonomous Port Accumulation Mode Enable</i>) is Set). 0 = Disables Lock Down mode 1 = Enables Lock Down mode	RWS	Yes	0
6:3	Reserved	RsvdP	No	0h
7	Autonomous Port Accumulation Mode Enable 0 = Disables Autonomous Port Accumulation mode 1 = Enables Autonomous Port Accumulation mode	RWS	Yes (Serial EEPROM only)	0
7	Reserved	RsvdP	No	0
10:8	Auto Port Configuration Returns the current Port configuration selected by the Port Accumulation logic. <i>Note: Refer to Table 11-5 for the Port Configurations associated with these values.</i> 001b = 1 010b = 2 All other encodings are Reserved .	ROS	No	PCFG
11	PIPE Reverse Returns the PIPE Reversal mode selected by the Port Accumulation logic. 0 = PIPE Reversal mode is disabled (bit 1 of field [1:0] (<i>Lock Down Mode</i>) is Cleared) 1 = PIPE Reversal mode is enabled (bit 1 of field [1:0] (<i>Lock Down Mode</i>) is Set)	ROS	No	PCFG
31:12	Reserved	RsvdP	No	0000_0h

**Register 11-187. BC4h Recovery Diagnostic
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>				
15:0	Recovery Counter Quantity of times that the Port entered the <i>Recovery</i> state since the Counter was last Cleared.	ROS	No	PCFG
23:16	Reserved	RsvdP	No	00h
26:24	Port Select Selects the Port for which to return the Recovery Count, or the Port's Recovery Counter to Clear.	RW	Yes	000b
30:27	Reserved	RsvdP	No	0h
31	Clear Recovery Count Writing 1 to this bit Clears the Port's Recovery Counter.	RZ	Yes	0

**Register 11-188. BC8h User Lane Equalization Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
Notes: <i>The Port x column is provided to indicate the Port Number associated with fields that include "Port x" in their name.</i> <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i> <i>Port 0, field [15:8], is Factory Test Only, RsvdP, not serial EEPROM-writable, and has a default value of 00h.</i> <i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>					
7:0	User Lane Equalization Control Data for Port x These fields allow MemWr commands (rather than the serial EEPROM) to load the Lane x Equalization Control register(s) (offset(s) 118h through 134h) if this register is written.	0, 8, 16	RWS	Yes	00h
15:8		9, 17	RWS	Yes	00h
31:16	Factory Test Only		RsvdP	No	0000h

**Register 11-189. BD4h Gen 3 Coefficient Values
(Ports 0, 8, and 16)**

Bit(s)	Description		Type	Serial EEPROM and I ² C	Default
<i>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i>					
<i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>					
17:0	Preset 0 Coefficients		RWS	Yes	1_0BC0h
	Bit(s)	Description			
	5:0	Preshoot			
	11:6	Main			
	17:12	De-Emphasis			
23:18	Gen 3 FS Value		RWS	Yes	3Fh
27:24	Preset Select		RWS	Yes	0h
29:28	Factory Test Only		RWS	Yes	00b
30	Reserved		RsvdP	No	0
31	Coefficient Write Enable Control Must be Set to enable modification of bits [23:0].		RWS	Yes	0

**Register 11-190. BD8h Equalization Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, bit 1, is Factory Test Only, RsvdP, not serial EEPROM-writable, and has a default value of 0.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Port x Bypass Equalization Directs Downstream Ports to bypass the Transmitter Equalization phases.	0, 8, 16	RWS	Yes	0
1		9, 17	RWS	Yes	0
5:2	Factory Test Only		RsvdP	No	0h
7:6	Reserved		RsvdP	No	00b
8	Set start_equalization_w_preset Directs Downstream Ports to Set the start_equalization_w_preset variable to 1 at the appropriate time.	9, 17	RWS	Yes	0
9		0, 8, 16	RWS	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b

**Register 11-190. BD8h Equalization Control
(Ports 0, 8, and 16) (Cont.)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
16	Reset EIEOS Counter Directs Ports to Set the <i>Reset EIEOS Counter</i> bit in the TS1 Ordered-Sets transmitted during its Equalization phase.	0, 8, 16	RWS	Yes	0
17	Note: Port 0, bit 17, is Factory Test Only , RsvdP, not serial EEPROM-writable, and has a default value of 0.	9, 17	RWS	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
23:22	Reserved		RsvdP	No	00b
26:24	Receiver Evaluation Period Selects the length of time to use for the Receiver Evaluation period. Silicon Revision BA 000b = 1 μ s 001b = 2 μ s 010b = 4 μ s 011b = 8 μ s 100b = 26 μ s (default) 101b = 32 μ s 110b = 64 μ s 111b = 128 μ s Silicon Revision CA 000b = 4 μ s 001b = 8 μ s 010b = 16 μ s 011b = 32 μ s 100b = 64 μ s (default) 101b = 128 μ s 110b = 256 μ s 111b = 512 μ s		RWS	Yes	100b
31:27	Receiver Evaluation Threshold Selects the maximum quantity of Receiver Evaluation periods per Transmitter Tuning phase.		RWS	Yes	19h

**Register 11-191. BDCh Signal Detect Level
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>This register programs the Signal Detect Level for 2.5 and 8.0 GT/s; writes to this register do not affect the Signal Detect Level for 5.0 GT/s. The Signal Detect Level for individual Lanes and/or SerDes quads can be programmed, independently, for 2.5, 5.0 and 8.0 GT/s, through the AHB Access Control register (Port 0, 8, or 16, offset BFCh).</p> <p>Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i></p> <p><i>Port 0, field [6:4], is Factory Test Only, RsvdP, not serial EEPROM-writable, and has a default value of 00b.</i></p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
2:0	Port 0, 8, 16 Signal Detect Level	RWS	Yes	010b
3	Reserved	RsvdP	No	0
6:4	Port 9, 17 Signal Detect Level	RWS	Yes	010b
7	Reserved	RsvdP	No	0
22:8	Factory Test Only/Reserved	RsvdP	No	0-0h
31:23	Reserved	RsvdP	No	0-0h

**Register 11-192. BE0h Gen 3 LFSR Seed
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</i> <i>The Port 0 bits are for Lanes [0-15]. The Port 8 bits are for Lanes [16-31]. The Port 16 bits are for Lanes [32-47].</i>				
22:0	LFSR Seed Linear Feedback Shift register (LFSR) seed. Used as the Lane-specific scrambler seed for the Gen 3 scrambler/de-scrambler.	RWS	Yes	1D_BFBCh
23	Reserved	RsvdP	No	0
26:24	Lane Select Specifies which of eight register banks in field [22:0] (<i>LFSR Seed</i>) is to be accessed. (Lanes are by Station.) 000b = Lanes 0, 8 (default) 001b = Lanes 1, 9 010b = Lanes 2, 10 011b = Lanes 3, 11 100b = Lanes 4, 12 101b = Lanes 5, 13 110b = Lanes 6, 14 111b = Lanes 7, 15	RWS	Yes	000b
30:27	Reserved	RsvdP	No	0h
31	LFSR Seed Write Enable Control Must be Set to enable modification of field [22:0] (<i>LFSR Seed</i>).	RWS	Yes	0

**Register 11-193. BECh TLP Round Trip Timer Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default	
Notes: <i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</i>					
<i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i>					
0	TRT Enable Enable TLP Round Trip (TRT) Timer. 0 = TLP Round Trip Timer is disabled 1 = TLP Round Trip Timer is enabled	RW	Yes	0	
1	TRT Clear Always returns a value of 0 when read. 1 = Clear minimum and maximum registers	RW	Yes	0	
2	TRT Read Maximum 0 = Return minimum time in field [31:16] (<i>TRT Time</i>) 1 = Return maximum time in field [31:16] (<i>TRT Time</i>)	RW	Yes	0	
3	TRT Active 1 = TRT Timer is active, time update is pending	RO	No	0	
6:4	TRT Port Select	RW	Yes	000b	
7	<i>Reserved</i>	RsvdP	No	0	
14:8	TRT TLP Type and Format Select		RWS	Yes	0-0h
	Bit(s)	Description/Function			
	12:8	Non-Posted TLP Type			
	14:13	Non-Posted TLP Format			
15	TRT Ignore Format Field 1 = Detect egress TLPs, by matching only bits [12:8] (<i>Non-Posted TLP Type</i>) of field [14:8]	RW	Yes	0	
31:16	TRT Time Returns the minimum or maximum round trip time, depending upon the bit 2 (<i>TRT Read Maximum</i>) state.	RO	No	FFFFh	

**Register 11-194. BF0h Port Receiver Error Counter
(Ports 0, 8, and 16)**

Bit(s)	Description	Port x	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name. Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>Port 0, field [15:8], is Factory Test Only, RsvdP, not serial EEPROM-writable, and has a default value of 00h.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
7:0	Port x Receiver Error Counter When read, returns the quantity of Receiver errors that the Port detected (Receiver Error Counter). The Error Counter saturates at 255.	0, 8, 16	RW1C	No	00h
15:8		9, 17	RW1C	No	00h
31:16	Factory Test Only		RsvdP	No	0000h

**Register 11-195. BFCh AHB Access Control
(Ports 0, 8, and 16)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
<p>In addition to the functions defined for each bit/field, this register can also be used to program the Signal Detect Level, per Lane or SerDes Quad, independently, for each of the three data rates (2.5, 5.0, and 8.0 GT/s), by Station. (Refer to Table 11-36.) Signal Detect Level is defined by 3-bit values (48 fields, per Station). Because the AHB Data window is 8 bits wide, a Read/Modify/Write sequence is required, to preserve the values of other bits within the register. The 3-bit field for 5.0 GT/s exists within one 8-bit window; therefore, only one Read/Modify/Write sequence is needed. However the 3-bit fields for 2.5 and 8.0 GT/s are each split between two offsets; therefore, two Read/Modify/Write sequences are required to modify a single 3-bit field.</p> <p><i>For example</i>, to program SerDes Quad 0 to use value 3 during 8.0 GT/S, software performs the following actions:</p> <ol style="list-style-type: none"> 1. Writes the value 000E_5800h to offset BFCh. 2. Reads the register (to preserve bits [7:1]). 3. Clears bit 0 (msb of 3-bit Signal Detect value). 4. ORs the field [7:0] value with 008E_5800h. 5. Writes the result back to offset BFCh. 6. Writes the value 000E_5700h to offset BFCh. 7. Reads the register (to preserve bits [5:0]). 8. Changes the value of bits [7:6] to 10b (lsb of Signal Detect value). 9. ORs the field [7:0] value with 008E_5700h. 10. Writes the result back to offset BFCh. <p>Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p><i>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</i></p>				
7:0	AHB Data When an AHB register is being written, the data in this field is the Write data. When an AHB register is read, the response (Read) data is returned in this field.	RWS	Yes	00h
20:8	AHB Address Specifies the address of the AHB register being accessed.	RWS	Yes	0-0h
22:21	AHB Quad Select Specifies the SerDes quad to which the AHB access is directed.	RWS	Yes	00b
23	AHB -Read/+Write Specifies the AHB access type. 0 = Read 1 = Write	RWS	Yes	0
29:24	Reserved	RsvdP	No	0-0h
30	AHB Access Timeout 1 = An AHB register access did not return AHB_Ready	RW1C	No	0
31	AHB Ready 0 = Indicates that the AHB Controller is processing the previous access or client accesses 1 = Indicates that the AHB Controller is ready to accept a new access	ROS	No	1

Table 11-36. Signal Level Detect Read/Modify/Write Values for AHB Access Control Register (Ports 0, 8, and 16, offset BFCh)^a

Quad	Lane(s)	Gen 1 (2.5 GT/s)						Gen 2 (5.0 GT/s)			Gen 3 (8.0 GT/s)					
		Read/Modify/Write			Read/Modify/Write			Read/Modify/Write			Read/Modify/Write			Read/Modify/Write		
		Write (bit 23 = 0)	Read (bit 23 = 1) [7:1]	Write (bit 23 = 1) OR [7:1] OR	Write (bit 23 = 0)	Read (bit 23 = 1) [5:0]	Write (bit 23 = 1) OR [5:0] OR	Write (bit 23 = 0)	Read (bit 23 = 1) [4:0]	Write (bit 23 = 1) OR [4:0] OR	Write (bit 23 = 0)	Read (bit 23 = 1) [7:1]	Write (bit 23 = 1) OR [7:1] OR	Write (bit 23 = 0)	Read (bit 23 = 1) [5:0]	Write (bit 23 = 1) OR [5:0] OR
				[[0] = msb]			[[7:6] = lsb]			(bits [7:5])			[[0] = msb]			[[7:6] = lsb]
0	(All 4)	000E1300h		008E13_h	000E1200h		008E12_h	000E4F00h		008E4F_h	000E5800h		008E58_h	000E5700h		008E57_h
	0	00021300h		008213_h	00021200h		008212_h	00024F00h		00824F_h	00025800h		008258_h	00025700h		008257_h
	1	00041300h		008413_h	00041200h		008412_h	00044F00h		00844F_h	00045800h		008458_h	00045700h		008457_h
	2	00061300h		008613_h	00061200h		008612_h	00064F00h		00864F_h	00065800h		008658_h	00065700h		008657_h
	3	00081300h		008813_h	00081200h		008812_h	00084F00h		00884F_h	00085800h		008858_h	00085700h		008857_h
1	(All 4)	002E1300h		00AE13_h	002E1200h		00AE12_h	002E4F00h		00AE4F_h	002E5800h		00AE58_h	002E5700h		00AE57_h
	4	00221300h		00A213_h	00221200h		00A212_h	00224F00h		00A24F_h	00225800h		00A258_h	00225700h		00A257_h
	5	00241300h		00A413_h	00241200h		00A412_h	00244F00h		00A44F_h	00245800h		00A458_h	00245700h		00A457_h
	6	00261300h		00A613_h	00261200h		00A612_h	00264F00h		00A64F_h	00265800h		00A658_h	00265700h		00A657_h
	7	00281300h		00A813_h	00281200h		00A812_h	00284F00h		00A84F_h	00285800h		00A858_h	00285700h		00A857_h
2	(All 4)	004E1300h		00CE13_h	004E1200h		00CE12_h	004E4F00h		00CE4F_h	004E5800h		00CE58_h	004E5700h		00CE57_h
	8	00421300h		00C213_h	00421200h		00C212_h	00424F00h		00C24F_h	00425800h		00C258_h	00425700h		00C257_h
	9	00441300h		00C413_h	00441200h		00C412_h	00444F00h		00C44F_h	00445800h		00C458_h	00445700h		00C457_h
	10	00461300h		00C613_h	00461200h		00C612_h	00464F00h		00C64F_h	00465800h		00C658_h	00465700h		00C657_h
	11	00481300h		00C813_h	00481200h		00C812_h	00484F00h		00C84F_h	00485800h		00C858_h	00485700h		00C857_h
3	(All 4)	006E1300h		00EE13_h	006E1200h		00EE12_h	006E4F00h		00EE4F_h	006E5800h		00EE58_h	006E5700h		00EE57_h
	12	00621300h		00E213_h	00621200h		00E212_h	00624F00h		00E24F_h	00625800h		00E258_h	00625700h		00E257_h
	13	00641300h		00E413_h	00641200h		00E412_h	00644F00h		00E44F_h	00645800h		00E458_h	00645700h		00E457_h
	14	00661300h		00E613_h	00661200h		00E612_h	00664F00h		00E64F_h	00665800h		00E658_h	00665700h		00E657_h
	15	00681300h		00E813_h	00681200h		00E812_h	00684F00h		00E84F_h	00685800h		00E858_h	00685700h		00E857_h

a. Throughout this data book, 32-bit hex values usually include an underscore character (_), separating the combined 16-bit values. In this table, however, that underscore is not used, to avoid confusion with the underscores used for placeholder values.

11.19 Multicast Extended Capability Registers (Offsets E00h – E2Ch)

This section details the Multicast Extended Capability registers. [Table 11-37](#) defines the register map. Multicast is described, in detail, in [Section 8.6, “Multicast.”](#)

Table 11-37. Multicast Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Next Capability Offset (B00h or F24h)																Capability Version (1h)				PCI Express Extended Capability ID (0012h)																E00h
Multicast Control																Multicast Extended Capability																E04h				
Multicast BAR0																																E08h				
Multicast BAR1																																E0Ch				
Multicast Receive 0																																E10h				
Multicast Receive 1																																E14h				
Multicast Block All 0																																E18h				
Multicast Block All 1																																E1Ch				
Multicast Block Untranslated 0																																E20h				
Multicast Block Untranslated 1																																E24h				
Multicast Overlay BAR0																																E28h				
Multicast Overlay BAR1																																E2Ch				

**Register 11-196. E00h Multicast Extended Capability Header
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID Program to 0012h, to indicate that the Extended Capability structure is the Multicast Extended Capability structure.		ROS	Yes	0012h
19:16	Capability Version		ROS	Yes	1h
31:20	Next Capability Offset Next extended capability is the LTR Extended Capability structure, offset B00h.	Upstream	ROS	Yes	B00h
	Next extended capability is the ACS Extended Capability structure, offset F24h.	Downstream	ROS	Yes	F24h

**Register 11-197. E04h Multicast Extended Capability and Control
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Multicast Extended Capability				
5:0	MC Max Group 00h = Indicates that one Multicast Group is supported 3Fh = Indicates the maximum quantity of Multicast Groups that the component supports, encoded as $M-1$	ROS	Yes	3Fh
14:6	<i>Reserved</i>	RsvdP	No	0-0h
15	MC ECRC Generation Supported 0 = ECRC generation is not supported in Multicast 1 = ECRC generation is supported in Multicast	ROS	Yes	1
Multicast Control				
21:16	MC Num Group Indicates the quantity of Multicast Groups configured for use, encoded as $N-1$. The behavior of this field is undefined if its value exceeds the value indicated by field [5:0] (<i>MC Max Group</i>). This parameter indirectly defines the upper limit of the Multicast Address range. This field is ignored if bit 31 (<i>MC Enable</i>) is Cleared. 00h = Indicates that one Multicast Group is configured for use	RW	Yes	0-0h
30:22	<i>Reserved</i>	RsvdP	No	0-0h
31	MC Enable 0 = Disables Multicast 1 = Enables Multicast	RW	Yes	0

**Register 11-198. E08h Multicast BAR0
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
5:0	MC Index Position The Multicast Group Number LSB location within the address. The behavior of this field is undefined if its value is less than 12 (Ch) and the Multicast Control register <i>MC Enable</i> bit (offset E04h[31]) is Set.	RW	Yes	0-0h
11:6	<i>Reserved</i>	RsvdP	No	0-0h
31:12	MC Base Address Multicast Lower Base Address[31:12]. Base address of the Multicast Address range. The behavior is undefined if: <ul style="list-style-type: none"> • Multicast Control register <i>MC Enable</i> bit (offset E04h[31]) is Set, and • Bits in this field corresponding to Address bits that contain the Multicast Group number, or Address bits less than the value indicated by field [5:0] (<i>MC Index Position</i>), are non-zero. 	RW	Yes	0000_0h

**Register 11-199. E0Ch Multicast BAR1
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Upper Base Address Multicast Upper Base Address[63:32]. Base address of the Multicast Address range. The behavior is undefined if: <ul style="list-style-type: none"> • Multicast Control register <i>MC Enable</i> bit (offset E04h[31]) is Set, and • Bits in this field corresponding to Address bits that contain the Multicast Group number, or Address bits less than the value indicated by the Multicast BAR0 register <i>MC Index Position</i> field (offset E04h[5:0]), are non-zero. 	RW	Yes	0000_0000h

**Register 11-200. E10h Multicast Receive 0
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Receive Multicast Receive[31:0]. Provides a bit Vector that denotes to which Multicast Groups the Port should forward Multicast TLPs. For each bit that is Set, this Port receives a copy of any Multicast TLPs that exist for the associated Multicast Group. Bits above MC Num Group (Multicast Extended Capability register <i>MC Num Group</i> field, offset E04h[21:16]) are ignored by hardware.	RW	Yes	0000_0000h

**Register 11-201. E14h Multicast Receive 1
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Receive Multicast Receive[63:32]. Provides a bit Vector that denotes to which Multicast Groups the Port should forward Multicast TLPs. For each bit that is Set, this Port receives a copy of any Multicast TLPs that exist for the associated Multicast Group. Bits above MC Num Group (Multicast Extended Capability register <i>MC Num Group</i> field, offset E04h[21:16]) are ignored by hardware.	RW	Yes	0000_0000h

**Register 11-202. E18h Multicast Block All 0
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Block All Multicast Block All[31:0]. Provides a bit Vector that denotes which Multicast Groups the Multicast function should block. For each bit that is Set, this Port is blocked from sending TLPs to the associated Multicast Group. Bits above MC Num Group (Multicast Extended Capability register <i>MC Num Group</i> field, offset E04h[21:16]) are ignored by hardware.	RW	Yes	0000_0000h

**Register 11-203. E1Ch Multicast Block All 1
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Block All Multicast Block All[63:32]. Provides a bit Vector that denotes which Multicast Groups the Multicast function should block. For each bit that is Set, this Port is blocked from sending TLPs to the associated Multicast Group. Bits above MC Num Group (Multicast Extended Capability register <i>MC Num Group</i> field, offset E04h[21:16]) are ignored by hardware.	RW	Yes	0000_0000h

**Register 11-204. E20h Multicast Block Untranslated 0
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Block Untranslated Multicast Block Untranslated[31:0]. Used to determine whether a TLP that includes an Untranslated Address should be blocked. For each bit that is Set, this Port is blocked from sending TLPs containing Untranslated addresses to the associated Multicast Group. Bits above MC Num Group (Multicast Extended Capability register <i>MC Num Group</i> field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

**Register 11-205. E24h Multicast Block Untranslated 1
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	MC Block Untranslated Multicast Block Untranslated[63:32]. Used to determine whether a TLP that includes an Untranslated Address should be blocked. For each bit that is Set, this Port is blocked from sending TLPs containing Untranslated addresses to the associated Multicast Group. Bits above MC Num Group (Multicast Extended Capability register <i>MC Num Group</i> field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

**Register 11-206. E28h Multicast Overlay BAR0
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Specifies the Base address of a window in Unicast space onto which Multicast TLPs output from an egress Port are overlaid by a process of address replacement. This allows a single BAR in an endpoint attached to the PEX 8747 to be used for both Unicast and Multicast traffic. At the Upstream Port, this register allows the Multicast Address range, or a portion of it, to be overlaid onto Host memory.				
5:0	MC Overlay Size Less than 06h = Disables the Overlay mechanism 06h or greater = Specifies the size (in bytes) of the Overlay Address range, as a power of 2	RW	Yes	0-0h
31:6	MC Overlay BAR Multicast Overlay Lower Base Address[31:6]. Specifies the Base address of the window onto which Multicast TLPs passing through the Multicast function will be overlaid.	RW	Yes	0-0h

**Register 11-207. E2Ch Multicast Overlay BAR1
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
Specifies the Base address of a window in Unicast space onto which Multicast TLPs output from an egress Port are overlaid by a process of address replacement. This allows a single BAR in an endpoint attached to the PEX 8747 to be used for both Unicast and Multicast traffic. At the Upstream Port, this register allows the Multicast Address range, or a portion of it, to be overlaid onto Host memory.				
31:0	MC Overlay Upper Base Address Multicast Overlay Upper Base Address[63:32]. Specifies the Base address of the window onto which Multicast TLPs passing through the Multicast function will be overlaid.	RW	Yes	0000_0000h

11.20 ACS Extended Capability Registers (Offsets F24h – F2Ch)

This section details the ACS Extended Capability registers. [Table 11-38](#) defines the register map.

Table 11-38. ACS Extended Capability Register Map (Downstream Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																							
Reserved (Upstream)																																F24h							
Next Capability Offset (B70h) (Downstream)																Capability Version (1h) (Downstream)								PCI Express Extended Capability ID (000Dh) (Downstream)															
Reserved (Upstream)																																F28h							
ACS Control (Downstream)																ACS Capability (Downstream)																							
Reserved (Upstream) Egress Control Vector (Downstream)																																F2Ch							

Register 11-208. F24h ACS Extended Capability Header (Downstream Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Note: Because this register is implemented as one physical register common to all Ports, the Upstream Port's register (which is Reserved) has the same value as the Downstream Ports' registers. However, in the Upstream Port, the ACS Extended Capability is excluded from the Linked List of PCI Express Extended Capabilities, and therefore, the Upstream Port's register is effectively hidden from system software and the non-zero value has no significant consequence.					
15:0	Reserved	Upstream	RsvdP	No	0000h
	PCI Express Extended Capability ID	Downstream	ROS	Yes	000Dh
19:16	Reserved	Upstream	RsvdP	No	0h
	Capability Version	Downstream	ROS	Yes	1h
31:20	Reserved	Upstream	RsvdP	No	000h
	Next Capability Offset Program to B70h, which addresses the Vendor-Specific Extended Capability 2 structure.	Downstream	ROS	Yes	B70h

**Register 11-209. F28h ACS Control and Capability
(Downstream Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
ACS Capability					
0	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress control.	Downstream	RO	Yes	1
6	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	<i>Reserved</i>		RsvdP	No	0
12:8	<i>Reserved</i>	Upstream	RsvdP	No	0
	Egress Control Vector Size Encodings 01h through FFh directly indicate the number of each Port's Egress Control Vector register <i>Peer-to-Peer Port x Control</i> bit (offset F2Ch[17:16, 9:8, 0]). <i>Note: The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.</i>	Downstream	HwInit	Yes	18h
15:13	<i>Reserved</i>		RsvdP	No	000b

**Register 11-209. F28h ACS Control and Capability
(Downstream Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
ACS Control					
16	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Source Validation Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Translation Blocking Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS P2P Request Redirect Enable Enables or disables ACS Peer-to-Peer Request redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect Enable Enables or disables ACS Peer-to-Peer Completion redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
20	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS P2P Egress Control Enable Enables or disables ACS Peer-to-Peer Egress control. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	<i>Reserved</i>	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable Enables or disables ACS Direct Translated Peer-to-Peer. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	<i>Reserved</i>		RsvdP	No	0-0h

**Register 11-210. F2Ch Egress Control Vector
(Downstream Ports)**

Bit(s)	Description	Downstream Port x	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Upstream Port bits are Reserved, RsvdP, not serial EEPROM nor I²C writable, and have a default value of 0.</p> <p>The Downstream Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name.</p> <p><i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.</p> <p>The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Peer-to-Peer Port x Control Valid when the ACS Control register <i>ACS P2P Egress Control Enable</i> bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	0	RW	Yes	0
5:1	Factory Test Only		RsvdP	No	0-0h
7:6	Reserved		RsvdP	No	00b
8	Peer-to-Peer Port x Control Valid when the ACS Control register <i>ACS P2P Egress Control Enable</i> bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	8	RW	Yes	0
9		9	RW	Yes	0
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Peer-to-Peer Port x Control Valid when the ACS Control register <i>ACS P2P Egress Control Enable</i> bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	16	RW	Yes	0
17		17	RW	Yes	0
21:18	Factory Test Only		RsvdP	No	0h
31:22	Reserved		RsvdP	No	0-0h

11.21 Device-Specific Registers (Offsets F30h – FB0h)

This section details the Device-Specific registers located at offsets F30h through FB0h. Device-Specific registers are unique to the PEX 8747 and not referenced in the *PCI Express Base r3.0*. [Table 11-39](#) defines the register map.

Other Device-Specific registers are detailed in:

- [Section 11.16, “Device-Specific Registers \(Offsets 1C0h – A74h\)”](#)
- [Section 11.18, “Device-Specific Registers \(Offsets B70h – DFCh\)”](#)

Note: It is recommended that these registers not be changed from their default values.

Table 11-39. Device-Specific Register Map (Offsets F30h – FB0h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Egress Control (Offsets F30h – F44h)		F30h ... F44h
Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)		F48h ... F6Ch
Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)		F70h ... FB0h

11.21.1 **Device-Specific Registers – Egress Control
(Offsets F30h – F44h)**

This section details the Device-Specific Egress Control registers. [Table 11-40](#) defines the register map.

**Table 11-40. Device-Specific Egress Control Register Map
(All Ports)**

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Egress Control and Status	F30h
Reserved	F34h
Port Egress TLP Threshold	F38h
Reserved	F3Ch – F40h
Factory Test Only	F44h

**Register 11-211. F30h Egress Control and Status
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. For bits [12:9] – The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.					
1:0	Reserved		RsvdP	No	00b
5:2	Factory Test Only		RWS	Yes	0-0h
6	Factory Test Only		RWS	Yes	0
7	Ex Tag 8 Bit Exerciser Tag is 8 bits	0, 8, 16	RWS	Yes	0
8	Rdr Hdr Prefetch Disable 0 = Prefetch Headers on this Port 1 = Do not prefetch Headers on this Port		RWS	Yes	0
9	Vendor-Defined Type 0 UR 0 = Do not generate UR Vendor-Defined Type 0 Broadcast TLP in the <i>DL_Down</i> state 1 = Generate UR Vendor-Defined Type 0 Broadcast TLP in the <i>DL_Down</i> state	0, 8, 16	RWS	Yes	0
10	Egress Credit Timeout Enable 0 = Egress Credit Timeout mechanism is disabled. 1 = Egress Credit Timeout mechanism is enabled. The timeout period is selected in field [12:11] (<i>Egress Credit Timeout Value</i>). Status is reflected in bit 16 (<i>Egress Credit Timeout Status</i>). If the Egress Credit Timer is enabled and expires (due to lack of Flow Control credits from the connected device), the Port brings down its Link. This event generates a Surprise Down Uncorrectable error, for Downstream Ports. For Upstream Port Egress Credit Timeout, the connected Upstream device detects the Surprise Down event.	0, 8, 16	RWS	Yes	0
12:11	Egress Credit Timeout Value 00b = 1 ms 01b = 512 ms 10b = 1 s 11b = Reserved	0, 8, 16	RWS	Yes	00b
15:13	Reserved		RsvdP	No	000b

**Register 11-211. F30h Egress Control and Status
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
16	Egress Credit Timeout Status 0 = No timeout 1 = Timeout		RW1CS	No	0
18:17	Egress Credit Timeout VC&T Egress Credit timeout for Virtual Channel and Type. 00b = Posted 01b = Non-Posted 10b = Completion 11b = <i>Reserved</i>		ROS	No	00b
30:19	<i>Reserved</i>		RsvdP	No	0-0h
31	Port Activity 0 = Port is idle 1 = Port has one or more pending TLPs to transmit		ROS	No	0

**Register 11-212. F38h Port Egress TLP Threshold
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<i>Note: Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and enabling both concurrently can result in Fatal errors.</i>					
11:0	Port Lower TLP Counter When Source Scheduling is disabled due to Threshold, it is re-enabled when the Port TLP Counter goes below this Threshold value.	Upstream	RWS	Yes	003h
		Downstream	RWS	Yes	FFFh
15:12	<i>Reserved</i>		RsvdP	No	0h
27:16	Port Upper TLP Counter When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP scheduling to this egress Port.	Upstream	RWS	Yes	006h
		Downstream	RWS	Yes	FFFh
31:28	<i>Reserved</i>		RsvdP	No	0h

11.21.2 Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)

This section details the Device-Specific Ingress Control and Port Enable registers, which also include the **Negotiated Link Width** registers. Table 11-41 defines the register map.

Table 11-41. Device-Specific Ingress Control and Port Enable Register Map (Ports^a)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																																
Ingress Port-Based Control																																F48h
Port Enable Status																																F4Ch
Reserved								Negotiated Link Width for Ports 0																								F50h
Reserved								Factory Test Only																Negotiated Link Width for Ports 8, 9								F54h
Reserved								Factory Test Only																Negotiated Link Width for Ports 16, 17								F58h
Minimum/Maximum Status																																F5Ch
Ingress Control																				Factory Test Only/ Reserved/Not Used												F60h
Reserved																																F64h – F6Ch

a. Certain registers are Port-specific, others are Station-specific or Chip-specific; all are Device-specific.

Register 11-213. F48h Ingress Port-Based Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
1:0	ACK TLP Counter Timeout Sets the quantity of ingress TLP Acknowledges (ACKs) pending, which causes a high-priority ACK to be sent. 00b = 16 TLPs 01b = 8 TLPs 10b = 4 TLPs 11b = Feature is disabled	RWS	Yes	00b
31:2	Reserved	RsvdP	No	0-0h

Register 11-214. F4Ch Port Enable Status (Upstream Port)

Bit(s)	Description	Upstream Port x	Type	Serial EEPROM and I ² C	Default
<p>The value of this register depends upon the Port configuration for each Station – Station 0 (bit 0), Station 1 (bits [9:8]), and Station 2 (bits [17:16]). When a Port is enabled in the corresponding Station configuration, the bit for that Port is Set; otherwise, the bit is Cleared.</p> <p>Notes: The Downstream Port bits are Reserved, RsvdP, not serial EEPROM nor I²C writable, and have a default value of 0.</p> <p>The Upstream Port x column is provided to indicate the Port Number associated with bits/fields that include “Port x” in their name.</p> <p><i>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations and Ports.</i></p>					
0	Port x Enable Status 0 = Port is disabled 1 = Port is enabled	0	RO	No	1
5:1	Factory Test Only		RsvdP	No	0-0h
7:6	Reserved		RsvdP	No	00b
8	Port x Enable Status 0 = Port is disabled 1 = Port is enabled	8	RO	No	Defined by STRAP_STN1_PORTCFG0 input state, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station 1</i> field (Port 0, offset 300h[5:3])
9		9	RO	No	
13:10	Factory Test Only		RsvdP	No	0h
15:14	Reserved		RsvdP	No	00b
16	Port x Enable Status 0 = Port is disabled 1 = Port is enabled	16	RO	No	Defined by STRAP_STN2_PORTCFG0 input state, or programmed by serial EEPROM value for the Port Configuration register <i>Port Configuration for Station 2</i> field (Port 0, offset 300h[8:6])
17		17	RO	No	
21:18	Factory Test Only		RsvdP	No	0h
31:22	Reserved		RsvdP	No	0-0h

Register 11-215. F50h Negotiated Link Width for Ports 0 (Upstream Port)

Bit(s)	Description	Upstream Port <i>x</i>	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Downstream Port bits are Reserved, RsvdP, not serial EEPROM nor I²C writable, and have a default value of 0. The Upstream Port <i>x</i> column is provided to indicate the Port Number associated with bits/fields that include “Port <i>x</i>” in their name.</p> <p><i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p>					
3:0	<p>Negotiated Link Width and Link Speed Encoding for Port <i>x</i></p> <p>Remainder of value divided by 5 indicates the negotiated Link width. If the Link is Down, the value is 0h.</p> <p>0h = x1, or the Port is in the <i>DL_Down</i> state 1h = x2 2h = x4 3h = x8 4h = x16</p> <p>Quotient of division indicates the Link speed.</p> <p>0h = Gen 1 (2.5 GT/s) 1h = Gen 2 (5.0 GT/s) 2h = Gen 3 (8.0 GT/s)</p> <p>All other encodings are Reserved.</p>	0	RO	No	PCFG
23:4	Factory Test Only		RsvdP	No	00_000h
31:24	Reserved		RsvdP	No	00h

Register 11-216. F54h Negotiated Link Width for Ports 8, 9 (Upstream Port)

Bit(s)	Description	Upstream Port <i>x</i>	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Downstream Port bits are Reserved, RsvdP, not serial EEPROM nor I²C writable, and have a default value of 0.</p> <p>The Upstream Port <i>x</i> column is provided to indicate the Port Number associated with bits/fields that include “Port <i>x</i>” in their name.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p>					
3:0	Negotiated Link Width and Link Speed Encoding for Port <i>x</i> Remainder of value divided by 5 indicates the negotiated Link width. If the Link is Down, the value is 0h. 0h = x1, or the Port is in the <i>DL_Down</i> state 1h = x2 2h = x4 3h = x8 4h = x16	8	RO	No	PCFG
7:4	Quotient of division indicates the Link speed. 0h = Gen 1 (2.5 GT/s) 1h = Gen 2 (5.0 GT/s) 2h = Gen 3 (8.0 GT/s) All other encodings are Reserved .	9	RO	No	
23:8	Factory Test Only		RsvdP	No	0000h
31:24	Reserved		RsvdP	No	00h

Register 11-217. F58h Negotiated Link Width for Ports 16, 17 (Upstream Port)

Bit(s)	Description	Upstream Port <i>x</i>	Type	Serial EEPROM and I ² C	Default
<p>Notes: The Downstream Port bits are Reserved, RsvdP, not serial EEPROM nor I²C writable, and have a default value of 0.</p> <p>The Upstream Port <i>x</i> column is provided to indicate the Port Number associated with bits/fields that include “Port <i>x</i>” in their name.</p> <p><i>Table 11-5</i> indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, Ports, SerDes modules, and Lanes.</p>					
3:0	Negotiated Link Width and Link Speed Encoding for Port <i>x</i> Remainder of value divided by 5 indicates the negotiated Link width. If the Link is Down, the value is 0h. 0h = x1, or the Port is in the <i>DL_Down</i> state 1h = x2 2h = x4 3h = x8 4h = x16	16	RO	No	PCFG
7:4	Quotient of division indicates the Link speed. 0h = Gen 1 (2.5 GT/s) 1h = Gen 2 (5.0 GT/s) 2h = Gen 3 (8.0 GT/s) All other encodings are Reserved .	17	RO	No	
23:8	Factory Test Only		RsvdP	No	0000h
31:24	Reserved		RsvdP	No	00h

Register 11-218. F5Ch Minimum/Maximum Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
15:0	Minimum Cut-Thru Value Bits [15:13] are tied to 000b.	RO	No	1FFFh
31:16	Maximum Cut-Thru Value Bits [31:29] are tied to 000b.	RO	No	0000h

**Register 11-219. F60h Ingress Control
(Upstream Port)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
3:0	<i>Factory Test Only</i>	RWS	Yes	2h
5:4	<i>Not used</i>	RWS	Yes	00b
6	<i>Reserved</i>	RsvdP	No	0
7	<i>Not used</i>	RsvdP	No	0
8	Drop ECRC TLPs Drop End-to-end Cyclic Redundancy Check (ECRC) TLPs. 1 = ECRC TLP was dropped	RWS	Yes	0
9	Drop Poisoned TLPs 0 = Nullify (invert Link Cyclic Redundancy Check (LCRC), add EDB) and forward any TLPs received as Poisoned. 1 = Discard Poisoned TLPs <i>Note:</i> The PEX 8747 never Sets the EP bit in the TLP Header. If a TLP is received with its EP bit Set (indicating Poisoned), the Port Sets its Detected Parity Error bit(s) (PCI Status register Detected Parity Error bit (offset 04h[31]) on the primary side, and/or Secondary Status register Detected Parity Error bit (offset 1Ch[31]) on the secondary side).	RWS	Yes	0
10	<i>Factory Test Only</i>	RWS	Yes	0
12:11	<i>Not used</i>	RWS	Yes	00b
14:13	<i>Factory Test Only</i>	RWS	Yes	00b
15	<i>Reserved</i>	RsvdP	No	0
23:16	<i>Not used</i>	RWS	Yes	00h

Register 11-219. F60h Ingress Control (Upstream Port) (Cont.)

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
24	<i>Reserved</i>	RsvdP	No	0
25	<i>Factory Test Only</i>	RWS	Yes	0
26	Disable Upstream Port BAR0 and BAR1 0 = Enables the Upstream Port Base Address 0 and Base Address 1 registers (BAR0 and BAR1 , Upstream Port, offsets 10h and 14h , respectively) 1 = Disables the Upstream Port BAR0 and BAR1	RWS	Yes	0
27	Flag Unexpected Completion Error 0 = Flag unexpected Completion errors for Completions that hit the PEX 8747's internal virtual PCI Bus space 1 = Silently unexpected Completion errors for Completions that hit the PEX 8747's internal virtual PCI Bus space	RWS	Yes	0
28	Disable VGA BIOS Memory Access Decoding 0 = Enables the Bridge Control register <i>VGA 16-Bit Decode Enable</i> , <i>VGA Enable</i> , and <i>ISA Enable</i> bits (offset 3Ch[20:18], respectively), and enables decoding of PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are blocked) 1 = Disables the Bridge Control register <i>VGA 16-Bit Decode Enable</i> , <i>VGA Enable</i> , and <i>ISA Enable</i> bits (offset 3Ch[20:18], respectively), and disables decoding of PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are <i>not</i> blocked)	RWS	Yes	1
30:29	<i>Factory Test Only</i>	RWS	Yes	00b
31	<i>Not used</i>	RWS	Yes	0

11.21.3 Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)

This section details the Device-Specific Error Checking and Debug registers located at offsets F70h through FB0h. [Table 11-42](#) defines the register map.

Other Device-Specific Error Checking and Debug registers are detailed in [Section 11.16.11](#), “Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch).”

Table 11-42. Device-Specific Error Checking and Debug Register Map (Offsets F70h – FB0h) (All Ports)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Power Management Hot Plug User Configuration																F70h															
Reserved																F74h – FA4h															
ACK Transmission Latency Limit																FA8h															
Bad TLP Count																FACh															
Bad DLLP Count																FB0h															

**Register 11-220. F70h Power Management Hot Plug User Configuration
(All Ports)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
0	L0s Entry Idle Count Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 μ s 1 = Idle condition must last 4 μ s		RWS	Yes	0
1	Factory Test Only		RWS	Yes	0
2	Not enabled Functionality associated with this bit is enabled only on Downstream Ports.	Upstream	RWS	Yes	0
	HPC PME Turn-Off Enable 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a Downstream Port	Downstream	RWS	Yes	0
7:3	Factory Test Only		RWS	Yes	0-0h
8	DLLP Timeout Link Retrain Disable Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 μ s. 0 = Enables Link retraining when no DLLPs are received for more than 256 μ s (default) 1 = DLLP Timeout is disabled		RWS	Yes	0
9	Factory Test Only		RWS	Yes	0
10	L0s Entry Disable 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met		RWS	Yes	0
11	Factory Test Only		RWS	Yes	0
12	Software-Controlled Hot Plug Enable 1 = Hot Plug input functionality is disabled and software controls the input functionality		RWS	Yes	0
26:13	Reserved		RsvdP	No	0-0h
27	Software Present Detect State Value Presence Detect state (Port's Slot Status register <i>Presence Detect State</i> bit (Downstream Ports, offset 80h[22])) value is programmed from this register when bit 12 (<i>Software-Controlled Hot Plug Enable</i>) is Set.		RWS	Yes	0
28	Reserved		RsvdP	No	0
29	PHY Upstream Port Control Write Enable 1 = Enables the following bits to be functional on Upstream Port: <ul style="list-style-type: none"> Link Control register <i>Link Disable</i> bit (offset 78h[4]) Link Control register <i>Retrain Link</i> bit (offset 78h[5]) Link Control 2 register <i>Target Link Speed</i> field (offset 98h[3:0]) 		RWS	Yes	0
31:30	Factory Test Only		RWS	Yes	00b

**Register 11-221. FA8h ACK Transmission Latency Limit
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
The value of this register should be valid after Link negotiation.				
11:0	ACK Transmission Latency Limit Acknowledge Control Packet (ACK) Transmission Latency Limit. The value of this field changes, based upon the Port's Negotiated Link Width (offset 78h[25:20]), Current Link Speed (offset 78h[19:16]) after the Link is Up, and Maximum Payload Size (offset 70h[7:5]). x1 = 255d x2 = 217d x4 = 118d x8 = 107d (Station 1 and Station 2 only) x16 = 100d	RWS	Yes	Defined by STRAP_STNx_PORTCFG0 input states
15:12	Reserved	RsvdP	No	0h
23:16	Upper 8 Bits of the Replay Timer Limit If the serial EEPROM is not present, the value of this register changes based upon the negotiated Link width after the Link is Up. The value in this field is a multiplier of the default internal timer values that are compliant to the <i>PCI Express Base r3.0</i> . These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	Reserved	RsvdP	No	00h
31	ACK Transmission Latency Timer Status Indicates the written status of field [11:0] (<i>ACK Transmission Latency Limit</i>). After the register is written, either by software and/or serial EEPROM, this bit is Set and Cleared only by a Fundamental Reset.	RO	No	0

**Register 11-222. FACH Bad TLP Count
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	Bad TLP Count Counts the quantity of TLPs received with bad LCRC, or quantity of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

**Register 11-223. FB0h Bad DLLP Count
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	Bad DLLP Count Counts the quantity of DLLPs received with bad LCRC, or quantity of DLLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

11.22 Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

This section details the Advanced Error Reporting Extended Capability registers. [Table 11-43](#) defines the register map.

Table 11-43. Advanced Error Reporting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16																15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0																				
Next Capability Offset (138h or 148h)																Capability Version (1h)				PCI Express Extended Capability ID (0001h)																FB4h
Uncorrectable Error Status																																FB8h				
Uncorrectable Error Mask																																FBCh				
Uncorrectable Error Severity																																FC0h				
<i>Reserved</i>																Correctable Error Status																FC4h				
<i>Reserved</i>																Correctable Error Mask																FC8h				
Advanced Error Capabilities and Control																																FCCh				
Header Log 0																																FD0h				
Header Log 1																																FD4h				
Header Log 2																																FD8h				
Header Log 3																																FDCCh				

Register 11-224. FB4h Advanced Error Reporting Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
15:0	PCI Express Extended Capability ID		ROS	Yes	0001h
19:16	Capability Version		ROS	Yes	1h
31:20	Next Capability Offset Program to 138h, which addresses the Upstream Port Power Budget Extended Capability structure.	Upstream	ROS	Yes	138h
	Program to 148h, which addresses the Virtual Channel Extended Capability structure.	Downstream	ROS	Yes	148h

Register 11-225. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Notes: If an individual error is masked (corresponding bit in the Uncorrectable Error Mask register (offset FBCh) is Set) when the error is detected, its Error Status bit is still updated; however, an error reporting Message (ERR_FATAL or ERR_NONFATAL) is not sent to the Root Complex, and the Advanced Error Capabilities and Control register First Error Pointer field (offset FCCh[4:0]) and Header Log x registers (offsets FD0h through FDCh) remain unchanged.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>For bit 22 – The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
3:0	Reserved		RsvdP	No	0h
4	Data Link Protocol Error Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
5	Reserved	Upstream	RsvdP	No	0
	Surprise Down Error Status 0 = No error is detected 1 = Error is detected	Downstream	RW1CS ^a	Yes	0
11:6	Reserved		RsvdP	No	0-0h
12	Poisoned TLP Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
13	Flow Control Protocol Error Status Reserved/Not supported		RsvdP	No	0
14	Completion Timeout Status Not applicable to switches.		RsvdP	No	0
15	Completer Abort Status		RW1CS ^a	Yes	0
16	Unexpected Completion Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
17	Receiver Overflow Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
18	Malformed TLP Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
19	ECRC Error Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0

**Register 11-225. FB8h Uncorrectable Error Status
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
20	Unsupported Request Error Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
21	Reserved	Upstream	RsvdP	No	0
	ACS Violation Error Status 0 = No violation is detected 1 = Violation is detected	Downstream	RW1CS ^a	Yes	0
22	Uncorrectable Internal Error Status 0 = No error is detected 1 = Error is detected	0, 8, 16	RW1CS ^a	Yes	0
	Reserved	Otherwise	RsvdP	No	0
23	MC Blocked TLP Status Multicast blocked TLP status. 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
24	Atomic Operation Egress Blocked Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
31:25	Reserved		RsvdP	No	0-0h

- a. When the **ECC Error Check Disable** register *Software Force Error Enable* bit (Downstream Ports, offset 720h[2]) is Set, Type changes from RW1CS to RW.

Register 11-226. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Notes: The bits in this register can be used to mask their respective Uncorrectable Error Status register bits (offset FB8h). Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>For bit 22 – The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
3:0	Reserved		RsvdP	No	0h
4	Data Link Protocol Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
5	Reserved	Upstream	RsvdP	No	0
	Surprise Down Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
11:6	Reserved		RsvdP	No	0-0h
12	Poisoned TLP Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
13	Flow Control Protocol Error Mask Reserved/Not supported		RsvdP	No	0
14	Completion Timeout Mask Not applicable to switches.		RsvdP	No	0
15	Completer Abort Mask		RWS	Yes	0

**Register 11-226. FBCh Uncorrectable Error Mask
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
16	Unexpected Completion Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
17	Receiver Overflow Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
18	Malformed TLP Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
19	ECRC Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
20	Unsupported Request Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
21	Reserved	Upstream	RsvdP	No	0
	ACS Violation Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
22	Uncorrectable Internal Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	0, 8, 16	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
23	MC Blocked TLP Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
24	Atomic Operation Egress Blocked Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
31:25	Reserved		RsvdP	No	0-0h

Register 11-227. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
Notes: Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports. For bit 22 – The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.					
3:0	Reserved		RsvdP	No	0h
4	Data Link Protocol Error Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
5	Surprise Down Error Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal	Upstream	ROS	No	1
		Downstream	RWS	Yes	1
11:6	Reserved		RsvdP	No	0-0h
12	Poisoned TLP Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
13	Flow Control Protocol Error Severity Reserved/Not supported		RO	No	1
14	Completion Timeout Severity Not applicable to switches. Because the Status and Mask are both Reserved for this bit, Severity can be ignored.		RsvdP	No	0
15	Completer Abort Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
16	Unexpected Completion Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
17	Receiver Overflow Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
18	Malformed TLP Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
19	ECRC Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0

**Register 11-227. FC0h Uncorrectable Error Severity
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
20	Unsupported Request Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
21	<i>Reserved</i>	Upstream	RsvdP	Yes	0
	ACS Violation Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	Downstream	RWS	Yes	0
22	Uncorrectable Internal Error Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal	0, 8, 16	RWS	Yes	1
	<i>Reserved</i>	Otherwise	RsvdP	No	1
23	MC Blocked TLP Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	0
24	Atomic Operation Egress Blocked Severity 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	0
31:25	<i>Reserved</i>		RsvdP	No	0-0h

Register 11-228. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Notes: If an individual error is masked (corresponding bit in the Correctable Error Mask register (offset FC8h) is Set) when the error is detected, its Error Status bit is still updated; however, an error reporting Message (ERR_COR) is not sent to the Root Complex.</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>For bit 14 – The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Receiver Error Status Indicates that one or more of the following Receiver errors was detected: <ul style="list-style-type: none"> • Code (symbol) error • Disparity error • Elastic Buffer overflow/underflow • Gen 3 Framing error 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
5:1	Reserved		RsvdP	No	0-0h
6	Bad TLP Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
7	Bad DLLP Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
8	REPLAY NUM Rollover Status Replay Number Rollover status. 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
11:9	Reserved		RsvdP	No	000b

**Register 11-228. FC4h Correctable Error Status
(All Ports) (Cont.)**

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
12	Replay Timer Timeout Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
13	Advisory Non-Fatal Error Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
14	Corrected Internal Error Status 0 = No error is detected 1 = Error is detected	0, 8, 16	RW1CS ^a	Yes	0
	<i>Reserved</i>	Otherwise	RsvdP	No	0
15	Header Log Overflow Status 0 = No error is detected 1 = Error is detected		RW1CS ^a	Yes	0
31:16	<i>Reserved</i>		RsvdP	No	0000h

- a. When the **ECC Error Check Disable** register *Software Force Error Enable* bit (Downstream Ports, offset 720h[2]) is Set, Type changes from RW1CS to RW.

Register 11-229. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I ² C	Default
<p>Notes: The bits in this register can be used to mask their respective Correctable Error Status register bits (offset FC4h).</p> <p>Table 11-5 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming. The table also lists the relationship between the Stations, Station Ports, and Ports.</p> <p>For bit 14 – The Port 0 bit is for Port 0. The Port 8 bits are for Ports 8 and 9. The Port 16 bits are for Ports 16 and 17.</p>					
0	Receiver Error Mask 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
5:1	Reserved		RsvdP	No	0-0h
6	Bad TLP Mask 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
7	Bad DLLP Mask 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
8	REPLAY NUM Rollover Mask Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
11:9	Reserved		RsvdP	No	000b
12	Replay Timer Timeout Mask 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	0
13	Advisory Non-Fatal Error Mask 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	1
14	Corrected Internal Error Mask 0 = Error reporting is not masked 1 = Error reporting is masked	0, 8, 16	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
15	Header Log Overflow Mask 0 = Error reporting is not masked 1 = Error reporting is masked		RWS	Yes	1
31:16	Reserved		RsvdP	No	0000h

**Register 11-230. FCCh Advanced Error Capabilities and Control
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
4:0	First Error Pointer Identifies the bit position of the first error reported in the Uncorrectable Error Status register (offset FB8h).	ROS	No	1Fh
5	ECRC Generation Capable 0 = ECRC generation is not supported 1 = ECRC generation is supported, but must be enabled	ROS	Yes	1
6	ECRC Generation Enable 0 = ECRC generation is disabled 1 = ECRC generation is enabled	RWS	Yes	0
7	ECRC Check Capable 0 = ECRC checking is not supported 1 = ECRC checking is supported, but must be enabled	ROS	Yes	1
8	ECRC Check Enable 0 = ECRC checking is disabled 1 = ECRC checking is enabled	RWS	Yes	0
31:9	Reserved	RsvdP	No	0-0h

**Register 11-231. FD0h Header Log 0
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	TLP Header 0 First DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

**Register 11-232. FD4h Header Log 1
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	TLP Header 1 Second DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

**Register 11-233. FD8h Header Log 2
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	TLP Header 2 Third DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

**Register 11-234. FDCh Header Log 3
(All Ports)**

Bit(s)	Description	Type	Serial EEPROM and I ² C	Default
31:0	TLP Header 3 Fourth DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

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Chapter 12 Test and Debug

12.1 Introduction

This chapter describes the following test- and debug-related information:

- [Physical Layer Loopback Operation](#)
- [Built-In Self-Test](#)
- [Using the SerDes Quad x Diagnostic Data Registers](#)
- [PHY Testability Features](#)
- [JTAG Interface](#)
- [Port Good Status LEDs](#)
- [Thermal Sensor Diode – 27 x 27 mm² Package](#)

12.2 Physical Layer Loopback Operation

12.2.1 Overview

Physical Layer (PHY) Loopback functions are used to test the SerDes in the PEX 8747, connections between devices, and SerDes of external devices, as well as various PEX 8747 and external digital logic. The PEX 8747 supports five types of Loopback operations, as described in [Table 12-1](#). Additional information regarding each type is provided in the sections that follow.

[Figure 12-1](#) illustrates the Physical Media Attachment Layer (PMA) and Physical Coding Sublayer (PCS) Loopback paths. [Table 12-2](#) provides additional Loopback information.

Table 12-1. Loopback Operations

Operation	Description
Internal Loopback Mode (LB_NES)	This mode connects the SerDes serial Tx output to the serial Rx input. The PRBS generator can be used to create a pseudo-random data pattern that is transmitted and returned to the PRBS checker.
Analog Loopback Master Mode	This mode depends upon an external device or passive connection (<i>such as</i> a cable) to loopback the transmitted data to the PEX 8747, without SKIP Ordered-Set clock compensation. If an external device is used, it must not include its Elastic buffer in the Slave Loopback data path, because no SKIP Ordered-Sets are transmitted. The PRBS generator and checker should be used to create and check the data pattern.
Digital Loopback Master Mode	This mode also depends upon an external device to loopback the transmitted data. This method is best used with an external device that includes at least its Elastic buffer in the Loopback data path. The PEX 8747 provides a user-definable Test Pattern generator and checker that inserts SKIP Ordered-Sets at the proper intervals.
Analog Loopback Slave Mode (LB_FEP)	The PEX 8747 enters this mode when an external device transmits Training Sets with the <i>Loopback Training Control Bit Set</i> and the Physical Layer Test 0 register Analog Loopback Enable bit (Port 0, 8, or 16, offset 224h[10]) is Set. The PEX 8747 automatically performs the necessary sequence of AHB register Writes, to enable this Loopback data path.
Digital Loopback Slave Mode (LB_PIPE)	<p>The PEX 8747 enters this mode when the following conditions are met:</p> <ul style="list-style-type: none"> • Physical Layer Test 0 register <i>Analog Loopback Enable</i> bit (Port 0, 8, or 16, offset 224h[10]) is Cleared, and • External device transmits Training Sets with the <i>Loopback Training Control Bit Set</i>, –or– • Port's Physical Layer Test 1 register <i>Port x Parallel Loopback Path Enable</i> bit (Port 0, 8, or 16, offset 228h[17:16]) is Set <p>This loopback path includes the Elastic buffer and 8b/10b (Gen 1 and Gen 2 Link speeds) or 128b/130b (Gen 3 Link speed) encode/decode.</p>

Figure 12-1. PMA and PCS Loopback Paths

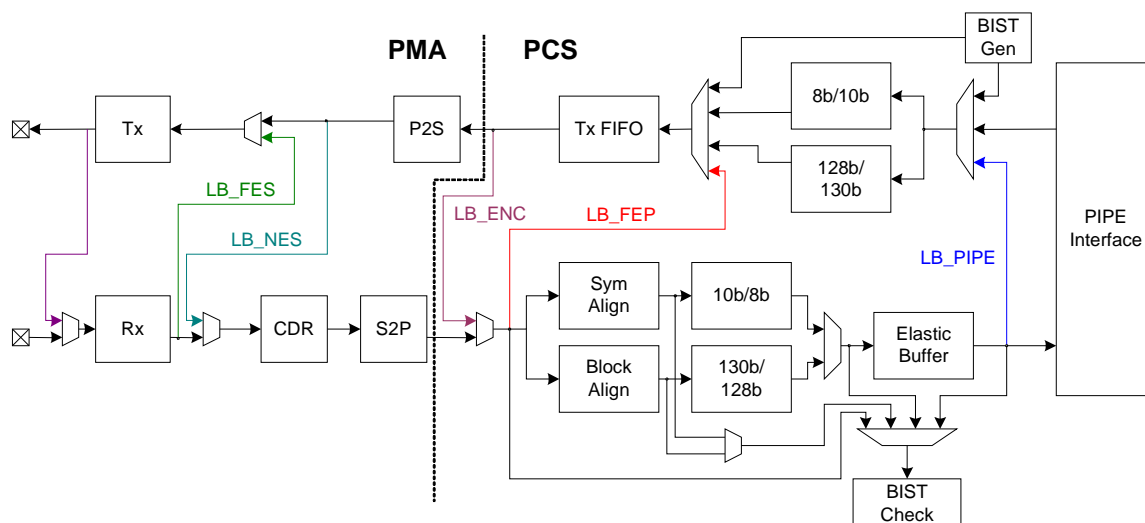


Table 12-2. Loopback

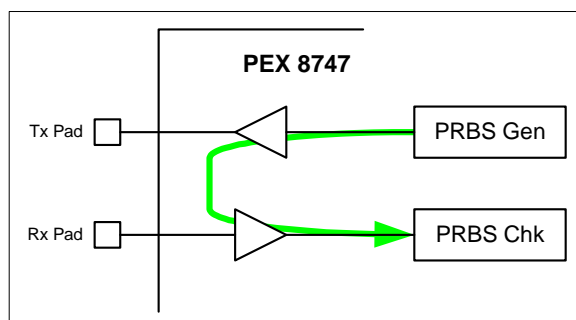
Loopback Name	Loopback Description	AHB Register/PIPE Control	Loopback Direction	Notes
LB_NES	Near-End Serial Loopback	Lane R3[6] = 1 (nes_lb_ena)	Tx -> Rx	Only runs up to 5 GT/s
LB_FES	Far-End Serial Loopback	Lane R1[6] = 1 (fes_lb_ena)	Rx-> Tx	Only runs up to 5 GT/s
LB_ENC	Encoder Loopback	Lane R0[2] = 1 (rx_src) Lane R0[1] = 0 (rx_clk_src)	Tx -> Rx	Requires reset.
LB_FEP	Far-End Parallel Loopback	Lane R1[6:4] = 110b (dmux_txbsel[2:0]) Lane R3[7] = 1 (rxclk_lb_ena) Lane R2[7] = 1 (cktrans_en)	Rx -> Tx	Requires reset and sequencing. Tx FIFO Write clock becomes recovered byte block.
LB_PIPE	PIPE-compliant loopback. Used when the PEX 8747 is a PCI Express Loopback Slave.	Lane R0[7:6] = 01b (dmux_txasel[1:0]) or TxDetRxLpbk && PowerDown = P0	Rx -> Tx	Automatically selected when LTSSM enters LB_ActSlv state.

12.2.2 Internal Loopback Mode (LB_NES)

Figure 12-2 illustrates the Loopback data path when Internal Loopback mode is enabled. The only items in the data path are the SerDes. This Loopback mode is used when the SerDes BIST (Built-in Self Test) is enabled.

SerDes BIST is intended to be overlapped with the serial EEPROM load operation. To achieve this overlap, the **Physical Layer Test 0** register *Factory Test Only* bit (Port 0, 8, or 16, offset 224h[11]) is written early in the serial EEPROM load operation. After the bit is Set, the SerDes are placed into Loopback mode, and the PRBS generator is started. The BIST is run for 15 ms, if an error is detected on any of the SerDes, the BIST_ERROR pin associated with the Station that includes the SerDes in error is asserted. While the SerDes BIST is in progress, the PRBS test data is present on the external PEX_PER/ PETp/nx balls. The continuing serial EEPROM register load has no effect on SerDes BIST.

Figure 12-2. Internal Loop Back (Analog Near End) Data Path



12.2.3 Analog Loopback Master Mode

Analog Loopback Master mode is typically used for Analog Far-End testing (refer to [Figure 12-3](#)), with a shallow Loopback path Slave device, to determine overall Bit Error rates. However, it can also be used to recreate the BIST described in [Section 12.2.2](#), by looping back the data with a cable. Looping back with a cable includes the internal circuitry, package connections to bond pads, package balls, board traces, and any connectors that might be in the test data path, as illustrated in [Figure 12-4](#). A PRBS pattern is typically used for this mode, because it is appropriate for bit error rate testing. A User Test Pattern (UTP) is *not* recommended for this application.

Figure 12-3. Analog Far-End Loopback

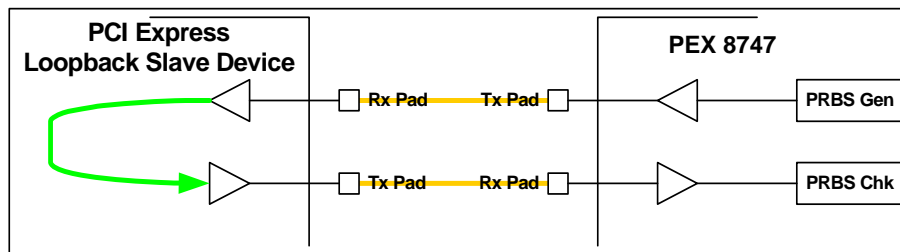
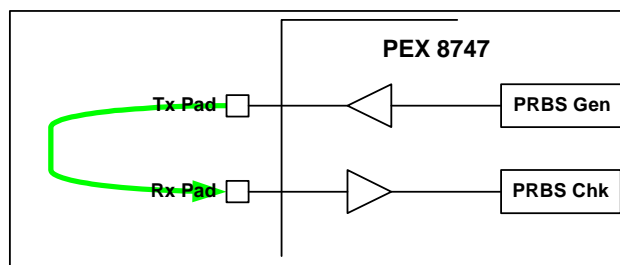


Figure 12-4. Cable Loopback



To cause a PEX 8747 Port to request to become a Loopback Master, the following must occur: After the Link is Up, a Configuration Write to the Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Port 0, 8, or 16, offset 230h[0 or 4]) causes the Port to transition from the L0 Link PM state to the *Recovery* state, and then to the *Loopback* state. If a cable is used for the Loopback, the Port transitions from the *Configuration* state to the *Loopback* state. The cable should be connected only after the Upstream Link is Up and Configuration Writes are possible. If the cable is connected before the Upstream device is able to Set the *Port x Loopback Command* bit, the Link with the cable can reach the L0 Link PM state and *not* go to the *Loopback* state. In this case, the Port must be forced to the *Recovery* state, by asserting the Port's **Link Control** register *Retrain Link* bit (Downstream Ports, offset 78h[5]). The cable length is limited only by the PCI Express drivers and cable properties.

After the Port is in the *Loopback* state the Port's **Physical Layer Port Command** register *Port x Ready as Loopback Master* bit (Port 0, 8, or 16, offset 230h[3 or 7]) is Set. At this time, the user can enable the PRBS engine, by Setting the *PRBS Enable* bit that is associated with the SerDes assigned to the Port being tested. The PRBS checker checks the returned PRBS data. Any errors are logged in the **SerDes Quad x Diagnostic Data** register (Port 0, 8, or 16, offsets 238h through 244h) that corresponds to the SerDes quad being tested.

12.2.4 Digital Loopback Master Mode

The only difference between Analog and Digital Loopback Master modes is that the external device is assumed to have some of its digital logic in the Loopback data path. Because this includes the Elastic buffer, SKIP Ordered-Sets must be included in the test data pattern, which precludes use of the PRBS engine.

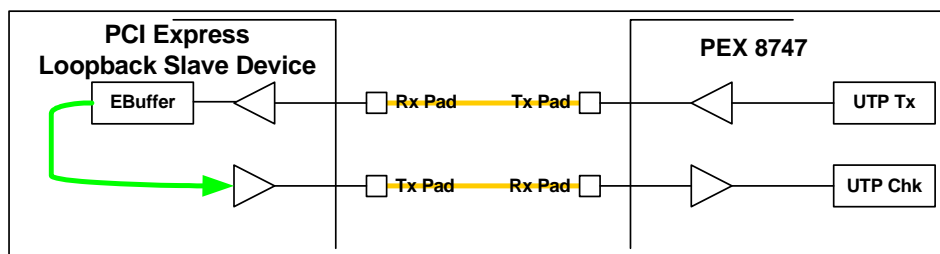
Figure 12-5 illustrates a Far-End Digital Loopback Master connection and data path.

The PEX 8747 provides the User Data Pattern Transmitter for Digital Far-End Loopback testing. After the Loopback Master mode is established, Configuration Writes are used to fill the Test Data Pattern registers. One or more **Physical Layer Test 1** register *SerDes Quad x Pair x User Test Pattern Enable* bits (Port 0, 8, or 16, offset 228h[31:24]) is Set, which starts the transmission of the User Data Pattern on all Lanes. If the Port's *Enable by Port* bit is also Set, the test pattern is transmitted on all Lanes of the corresponding Port, regardless of its Link width. If the *Enable by Port* bit is Cleared, the test pattern is transmitted only on the Lanes of the corresponding SerDes quad. SKIP Ordered-Sets are inserted at the interval determined by the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval in Blocks* or *SKIP Ordered-Set Interval in Clocks* field (Port 0, 8, or 16, offset 234h[27:16 or 11:0], respectively) value, at the nearest data pattern boundary:

- **Gen 3 (8.0 GT/s)** – Field [27:16]. Default interval is 371 block times.
- **Gen 1 and Gen 2 (2.5 and 5.0 GT/s, respectively)** – Field [11:0]. Default interval is 1,180 symbol times.

The Test Pattern checker ignores SKIP Ordered-Sets that are returned by the Loopback Slave, because the quantity of SKIP symbols received can be different than the quantity transmitted. All other data is compared to the transmitted data. Any errors are logged in the **SerDes Quad x Diagnostic Data** register (Port 0, 8, or 16, offsets 238h through 244h) that corresponds to the SerDes quad being tested.

Figure 12-5. Digital Far-End Loopback

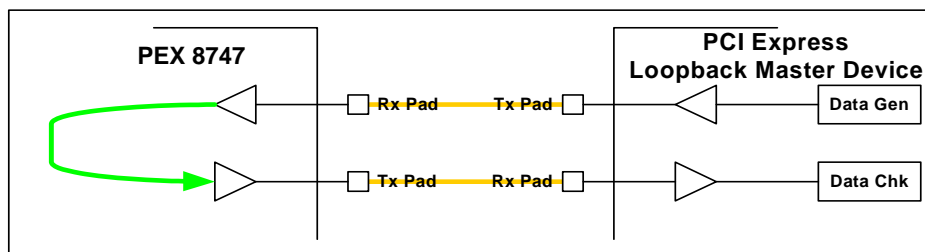


12.2.5 Analog Loopback Slave Mode (LB_FEP)

The PEX 8747 becomes an Analog Loopback Slave (as illustrated in [Figure 12-6](#)) if it receives Training Sets with the *Loopback* Training Control Bit Set while the **Physical Layer Test 0** register *Analog Loopback Enable* bit (Port 0, 8, or 16, offset 224h[10]) is Set.

While an Analog Loopback Slave, the PEX 8747 includes only the SerDes in the Loopback data path. The Loopback Master must provide the test data pattern and data pattern checking. It is not necessary for the Loopback Master to include SKIP Ordered-Sets in the data pattern.

Figure 12-6. Analog Loopback Slave Mode



12.2.6 Digital Loopback Slave Mode (LB_PIPE)

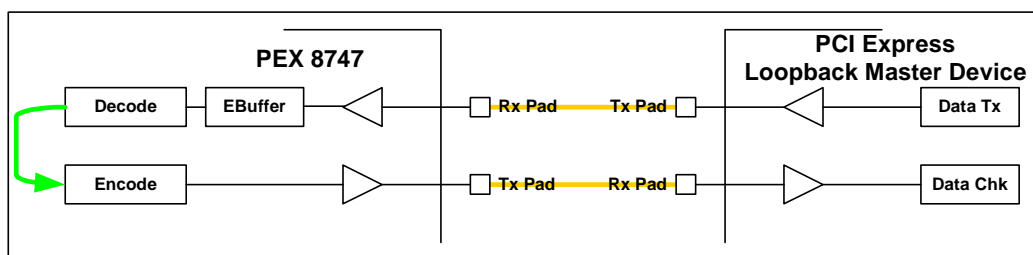
The PEX 8747 becomes a Digital Loopback Slave if it receives Training Sets with the *Loopback Training Control Bit Set*, –or– the Port’s **Physical Layer Test 1** register *Port x Parallel Loopback Path Enable* bit (Port 0, 8, or 16, offset 228h[17:16]) is Set, while the **Physical Layer Test 0** register *Analog Loopback Enable* bit (Port 0, 8, or 16, offset 224h[10]) is Cleared.

When a PEX 8747 Port is a Digital Loopback Slave:

- **Gen 1 and Gen 2 Link speeds (2.5 and 5.0 GT/s, respectively)** – Loopback data path includes the Elastic buffer and symbol alignment logic
- **Gen 3 Link speed (8.0 GT/s)** – Loopback data path includes the Elastic buffer and block aligner, as well as the 128b/130b encoder and decoder

The Loopback Master must provide the test data pattern and data pattern checker (*such as* a PEX 8747 User Test Pattern). The Loopback Master must also transmit SKIP Ordered-Sets with the data pattern. The PEX 8747 can return more or fewer SKIP symbols than the switch received from the Master. Therefore, the Master’s data pattern checker must make provisions for this when decoding for errors.

Figure 12-7. Digital Loopback Slave Mode



Note: 8b/10b (Gen 1 and Gen 2 Link speeds) or 128b/130b (Gen 3 Link speed) encode/decode.

12.3 Built-In Self-Test

Each Lane contains a Built-In Self-Test (BIST) generator and checker.

12.4 Using the SerDes Quad x Diagnostic Data Registers

Each SerDes quad has its own Diagnostic Data register, per Station. The **SerDes Quad x Diagnostic Data** register (Port 0, 8, or 16, offsets [238h](#) through [244h](#)) contents reflect the performance of the SerDes selected by the registers' *SerDes Diagnostic Data Select* field [25:24]. This control is specific to this register (which reports results of UTP tests).

When field [25:24] is Cleared, the information in that Diagnostic Data register is for the first SerDes within that SerDes quad. When field [25:24] is programmed to 01b, the information in that Diagnostic Data register is for the second SerDes within that SerDes quad, as illustrated in [Table 12-3](#). Following this pattern, a value of 10b indicates the third SerDes within that SerDes quad, and a value of 11b indicates the fourth SerDes within that SerDes quad.

Table 12-3. SerDes Quad x Diagnostic Data Register Contents When *SerDes Diagnostic Data Select* Field [25:24]=01b (Ports 0, 8, and 16), by Station Port

Offset	Register	Port 0	Port 8	Port 16
238h	SerDes Quad 0 Diagnostic Data	SerDes 1	SerDes 17	SerDes 33
23Ch	SerDes Quad 1 Diagnostic Data	SerDes 5	SerDes 21	SerDes 37
240h	SerDes Quad 2 Diagnostic Data	SerDes 9	SerDes 25	SerDes 41
244h	SerDes Quad 3 Diagnostic Data	SerDes 13	SerDes 29	SerDes 45

12.5 PHY Testability Features

The PEX 8747 includes several Configuration bits to ease PHY testability. Features include:

- Full support of the standard and modified Compliance patterns
- Register controllability of the common block and Lane-specific inputs of the SerDes

Table 12-4 describes the Configuration bits.

Table 12-4. Configuration Bits to Ease PHY Testability

Register Bit(s) ^a	Description
<i>SerDes x Mask Electrical Idle Detect</i> Physical Layer Electrical Idle Detect Mask register (offset 204h[15:0])	Never Detect Electrical Idle Mask. When any one of these bits is Set, the Lane's Electrical Idle condition flag does not assert, regardless of the actual presence of Electrical Idle.
<i>SerDes x Mask Receiver Not Detected</i> Physical Layer Receiver Not Detected Mask register (offset 204h[31:16])	Always Detect a Receiver Mask. When any one of these bits is Set, the PHY functions as if the Lane detected a Receiver, regardless of the actual presence of a Receiver.
<i>User Test Pattern</i> Physical Layer User Test Pattern, Bytes x through y registers (offsets 20Ch through 218h)	A 16-byte test pattern can be written to these four registers. When UTP transmission is enabled, Byte 0 of register offset 20Ch is transmitted first and Byte 3 of register offset 218h is transmitted last. (Refer to Section 12.2.4 for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.
<i>Port x Scrambler Disable Command</i> Physical Layer Port Command register (offset 230h[1 or 5])	Scramble Disable. Unconditionally disables the data scramblers on the Port's Lane(s), and causes the <i>Scramble Disable</i> Training Control Bit to be Set in transmitted Training Sets. There is one bit, per Port, per Station.
<i>Disable Port x</i> Port Control register (offset 208h[1:0])	Unconditional Port Disable. When Set, the LTSSM remains in the <i>Detect.Quiet</i> substate on the Port if it is currently in, or returns to, that substate. Unconditionally disables the Port. This is different from the LTSSM <i>Disabled</i> state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the <i>Detect.Quiet</i> substate and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the <i>Recovery</i> state, and then to an LTSSM <i>Detect</i> state. The Port remains disabled until its <i>Disable Port x</i> bit is Cleared. While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state.
<i>Hold Port x Quiet</i> Port Control register (offset 208h[9:8])	Port Quiet. When Set, the LTSSM remains in the <i>Detect.Quiet</i> substate if it is currently in, or returns to, that substate. These bits do not force the LTSSM to the <i>Detect.Quiet</i> substate. (Refer to the <i>Disable Port x</i> bits.) After entering the <i>Detect.Quiet</i> substate, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the <i>Loopback.Active</i> substate.
<i>Port x Bypass UTP Alignment Pattern</i> Port Control register (offset 208h[17:16])	Bypass Alignment Pattern. When Cleared, the UTP Transmitter continuously transmits the UTP alignment pattern (K28.5 D3.2 D18.2 D13.2), to allow the corresponding symbol alignment logic to find the symbol boundaries before sending the sync pattern (D3.2 D18.2 D13.2 D17.1) and programmed UTP. When Set, the UTP transmitter sends one UTP alignment pattern (K28.5 D3.2 D18.2 D13.2), one sync pattern (D3.2 D18.2 D13.2 D17.1), and then the programmed UTP.

Table 12-4. Configuration Bits to Ease PHY Testability (Cont.)

Register Bit(s) ^a	Description
<i>Port x Test Pattern x Rate</i> Port Control register (offset 208h[24])	Test Pattern Rate. The Port transmits the selected test pattern (PRBS or UTP) at 8.0 GT/s, if the Port's Port Control register <i>Hold Port x Quiet</i> bit (offset 208h[9:8]) is also Set (manual rate selection is enabled only when the <i>Hold Port x Quiet</i> bit is Set).
Physical Layer Error Injection Control register (offset 25Ch)	1-Bit Error Injection. Provides Port-specific controls for 1-bit error injection from the PEX 8747 Transmitters. Far-end devices can use this feature to test their error-handling capability.
<i>Port x Receiver Error Counter</i> Port Receiver Error Counter register (offset BF0h[31:0])	Receiver Error Counter. Contains four 8-bit fields that, when read, return the quantity of Receiver errors that the Port detected. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this register is RO.

a. All register bits listed in this table are located in Port 0, 8, or 16.

12.6 JTAG Interface

The PEX 8747 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each ball.

12.6.1 *IEEE 1149.1* and *IEEE 1149.6* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly called the *JTAG Debug Port*, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to *1149.1* to support PCI Express SerDes testing. These standards describe methods for accessing internal device facilities, using a four- or five-signal interface.

The JTAG Debug Port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals** – JTAG Debug Port implements the four required JTAG signals – [JTAG_TCK](#), [JTAG_TDI](#), [JTAG_TDO](#), [JTAG_TMS](#) – and optional [JTAG_TRST#](#) signal
- **Clock Requirements** – JTAG_TCK signal frequency ranges from 0 to 15 MHz
- **JTAG Reset Requirements** – Refer to [Section 12.6.4](#)

12.6.2 JTAG Instructions

The JTAG Debug Port provides the *IEEE Standard 1149.1-1990* BYPASS, EXTEST, SAMPLE, PRELOAD, CLAMP, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. [Table 12-5](#) lists the JTAG instructions, along with their input codes.

The PEX 8747 returns the JTAG IDCODE values listed in [Table 12-6](#).

Table 12-5. JTAG Instructions

Instruction	Input Code	Comments
BYPASS	7EFFh	<i>IEEE Standard 1149.1-1990</i>
EXTEST	7FDFh	
SAMPLE	7FCFh	
PRELOAD	7FCFh	
EXTEST_PULSE	7F9Fh	<i>IEEE Standard 1149.6-2003</i>
EXTEST_TRAIN	7F5Fh	
CLAMP	7FEFh	<i>IEEE Standard 1149.1-1990</i>
IDCODE	1FFFh	

Table 12-6. JTAG IDCODE Values

Silicon Revision	Units	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
BA	Bits	0001b	1000_0111_0100_0111b	001_1100_1101b	1
	Hex	1h	8747h	1CDh	1h
	Decimal	1	34631	461	1
CA	Bits	0010b	1000_0111_0100_0111b	001_1100_1101b	1
	Hex	2h	8747h	1CDh	1h
	Decimal	2	34631	461	1

12.6.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE Standard 1149.1-1994, is a supplement to the IEEE Standard 1149.1-1990 and IEEE Standard 1149.1a-1993, *IEEE Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the IEEE 1076-1993 *Standard VHSIC Hardware Description Language (VHDL)*, allows a rigorous description of testability features in components which comply with the standard. This standard is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical Port description, physical ball map, instruction set, and **Boundary** register description.

The logical Port description assigns symbolic names to the device's signal balls. Each ball includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical ball map correlates the device's logical Ports to the physical balls of a specific package. A BSDL description can include several physical ball maps, and maps are provided with a unique name.

Instruction set statements describe the bit patterns that must be shifted into the **Instruction** register to place the device in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the PEX 8747.

The **Boundary** register description lists each cell or shift stage of the **Boundary** register. Each cell has a unique number – the cell numbered 0 is the closest to the **JTAG Test Data Output (JTAG_TDO)**, and the cell with the highest number is closest to the **JTAG Test Data Input (JTAG_TDI)**. Each cell includes additional information, *such as*:

- Cell type
- Logical Port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

12.6.4 JTAG Reset Input – JTAG_TRST#

The **JTAG_TRST#** input is the asynchronous reset input to the JTAG TAP Controller logic. JTAG_TRST# assertion places the PEX 8747's TAP Controller into the *Test-Logic-Reset* state, which selects the PEX 8747 standard logic path (core-to-I/O), as required for typical functionality of the switch. JTAG_TRST# de-assertion enables the TAP Controller for test and debug functionality, such as boundary scan.

- If JTAG functionality is required, the JTAG_TRST# input should be transitioned from Low-to-High once during PEX 8747 bootup, along with **PEX_PERST#** de-assertion. In any JTAG state, the JTAG TAP Controller can be returned to the *Test-Logic-Reset* (initial) state, by holding the **JTAG_TMS** input High while clocking the **JTAG_TCK** input at least five times.
- If the design is not going to use the JTAG TAP Controller, an external pull-down resistor is recommended on the JTAG_TRST# input, because its internal pull-down resistor is weak.

12.7 Port Good Status LEDs

The PEX 8747 provides Port Good outputs, PORT_GOOD[9:8, 5:4, 0]# (PORT_GOODx#), that can be used to control external circuitry, *such as* LEDs, to provide visual indication that the PHY of that Port's Link is trained to at least x1 width. These outputs can:

- Default to the PORT_GOOD output function, when the STRAP_TESTMODE0 3-state input selects the PORT_GOOD output function (*that is*, Test mode 0), –or–
- Be programmed as a general-purpose I/O, to assume the PORT_GOOD output function (refer to the GPIO 0_x Direction Control register Direction Control bit(s) (Port 0, offset(s) 600h and/or 604h)

The PORT_GOODx#/GPIOx I/Os operate from the VDD18 supply, and the maximum input voltage is 2.5V. Because the LED forward voltage drop is typically greater than 1.8V, the LED voltage source will likely be higher than 2.5V. In this case, if the LED is connected directly to the PORT_GOODx# input, the input voltage level (while the LED is turned Off) would exceed the specification. Therefore, a PORT_GOODx# signal typically cannot drive an LED directly; however, it can be used to gate a transistor that switches the LED On and Off.

Notes: PORT_GOOD[9:8, 5:4, 0]# correspond to Ports 17, 16, 9, 8, and 0, respectively. PORT_GOODx# signals can be re-assigned to any Port, however, by programming the Port Good Selector x register(s) (Port 0), offset(s) 6A0h through 6A8h).

Table 4-1 indicates which Ports are enabled/used, and when, based upon the STRAP_STNx_PORTCFG0 input states and/or serial EEPROM programming.

Table 12-7 describes the LED On/Off patterns when connected to the PORT_GOODx# signals.

Table 12-7. PORT_GOODx# LED On/Off Patterns, by State

State	LED Pattern
Link is Down	Off
Link is Up, 2.5 GT/s, any negotiated Link width	Blinking, 512 ms On, 512 ms Off (1 Hz)
Link is Up, 5.0 GT/s, any negotiated Link width	Blinking, 256 ms On, 256 ms Off (2 Hz)
Link is Up, 8.0 GT/s, any negotiated Link width	On

Software can determine:

- Which Lanes have completed PHY linkup, by performing a Memory Read of the Station x Lane Status register(s) Lane x Up Status bits (Port 0, offset(s) 330h[31:0] and 334h[15:0]).
- Whether the Link for each Port has trained, by reading either the Port's Link Status register Data Link Layer Link Active bit (Downstream Ports, offset 78h[29]) or VC0 Resource Status register VC0 Negotiation Pending bit (offset 160h[17]). If the Data Link Layer Link Active bit is Set, or VC0 Negotiation Pending bit is Cleared, the Link has completed Flow Control (FC) initialization.

The Link Status register can be read by either a PCI Express Configuration Request or Memory Read. The VC0 Resource Status register can be read by either a PCI Express Enhanced Configuration access or Memory Read.

- The negotiated Link width of each Port, by reading the Port's Link Status register Negotiated Link Width field (offset 78h[25:20]). This register can be read by either a Configuration Request or Memory Read.

12.8 Thermal Sensor Diode – 27 x 27 mm² Package

The PEX 8747 includes a thermal-sensing diode, to facilitate the measurement of on-die device junction temperature. On the package level, there are two external inputs – [THERMAL_DIODEn](#) and [THERMAL_DIODEp](#), that connect to anode and cathode terminals of a diode-connected transistor (PNP) implemented on the die.

At the board level, a temperature sensor chip, *such as* the Maxim MAX6657^a, can be used.

For further details, refer to the manufacturer's data sheet for the device being used.

Note: *The PEX 8747 thermal diode produces an offset in the external temperature sensor that results in a temperature reading that is 24°C above the approximate die temperature. Consequently, a temperature sensor chip that measures a maximum temperature of 128°C might not be sufficient, because the maximum temperature reported is effectively reduced to 104°C (128 - 24 = 104). Some sensor ICs support higher temperatures, such as 145°C; however, these devices have not been tested with the PEX 8747 thermal diode.*

a. The MAX6657, MAX6658, and MAX6659 are ±1°C, SMBus-Compatible Remote/Local Temperature Sensors with Overtemperature Alarms,” by Maxim Integrated Products.

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Chapter 13 Electrical Specifications

13.1 Introduction

This chapter provides the PEX 8747 electrical specifications:

- [Power-Up/Power-Down Sequence](#)
- [Absolute Maximum Ratings](#)
- [Power Characteristics](#)
- [Power Consumption Estimates](#)
- [I/O Interface Signal Groupings](#)
- [Transmit Characteristics](#)
- [Receive Characteristics](#)

13.2 Power-Up/Power-Down Sequence

The PEX 8747 does not have power sequencing requirements. The power rails can be powered up and powered down, in any sequence.

13.3 Absolute Maximum Ratings

Warning: *Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the PEX 8747 at these limits is not recommended.*

Table 13-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
I/O Interface Supply Voltage	VDD18	1.98	V
PLL Supply Voltage	VDD18A	1.98	V
Core (Logic) Supply Voltage	VDD09	0.99	V
SerDes Analog Supply Voltage	VDD09A	0.99 ^a	V
Input Voltage (1.8V Interface)	V _I	2.75	V
Operating Ambient Temperature (Commercial)	T _A	0 to +70	°C
Storage Temperature	T _{STG}	-65 to +150	°C

a. Technically 1.1V; however, most users tie VDD09A to 0.99V.

13.4 Power Characteristics

Table 13-2. Operating Condition Power Supply Rails

Symbol	Parameter	Voltage and Ranges	Min	Typ	Max	Units
VDD09	Digital Core Supply	0.9V -5%, +5.55%	0.855	0.9	0.95	V
VDD09A	Analog SerDes Supply	0.9V -5%, +5.55%	0.855	0.9	0.95	V
VDD18 ^a	I/O Supply	1.8V -5%, +10%	1.71	1.8	1.98	V
VDD18A	Phase-Locked Loop (PLL) Supply	1.8V -5%, +10%	1.71	1.8	1.98	V

a. The PEX 8747 I/Os are 2.5V-tolerant.

13.5 Power Consumption Estimates

Table 13-3. Power Consumption Estimates (Watts)

Lanes	Ports	Link Speed (GT/s)	Digital (VDD09)		SerDes Analog (VDD09A)		PLL and I/O (VDD18A + VDD18)		Total	
			Typ	Max	Typ	Max	Typ	Max	Typ ^a	Max ^{b, c}
48	3 or 5	2.5	3.32	8.45	2.09	3.25	0.83	0.98	6.24	12.69
		5.0	3.69	9.19	2.09	3.41	0.83	0.98	6.60	13.58
		8.0	3.81	9.90	2.70	4.13	0.83	0.98	7.34	15.02

a. Typical power based upon 35% traffic, idle Lanes in active L0s PM state, typical power rails (0.9V/1.8V), at 25°C.

b. Maximum power based upon 85% traffic, idle Lanes in active L0s Link PM state, maximum power rails (0.95V/1.98V).

c. Maximum power is at 110°C Junction temperature and Fast/Fast (FF) process corner silicon.

13.6 I/O Interface Signal Groupings

Table 13-4. Signal Group PCI Express Analog Interface

Signal Group	Signal Type	Signals	Notes
(a)	PCI Express Output (Transmit)	PEX_PETp/nx	Refer to Table 13-6 and Table 13-7
(b)	PCI Express Input (Receive)	PEX_PERp/nx	Refer to Table 13-6 and Table 13-12
(c)	PCI Express Differential Clock Input	PEX_REFCLKp/n	Refer to Table 13-6
(d)	SerDes External Bias Resistor	REXT_Ax, REXT_Bx, REXT_CMU	3.00K Ω \pm 1%, and refer to Table 13-6

Table 13-5. Signal Group Digital Interface

Signal Group	Signal Type	Signals	Note
(e)	Digital Input	STRAP_RESERVEDx ^a , STRAP_RESERVED19# ^a , THERMAL_DIODEn/p ^b	Refer to Table 13-6
(f)	Digital Input with Internal Pull-Up Resistor	PEX_PERST#, STRAP_PLL_BYPASS#, STRAP_PROBE_MODE# ^b , STRAP_SERDES_MODE_EN# ^b	
(g)	Digital Input with Internal Pull-Down Resistor	JTAG_TCK, JTAG_TDI, JTAG_TMS, JTAG_TRST#	
(h)	Bidirectional with Internal Pull-Up Resistor (8 mA Drive)	EE_CS#, EE_DO, EE_SK, GPIO[10, 6, 3:1], PORT_GOOD[9, 5:4, 0]#, SPARE[2:0], STRAP_I2C_SMBUS_CFG_EN#	
(j)	Bidirectional with Internal Pull-Down Resistor (8 mA Drive)	GPIO7, PORT_GOOD8#, SPARE3	
(k)	Bidirectional Tri-Statable Output with Limited Slew Rate Input	I2C_SCL0, I2C_SDA0, PEX_INTA#	
(m)	Bidirectional Tri-Statable Output	EE_DI, FATAL_ERR#, JTAG_TDO	
(n)	Bidirectional with 3-State Input	I2C_ADDR0, STRAP_GEN1_GEN2 ^b , STRAP_I2C_SMBUS_EN, STRAP_STN1_PORTCFG0, STRAP_STN2_PORTCFG0, STRAP_TESTMODE0, STRAP_UPSTRM_PORTSEL[2:0] ^c	

- a. These signals must be pulled or tied High to VDD18 or Low to VSS (Ground). Refer to [Table 3-6](#), “Factory Test Only STRAP_RESERVED[21:20], STRAP_RESERVED19#, STRAP_RESERVED[18, 16:14, 12:9, 7, 5, 4:0] Input External Pull-Up/Pull-Down Resistor Requirements,” (27 x 27 mm² package), or [Table 3-17](#), “Factory Test Only STRAP_RESERVED[21:20], STRAP_RESERVED19#, STRAP_RESERVED[16:14, 9, 7, 5, 0] Input External Pull-Up/Pull-Down Resistor Requirements” (19 x 21 mm² package), for specific requirements.
- b. This signal exists only in the 27 x 27 mm² package.
- c. STRAP_UPSTRM_PORTSEL2 exists only in the 27 x 27 mm² package.

Table 13-6. Analog and Digital Interfaces (All Signal Groups) – DC Electrical Characteristics

Symbol	Signal Group	Parameter	Min	Typ	Max	Unit	Conditions
I_{OL}	(h) (k)	Output Low Current	10.4	17.9	26.5	mA	$V_{OLmax} = 0.45V$
I_{OH}	(h)	Output High Current	9.0	20.2	36.5	mA	$V_{OHmin} = 1.35V$
V_{IL}	(e) (f) (g) (h) (k)	Input Low Voltage	-0.3		0.63	V	
V_{IH}	(e) (f) (g) (h) (k)	Input High Voltage	1.17		2.75	V	
V_T	(e) (g) (h) (k)	Threshold Point	0.78	0.84	0.89	V	
C_{PIN}	(a) (b) (c) (d) (e) (f) (g) (h) (j) (k)	Ball Capacitance			5	pF	
$I_{LEAKAGE}$	(m)	Tri-State Leakage			± 10	μA	
	(e) (f)	Input Leakage			± 10	μA	
R_{PU}	(f) (h)	Pull-Up Impedance	38K	57K	92K	Ω	
R_{PD}	(g) (j)	Pull-Down Impedance	37K	53K	99K	Ω	

13.7 Transmit Characteristics

13.7.1 PCI Express Transmitter AC and DC Characteristics

Table 13-7. PCI Express Transmitter (Signal Group a) – AC and DC Characteristics

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	124.9625 (min) 125.0375 (max)	ps	The specified UI is equivalent to a tolerance of ± 300 ppm for each REFCLK source. Period does not account for Spread-Spectrum Clock (SSC)-induced variations. Refer to Note 1.
BW _{TX-PLL}	Tx PLL Bandwidth for 2.5 GT/s	1.5 (min) 22 (max)	Not specified	Not specified	MHz	Refer to Note 6.
BW _{TX-PKG-PLL1}	Tx PLL Bandwidth corresponding to PKG _{TX-PLL1}	Not specified	8 (min) 16 (max)	2 (min) 4 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 6.
BW _{TX-PKG-PLL2}	Tx PLL Bandwidth corresponding to PKG _{TX-PLL2}	Not specified	5 (min) 16 (max)	2 (min) 5 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 6.
PKG _{TX-PLL1}	Tx PLL Peaking	Not specified	3.0 (max)	2.0 (max)	dB	PLL Bandwidth = 8 MHz (min) at 5 GT/s or Bandwidth = 4 MHz (max) at 8 GT/s. Refer to Notes 6 and 8.
PKG _{TX-PLL2}	Tx PLL Peaking	Not specified	1.0 (max)	1.0 (max)	dB	PLL Bandwidth = 5 MHz (min) at 5 GT/s or Bandwidth = 5 MHz (max) at 8 GT/s. Refer to Note 8.
V _{TX-DIFF-PP}	Differential Peak-to-Peak Tx Voltage Swing	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	Refer to Table 13-9	VPP	Measured with compliance test load. Defined as $2 \times V_{TX-D+} - V_{TX-D-} $
V _{TX-DIFF-PP-LOW}	Low Power Differential Peak-to-Peak Tx Voltage Swing	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	Refer to Table 13-9	VPP	Measured with compliance test load. Defined as $2 \times V_{TX-D+} - V_{TX-D-} $. Refer to Note 9.
V _{TX-DE-RATIO-3.5dB}	Tx De-Emphasis Level Ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	Refer to Table 13-9	dB	
V _{TX-DE-RATIO-6dB}	Tx De-Emphasis Level Ratio	–	5.5 (min) 6.5 (max)	Refer to Table 13-9	dB	
T _{MIN-PULSE}	Instantaneous Lone Pulse Width	Not specified	0.9 (min)	Refer to Table 13-9	UI	Measured relative to rising/falling pulse. Refer to Notes 2 and 10.

Table 13-7. PCI Express Transmitter (Signal Group a) – AC and DC Characteristics (Cont.)

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
T_{TX-EYE}	Tx Eye Width (including all jitter sources)	0.75 (min)	0.75 (min)	Refer to Table 13-9	UI	Does not include SSC nor REFCLK jitter. Includes R_j at 10^{-12} . Refer to Notes 2, 3, 4, and 10. Note: 2.5 and 5.0 GT/s use different jitter determination methods.
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	0.125 (max)	Not specified	Not specified	UI	Measured differentially at zero crossing points, after applying the 2.5 GT/s Clock Recovery function. Refer to Note 2.
$T_{TX-HF-DJ-DD}$	Tx Deterministic Jitter > 1.5 MHz	Not specified	0.15 (max)	Refer to Table 13-9	UI	Deterministic jitter only. Refer to Notes 2 and 10.
$T_{TX-LF-RMS}$	Tx RMS Jitter < 1.5 MHz	Not specified	3.0	Refer to Table 13-9	ps RMS	Total energy measured over a 10-kHz to 1.5-MHz range.
$T_{TX-RISE-FALL}$	Tx Rise and Fall Time	0.125 (min)	0.15 (min)	Not specified	UI	Measured differentially from 20 to 80% of swing.
$T_{RF-MISMATCH}$	Tx Rise/Fall Mismatch	Not specified	0.1 (max)	Not specified	UI	Measured from 20 to 80% differentially. Refer to Note 2.
$RL_{TX-DIFF}$	TX Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz 4 (min) for 2.5 to 4 GHz	dB	
RL_{TX-CM}	TX Common Mode Return Loss (Package + Silicon)	6 (min) for 0.05 to 2.5 GHz	6 (min) for 0.05 to 2.5 GHz	6 (min) for 0.05 to 2.5 GHz 3 (min) for 2.5 GHz	dB	
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80 (min) 120 (max)	120 (max)	120 (max)	Ω	Low impedance defined during signaling. Parameter is captured for 5.0 GHz by $RL_{TX-DIFF}$.

Table 13-7. PCI Express Transmitter (Signal Group a) – AC and DC Characteristics (Cont.)

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
$V_{TX-CM-AC-PP}$	Tx AC Peak-to-Peak Common Mode Voltage (5.0 GT/s)	Not specified	150 (max)	150 (max)	mVPP	For 8 GT/s, no more than 50 mVPP within the 0.03- to 500-MHz range. Refer to Notes 5 and 12.
$V_{TX-CM-AC-P}$	Tx AC Peak Common Mode Voltage (2.5 GT/s)	20	Not specified	Not specified	mV	Refer to Note 5.
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	90 (max)	90 (max)	90 (max)	mA	Total single-ended current the Transmitter can supply when shorted to its Ground. Refer to Note 13.
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0 (min) 3.6 (max)	0 (min) 3.6 (max)	0 (min) 3.6 (max)	V	Allowed DC common mode voltage at a Transmitter ball, under any conditions. Refer to Note 13.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 Link PM state and Electrical Idle	0 (min) 100 (max)	0 (min) 100 (max)	0 (min) 100 (max)	mV	$ V_{TX-CM-DC} [\text{during L0}] - V_{TX-CM-Idle-DC} [\text{during Electrical Idle}] \leq 100 \text{ mV}$ $V_{TX-CM-DC} = DC_{(avg)} \text{ of } V_{TX-D+} + V_{TX-D-} / 2 [L0]$ $V_{TX-CM-Idle-DC} = DC_{(avg)} \text{ of } V_{TX-D+} + V_{TX-D-} / 2 [\text{Electrical Idle}]$
$V_{TX-CM-DC-LINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25 (max)	0 (min) 25 (max)	0 (min) 25 (max)	mV	$ V_{TX-CM-DC-D+} - V_{TX-CM-DC-D-} \leq 25 \text{ mV}$ $V_{TX-CM-DC-D+} = DC_{(avg)} \text{ of } V_{TX-D+} $ $V_{TX-CM-DC-D-} = DC_{(avg)} \text{ of } V_{TX-D-} $
$V_{TX-IDLE-DIFF-AC-p}$	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	0 (min) 20 (max)	mV	$V_{TX-IDLE-DIFFp} = V_{TX-Idle-D+} - V_{TX-Idle-D-} \leq 20 \text{ mV}$ Voltage must be high-pass filtered, to remove any DC component and HF noise. The bandpass is constructed from two first-order filters, the high- and low-pass 3-dB bandwidths are 10 kHz and 1.25 GHz, respectively.
$V_{TX-IDLE-DIFF-DC}$	DC Electrical Idle Differential Peak Output Voltage	Not specified	0 (min) 5 (max)	0 (min) 5 (max)	mV	$V_{TX-IDLE-DIFF-DC} = V_{TX-Idle-D+} - V_{TX-Idle-D-} \leq 5 \text{ mV}$ Voltage must be high-pass filtered, to remove any AC component. The low pass filter is first-order with a 3-dB bandwidth of 10 kHz.

Table 13-7. PCI Express Transmitter (Signal Group a) – AC and DC Characteristics (Cont.)

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
$V_{TX-RCV-DETECT}$	Amount of Voltage Change Allowed during Receiver Detection	600 (max)	600 (max)	600 (max)	mV	Total amount of voltage change in a positive direction that a Transmitter can apply, to sense whether a Low-Impedance Receiver is present. <i>Note: Receivers display substantially different impedance for $V_{IN} < 0$ versus $V_{IN} > 0$.</i>
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	20 (min)	20 (min)	20 (min)	ns	Minimum time a Transmitter must be in Electrical Idle.
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered-Set	8 (max)	8 (max)	8 (max)	ns	After sending the required Electrical Idle Ordered-Set (EIOS), the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Transmitter in Electrical Idle.
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum Time to Transition to Valid Differential Signaling after Leaving Electrical Idle	8 (max)	8 (max)	8 (max)	ns	Maximum time to transition to valid differential signaling, after leaving Electrical Idle. This is considered a de-bounce time to the Tx.
$T_{CROSSLINK}$	Cross-Link Random Timeout	1.0 (max)	1.0 (max)	1.0 (max)	ms	Random timeout that helps resolve potential conflicts in the cross-link configuration.
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	500 ps + 2 UI (max)	500 ps + 4 UI (max)	500 ps + 6 UI (max)	ps	Static skew between any two Lanes within a single Transmitter.
C_{TX}	AC-Coupling Capacitor	75 (min) 265 (max)	75 (min) 265 (max)	176 (min) 265 (max)	nF	All Transmitters shall be AC-coupled. The AC coupling is required either within the media, or within the transmitting component itself. Refer to Note 14.

Notes:

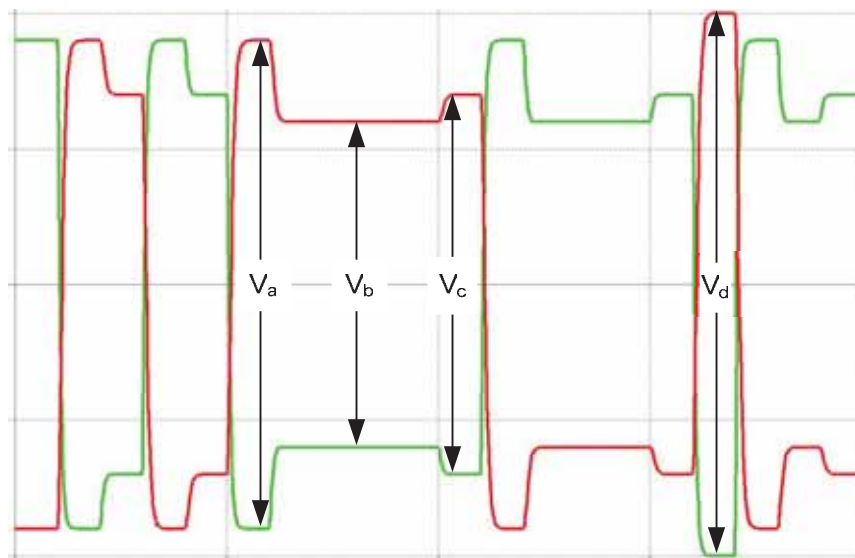
1. SSC permits a ± 0 , $\pm 5,000$ ppm modulation of the clock frequency, at a modulation rate not to exceed 33 kHz.
2. Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥ 12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require an oscilloscope with at least 6.2 GHz bandwidth. Measurement at 5.0 GT/s must de-convolve effects of a compliance test board, to yield an effective measurement at the Tx balls. 2.5 GT/s can be measured within 200 mils of the Tx device's pins, although de-convolution is recommended.
3. Transmitter jitter is measured by driving the Transmitter under test with a low jitter "ideal" clock and connecting the device under test (DUT) to a reference load.
4. Transmitter raw jitter data must be convolved with a filtering function that represents the worst case Clock and Data Recovery (CDR) circuit tracking bandwidth. 2.5 and 5.0 GT/s use different filter functions. After the convolution process is applied, the center of the resulting eye must be determined and then used as a reference point for obtaining eye voltage and margins.
5. $V_{TX-AC-CM-PP}$ and $V_{TX-AC-CM-P}$ are defined in the PCI Express Base r3.0, Section 4.3.4.9. Measurement is made over at least 10^6 UI.
6. The Tx PLL bandwidth must lie between the minimum and maximum ranges listed in [Table 13-7](#). PLL peaking must lie below the values listed in [Table 13-7](#). The PLL bandwidth extends from zero (0), up to the value(s) specified in [Table 13-7](#).
7. Measurements are made for both common mode and differential return loss. The DUT must be powered up and DC isolated, and its data+/data- outputs must be in the low-Z state at a static value
8. A single combination of PLL bandwidth and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two 20 combinations of PLL bandwidth and peaking are specified, to permit designers to make a tradeoff between the two parameters. If the PLL's minimum bandwidth is ≥ 8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥ 5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the maximum PLL bandwidth is 16 MHz.
9. Low swing output, defined by $V_{TX-DIFF-PP-LOW}$ must be implemented with no de-emphasis.
10. For 5.0 GT/s, de-emphasis timing jitter must be removed. This parameter is measured by accumulating a record length of 106 UI while the DUT outputs a compliance pattern. $T_{MIN-PULSE}$ is defined to be nominally 1 UI-wide, and is bordered on both sides by pulses of the opposite polarity.
11. Root Complex Tx de-emphasis is configured from an Upstream controller. Downstream Tx de-emphasis is Set by way of a command, issued at 2.5 GT/s. For details, refer to the appropriate location in the PCI Express Base r3.0, Section 4.2.
12. Tx common mode (CM) noise for 8.0 GT/s is measured at TP1, without de-embedding the breakout channel. The parameter captures device CM noise only, and is not intended to capture system CM noise. CM noise is measured by applying an LPF with a -3 dB corner frequency at 4 GHz to the raw data. No more than 50 mVPP of the 150 mVPP total can lie within the 0.03- to 500-MHz range.
13. $I_{TX-SHORT}$ and $V_{TX-DC-CM}$ stipulate the maximum current/voltage levels that a Transmitter can generate, and therefore define, the worst case transients that a Receiver must tolerate.
14. All Transmitters supporting 8.0 GT/s must implement the 180 to 265 nF C_{TX} value. Transmitters operating at 2.5 or 5.0 GT/s only may implement over a range of 75 to 265 nF.

13.7.2 Tx Preshoot and De-Emphasis

The equalization ratios implemented by the transmitter can be calculated from the PIPE tap-coefficients. These ratios are computed, based upon the voltage levels defined in [Figure 13-1](#).

[Table 13-8](#) defines the **x Preshoot and De-Emphasis Presets**

Figure 13-1. Definition of Tx Voltage Levels and Equalization Ratios



where

- De-Emphasis = $20 \log_{10} (V_b / V_a)$
- Preshoot = $20 \log_{10} (V_c / V_b)$
- Boost = $20 \log_{10} (V_d / V_b)$

Table 13-8. Tx Preshoot and De-Emphasis Presets

Preset Select ^a (Decimal)	Preshoot (dB)	De-Emphasis (dB)	De-Emphasis ^b (Decimal)	Main ^c (Decimal)	Preshoot ^d (Decimal)	Total
0	0	-6.0	16	47	0	63
1	0	-3.5	11	52	0	63
2	0	-4.5	13	50	0	63
3	0	-2.5	8	55	0	63
4	0	0	0	63	0	63
5	2.0	0	0	57	6	63
6	2.5	0	0	55	8	63
7	3.5	-6.0	13	44	6	63
8	3.5	-3.5	8	47	8	63
9	3.5	0	0	52	11	63
10	0	-9.5	21	42	0	63
11 to 15	Reserved					

- a. **Gen 3 Coefficient Values** register *Preset Select* field (Port 0, 8, or 16, offset *BD4h[27:24]*).
- b. **Gen 3 Coefficient Values** register *Preset 0 Coefficients – De-Emphasis* field (Port 0, 8, or 16, offset *BD4h[17:12]*).
- c. **Gen 3 Coefficient Values** register *Preset 0 Coefficients – Main* field (Port 0, 8, or 16, offset *BD4h[11:6]*).
- d. **Gen 3 Coefficient Values** register *Preset 0 Coefficients – Preshoot* field (Port 0, 8, or 16, offset *BD4h[5:0]*).

13.7.3 Tx Voltage and Jitter

Table 13-9. Tx Voltage and Jitter Parameters

Symbol	Parameter	Value	Units	Notes
$V_{TX-FS-NO-EQ}$	Full Swing Tx Voltage with no TxEq	800 (min) 1,300 (max)	mVPP	Refer to Note 1.
$V_{TX-RS-NO-EQ}$	Reduced Swing Tx Voltage with no TxEq	1,300 (max)	mVPP	Refer to Note 1.
$V_{TX-EIEOS-FS}$	Min Swing during Electrical Idle Exit Ordered-Set (EIEOS) for Full Swing	250 (min)	mVPP	Refer to Note 2.
$V_{TX-EIEOS-RS}$	Min Swing During EIEOS for Reduced Swing	232 (min)	mVPP	Refer to Note 2.
T_{TX-UTJ}	Tx Uncorrelated Total Jitter	31.25 (max)	psPP at 10^{-12}	
$T_{TX-UDJDD}$	Tx Uncorrelated Deterministic Jitter	12 (max)	psPP	
$T_{TX-UPW-TJ}$	Total Uncorrelated PWJ	24 (max)	psPP at 10^{-12}	Refer to Notes 3 and 4.
$T_{TX-UPW-DJDD}$	Deterministic DjDD Uncorrelated PWJ	10 (max)	psPP	Refer to Notes 3 and 4.
T_{TX-DDJ}	Data-Dependent Jitter	18 (max)	psPP	Refer to Notes 4 and 5.
$ps21_{TX}$	Pseudo Package Loss	-3.0 (min)	dB	PP ratio of 64 ones/64 zeros pattern versus 0101 pattern. No Tx equalization. Refer to Note 6.
$V_{TX-BOOST-FS}$	Tx Boost Ratio for Full Swing	8.0 (min)	dB	
$V_{TX-BOOST-RS}$	Tx Boost Ratio for Reduced Swing	2.5 (min)	dB	
$EQ_{TX-COEFF-RES}$	Tx Coefficient Resolution	1/63	—	

Notes:

1. Voltage measurements for $V_{TX-FS-NO-EQ}$ and $V_{TX-RS-NO-EQ}$ are made using the 64-zeros/64-ones pattern in the compliance pattern.
2. Voltage limits comprehend both full swing and reduced swing modes. The Tx must reject any changes that would violate this specification. The maximum level is covered in the $V_{TX-FS-NO-EQ}$ measurement which represents the maximum peak voltage that the Tx can drive. The $V_{TX-EIEOS-FS}$ and $V_{TX-EIEOS-RS}$ voltage limits are imposed, to guarantee the EIEOS threshold of 175 mVPP at the Rx ball. This parameter is measured, using the actual EIEOS pattern that is part of the compliance pattern, and then removing the ISI contribution of the breakout channel. The Transmitter must advertise a value for LF during TSI at 8.0 GT/s that ensures that these parameters are met.
3. PWJ parameters shall be measured after DDJ separation.
4. Measured with optimized preset value, after de-embedding to the Tx ball.
5. The 18 ps number takes measurement errors into account.
6. The -3.0 dB number takes measurement errors into account. For some Tx package/driver combinations, $ps21_{TX}$ can be greater than 0 dB.

13.8 Receive Characteristics

The Receiver circuit includes programmable equalization, to further compensate for the low-pass FR4 loss characteristics of the channel.

13.8.1 Receive Equalization

Figure 13-2 illustrates an example frequency response of the attenuator (ATT), which displays nearly 24 dB of programmable attenuation. Also, the ATT is capable of providing up to 9 dB of analog boost at high frequencies, for channel compensation.

The Rx Attenuator can be programmed, using the registers listed in Table 13-10.

Figure 13-2. ATT Frequency Response for Different ATT Settings

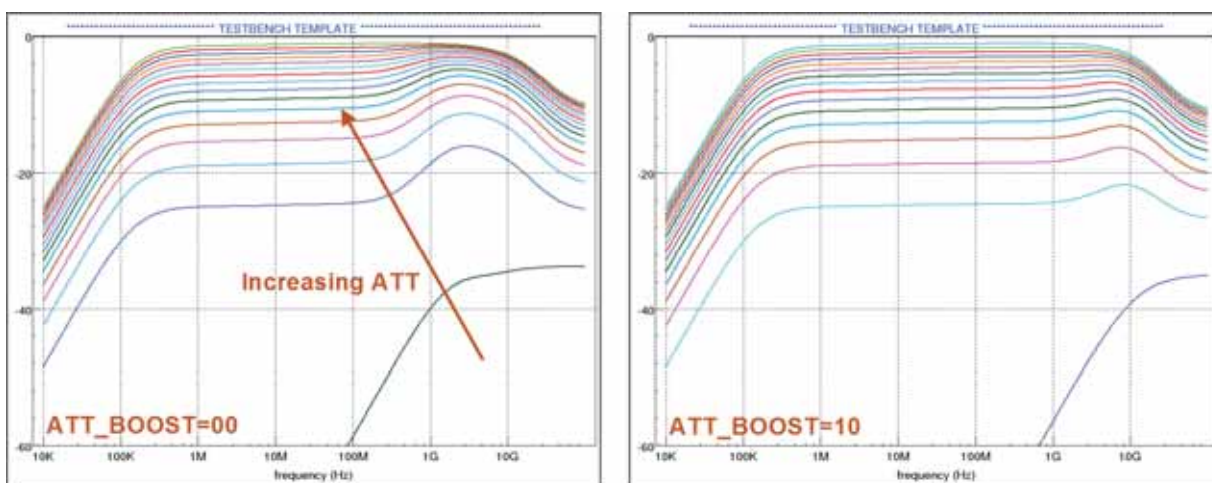


Table 13-10. Rx Attenuator Control

Register	Description
rx_att[3:0]	Rx attenuation value (15 minimum, 0 maximum).
rx_att_boost[1:0]	Rx attenuator analog boost value (2 minimum, 0 maximum, 3 invalid).

Figure 13-3. Increasing Boost

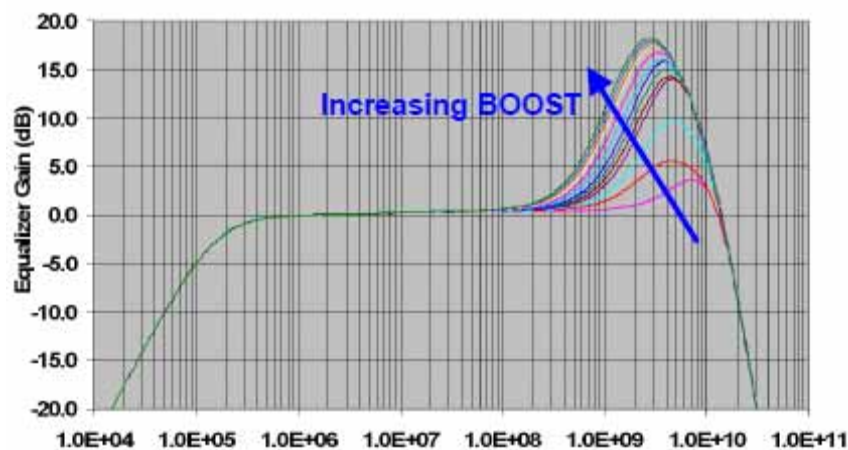


Table 13-11. Boost Settings and Gain

Boost Setting	Gain @ 4 GHz (dB)
0	0.75
1	1.31
2	1.74
3	2.46
4	4.69
5	5.46
6	7.84
7	8.18
8	10.10
9	11.78
10	12.98
11	15.20
12	15.61
13	17.25
14	17.25
15	17.25

13.8.2 PCI Express Receiver AC and DC Characteristics

Table 13-12. PCI Express Receiver (Signal Group b) – AC and DC Characteristics

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	124.9625 (min) 125.0375 (max)	ps	UI does not account for variations caused by SSC.
$V_{RX-DIFF-PP-CC}$	Differential Rx Peak-to-Peak Voltage for Common REFCLK Rx Architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	Refer to Table 13-13 and Table 13-14	V	
$V_{RX-DIFF-PP-DC}$	Differential Rx Peak-to-Peak Voltage for Data Clocked Rx Architecture	0.175 (min) 1.2 (max)	0.100 (min) 1.2 (max)	Refer to Table 13-13 and Table 13-14	V	
T_{RX-EYE}	Receiver Eye Time Opening	0.40 (min)	–	Refer to Table 13-13 and Table 13-14	UI	Minimum eye time at Rx balls to yield a 10^{-12} Bit Error Rate. Receiver eye margins are defined into a $2 \times 50\Omega$ reference load.
$T_{RX-TJ-CC}$	Maximum Rx Inherent Timing Error for Common REFCLK Rx Architecture	–	0.40 (max)	Refer to Table 13-13 and Table 13-14	UI	Refer to Note 1.
$T_{RX-TJ-DC}$	Maximum Rx Inherent Timing Error for Data Clocked Rx Architecture	–	0.34 (max)	Refer to Table 13-13 and Table 13-14	UI	Refer to Note 1.
$T_{RX-DJ-DD-CC}$	Maximum Rx Inherent Deterministic Timing Error for Common REFCLK Rx Architecture	–	0.30 (max)	Refer to Table 13-13 and Table 13-14	UI	Refer to Note 1.
$T_{RX-DJ-DD-DC}$	Maximum Rx Inherent Deterministic Timing Error for Data Clocked Rx Architecture	–	0.24 (max)	Refer to Table 13-13 and Table 13-14	UI	Refer to Note 1.

Table 13-12. PCI Express Receiver (Signal Group b) – AC and DC Characteristics (Cont.)

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Delta between the Median and Deviation from the Median	0.3 (max)	Not specified	Not specified	UI	Only specified for 2.5 GT/s.
$T_{RX-MIN-PULSE}$	Minimum Width Pulse at Rx	Not specified	0.6 (min)	Not specified	UI	Measured to account for worst T_j at 10^{-12} Bit Error Rate.
$V_{RX-MAX-MIN-RATIO}$	Minimum/Maximum Pulse Voltage on Consecutive UI	Not specified	5 (max)	Not specified	–	Rx eye must simultaneously meet V_{RX-EYE} limits.
BW_{RX-PLL}	Maximum Rx PLL Bandwidth for 2.5 GT/s	1.5 (min) 22 (max)	Not specified	Not specified	MHz	Refer to Note 2.
$BW_{RX-PKG-PLL1}$	Rx PLL Bandwidth corresponding to $PKG_{RX-PLL1}$	Not specified	8 (min) 16 (max)	2 (min) 4 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 2.
$BW_{RX-PKG-PLL2}$	Rx PLL Bandwidth corresponding to $PKG_{RX-PLL2}$	Not specified	5 (min) 16 (max)	2 (min) 5 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 2.
$PKG_{RX-PLL1}$	Rx PLL Peaking Limit for PLL1	Not specified	3.0 (max)	2.0 (max)	dB	PLL Bandwidth = 8 MHz (min) at 5 GT/s or Bandwidth = 4 MHz (max) at 8 GT/s. Refer to Note 2.
$PKG_{RX-PLL2}$	Rx PLL Peaking Limit for PLL2	Not specified	1.0 (max)	1.0 (max)	dB	PLL Bandwidth = 5 MHz (min) at 5 GT/s or Bandwidth = 5 MHz (max) at 8 GT/s. Refer to Note 2.
$RL_{RX-DIFF}$	Rx Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz 5 (min) for 2.5 to 4.0 GHz	dB	Refer to Note 3.

Table 13-12. PCI Express Receiver (Signal Group b) – AC and DC Characteristics (Cont.)

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
RL_{RX-CM}	Common Mode Return Loss	6 (min)	6 (min)	6 (min) for 0.05 to 1.25 GHz 8 (min) for 2.5 to 4.0 GHz	dB	Refer to Note 3.
Z_{RX-DC}	Rx DC Single Ended Impedance	40 (min) 60 (max)	40 (min) 60 (max)	Not specified	Ω	DC impedance limits are needed to guarantee Receiver detect. Refer to Note 4.
$T_{RX-GND-FLOAT}$	Rx Termination Ground Float Time	Not specified	Not specified	500	μs	Time allowed to float Rx internal Ground in 2.5 or 5.0 to 8.0 GT/s configuration change. Refer to Note 7.
$Z_{RX-DIFF-DC}$	DC Differential Rx Impedance	80 (min) 120 (max)	Not specified	Not specified	Ω	For 5.0 and 8.0 GT/s, covered under the $RL_{RX-DIFF}$ parameter. Refer to Note 4.
$V_{RX-CM-AC-P}$	Rx AC Common Mode Voltage	150 (max)	150 (max)	75 mV (max) (EH <100 mVPP) 125 mV (max) (EH \geq 100 mVPP)	mVP	Measured at Rx balls, into a pair of 50 Ω terminations into Ground. Refer to Note 5.
$Z_{RX-HIGH-IMP-DC-POS}$	DC Input Common Mode Input Impedance for Voltage >0 during Reset or Power-Down	10K (min)	10K (min)	10K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range 0 to 200 mV (with respect to Ground). Refer to Note 6.
$Z_{RX-HIGH-IMP-DC-NEG}$	DC Input Common Mode Input Impedance for Voltage <0 during Reset or Power-Down	1.0K (min)	1.0K (min)	1.0K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range -150 to 0 mV (with respect to Ground). Refer to Note 6.

Table 13-12. PCI Express Receiver (Signal Group b) – AC and DC Characteristics (Cont.)

Symbol	Parameter	Link Speed			Units	Comments
		2.5 GT/s	5.0 GT/s	8.0 GT/s		
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65 (min) 175 (max)	65 (min) 175 (max)	65 (min) 175 (max)	mV	$V_{RX-IDLE-DET-DIFFp-p} = \frac{1}{2} \times V_{RX-D+} - V_{RX-D-} $ Measured at the Receiver's package pins.
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected Electrical Idle Enter Idle Detect Threshold Integration Time	10 (max)	10 (max)	10 (max)	ms	An un-expected Electrical Idle ($V_{RX-DIFFp-p} < V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERTIME}$ to signal an unexpected idle condition.
$L_{RX-SKEW}$	Total Lane-to-Lane Skew	20 (max)	8 (max)	6 (max)	ns	Across all Lanes on a Port. $L_{RX-SKEW}$ comprehends Lane-to-Lane variations due to channel and repeater delay differences.

Notes:

1. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.
2. Two combinations of PLL bandwidth and peaking are specified at 5.0 GT/s, to permit designers to make trade-offs between the two parameters. If the PLL's minimum bandwidth is ≥ 8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥ 5.0 MHz, then a tighter peaking value of 1.0 dB must be met.

A PLL bandwidth extends from zero up to the value(s) defined as the minimum or maximum in [Table 13-12](#). For 2.5 GT/s, a single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3.0 dB are defined.

3. Measurements must be made for both common mode and differential return loss. In both cases, the DUT must be powered up and DC-isolated, and its D+/D- inputs must be in the low-Z state.
4. The Rx DC single-ended impedance must be present when the Receiver terminations are first enabled, to ensure that the Receiver Detect properly occurs. Compensation of this impedance can start immediately, and the Rx single-ended impedance (constrained by RL_{RX-CM} to $50\Omega \pm 20\%$) must be within the specified range by the time Detect is entered.
5. Common mode peak voltage is defined by the expression:

$$\max\{|(V_{d+} - V_{d-}) - V_{CMDC}|\}$$

6. $Z_{RX-HIGH-IMP-DC-NEG}$ and $Z_{RX-HIGH-IMP-DC-POS}$ are defined, respectively, for negative and positive voltages at the input of the Receiver. Transmitter designers must comprehend the large difference between >0 and <0 Rx impedances, when designing Receiver detect circuits.
7. Defines the time for the Receiver's input pads to settle to new common mode on 2.5 or 5.0 GT/s transition to 8.0 GT/s.

Table 13-13. Stressed Voltage Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator Launch Voltage	800	mVPP	Measured at TP1. Refer to the <i>PCI Express Base r3.0</i> , Figure 4-65. $V_{RX-LAUNCH-8G}$ can be adjusted, if necessary, to yield the proper EH, as long as the outside eye voltage at TP2 does not exceed 1,300 mVPP.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-SV-8G}$	Eye Height at TP2P	25 (-20 dB channel) 50 (-12 dB channel) 200 (-3 dB channel)	mVPP	Eye height at BER = 10^{-12} . Refer to Notes 1, 2.
$T_{RX-SV-8G}$	Eye Width at TP2P	0.3 to 0.35	UI	Eye width at BER = 10^{-12} . Refer to Note 2.
$V_{RX-SV-DIFF-8G}$	Differential Mode Interference	14 or greater	mVPP	Adjusted to Set EH. Frequency = 2.10 GHz. Refer to Note 3.
$V_{RX-SV-CM-8G}$	Rx AC Common Mode Voltage at TP2P	150 (EH < 100 mVPP) 250 (EH ≥ 100 mVPP)	mVPP	Defined for a single tone at 120 MHz. Refer to Note 3.
$T_{RX-SV-SJ-8G}$	Sinusoidal Jitter at 100 MHz	0.1	UI PP	Fixed at 100 MHz. Refer to Note 4.
$T_{RX-SV-RJ-8G}$	Random Jitter	2.0	ps RMS	Rj is spectrally flat before filtering. Refer to Notes 4, 5
$V_{RX-MAX-SE-SW}$	Maximum Single-Ended Swing	±300	mVP	Refer to Note 6.

Notes:

- $V_{RX-SV-8G}$ is tested at three different voltages, to ensure that the Rx DUT is capable of equalizing over a range of channel loss profiles. The test also guarantees that the Rx is capable of operating over a sufficient dynamic range of eye heights. “SV” in the parameter names refers to “stressed voltage”.
- $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ are referenced to TP2P, and are obtained after post processing data captured at TP2.

 $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ include the effects of applying the behavioral Rx model and Rx behavioral equalization.
- $V_{RX-SV-DIFF-8G}$ measurement is made at TP2, without post processing. $V_{RX-SV-CM-8G}$ can be made at either TP1 or TP2. $V_{RX-SV-DIFF-8G}$ voltage might need to be adjusted over a wide range for the different loss calibration channels.
- $T_{RX-SV-SJ-8G}$ and $T_{RX-SV-RJ-8G}$ measurements are made at TP1, without post processing.
- Rj is applied over the following range. The low frequency limit can be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. Refer to the *PCI Express Base r3.0*, Figure 4-74, for details.
- $V_{RX-MAX-SE-SW}$ sets the maximum outer, single-ended eye voltage limit in the presence of differential and CM noise applied to the Rx, as observed at TP2 relative to ground with no behavioral RxEq post processing.

Table 13-14. Stressed Jitter Eye Parameters

Symbol	Parameter	Limits at 8.0 GT/s	Units	Comments
$V_{RX-LAUNCH-8G}$	Generator Launch Voltage	800 (nominal)	mVPP	Measured at TP1. Refer to the <i>PCI Express Base r3.0</i> , Figure 4-65. Refer to Note 1.
$T_{RX-UI-8G}$	Unit Interval	125.00	ps	Nominal value is sufficient for Rx tolerancing. Value does not account for SSC.
$V_{RX-ST-8G}$	Eye height at TP2P	25 (min) 35 (max)	mVPP	At BER = 10^{-12} . Refer to Note 2.
$T_{RX-ST-8G}$	Eye width at TP2P	0.30	UI	At BER = 10^{-12} . Refer to Note 2.
$T_{RX-ST-SJ-8G}$	Sinusoidal Jitter	0.1 to 1.0	UI PP	Measured at TP1. Refer to the <i>PCI Express Base r3.0</i> , Figure 4-74. Refer to Note 3.
$T_{RX-ST-RJ-8G}$	Random Jitter	3.0	ps RMS	Rj spectrally flat before filtering. Measured at TP1. Refer to Note 4.

Notes:

1. $V_{RX-LAUNCH-8G}$ can be adjusted to meet $V_{RX-ST-8G}$, as long as the outside eye voltage at TP2 does not exceed 1,300 mVPP.
2. $V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ are referenced to TP2P, and are obtained after post processing data captured at TP2.

$V_{RX-ST-8G}$ and $T_{RX-ST-8G}$ include the effects of applying the behavioral Rx model and Rx behavioral equalization.

3. $T_{RX-ST-SJ-8G}$ can be measured at either TP1 or TP2.
4. While the nominal value is specified at 3.0 ps RMS, it can be adjusted to meet the 0.3 UI value for $T_{RX-ST-8G}$. Rj is measured at TP1, to prevent data-channel interaction from adversely affecting Rj calibration accuracy.

Rj is applied over the following range. The low-frequency limit can be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz.

14.1 Thermal Characteristics

Table 14-1. Sample Thermal Data, Commercial Temperature, with Heat Sink^a

Maximum Power (Watts) ^b	Air Flow Velocity (m/s)	Θ _{JA} (°C/W) JEDEC 4-Layer Board	Θ _{JA} (°C/W) JEDEC 8-Layer Board	Ψ _{JB} (°C/W) JEDEC 4-Layer Board	Ψ _{JB} (°C/W) JEDEC 8-Layer Board	Θ _{JC} (°C/W) JEDEC 4-Layer Board	Θ _{JC} (°C/W) JEDEC 8-Layer Board	Θ _{JB} (°C/W) JEDEC 4-Layer Board	Θ _{JB} (°C/W) JEDEC 8-Layer Board	Heat Sink
27 x 27 mm ² Package										
15.02	0.00	6.84	4.68	1.87	1.53	0.62	0.58	2.75	1.95	Aavid Thermalloy, 374324B60023G
	1.00	3.15	2.58	1.26	1.16					
	2.00	2.14	1.82	1.05	0.99					
19 x 21 mm ² Package										
15.02	0.00	9.05	5.51	2.19	1.88	0.61	0.61	3.57	2.4	Wakefield Solutions, 624-45ABT3
	1.00	4.89	3.57	1.56	1.48					
	2.00	3.35	2.7	1.26	1.25					

- a. The Maximum Operating Junction Temperature is 110°C.
The Maximum Junction Temperature for Reliability is 110°C.
- b. The maximum power value listed assumes the conditions listed in [Chapter 13, “Electrical Specifications,”](#) at Gen 3 (8.0 GT/s), with all Ports enabled.

14.2 General Package Specifications

Table 14-2 lists general specifications for the 27 x 27 mm² package. For a more complete list, refer to Figure 14-1.

Table 14-3 lists general specifications for the 19 x 21 mm² package. For a more complete list, refer to Figure 14-2 (with heat spreader) and Figure 14-3 (without heat spreader).

Table 14-2. General Package Specifications – 27 x 27 mm² Package

Parameter	Specification
Package Type	Flip-Chip Ball Grid Array with Heat Spreader (HFC-BGA)
Quantity of Balls	676
Package Dimensions	27 x 27 mm ² (approximately 2.55 ±0.25-mm high)
Ball Matrix Pattern	26 x 26
Ball Pitch	1.0 mm
Ball Diameter	0.60 ±0.1 mm
Ball Spacing	0.40 mm
Ball Pad Diameter	0.58 mm
Solder Mask Opening on Ball Pad	0.48 mm

Table 14-3. General Package Specifications – 19 x 21 mm² Package

Parameter	Specification	
	With Heat Spreader	Without Heat Spreader
Package Type	Flip-Chip Ball Grid Array with Heat Spreader (HFC-BGA)	Flip-Chip Ball Grid Array without Heat Spreader (FC-BGA)
Quantity of Balls	575	575
Package Dimensions	19.10 ±0.20 x 21 ±0.20 mm ² (approximately 2.46 ±0.25-mm high)	19.10 ±0.20 x 21 ±0.20 mm ² (approximately 1.92 ±0.25-mm high)
Ball Matrix Pattern	23 x 25	23 x 25
Ball Pitch	0.80 mm	0.80 mm
Ball Diameter	0.50 mm	0.50 mm
Ball Spacing	0.30 mm	0.30 mm
Solder Mask Opening on Ball Pad	0.40 mm	0.40 mm

14.3 Mechanical Dimensions

Figure 14-1. Mechanical Dimensions – 27 x 27 mm² Package with Heat Spreader

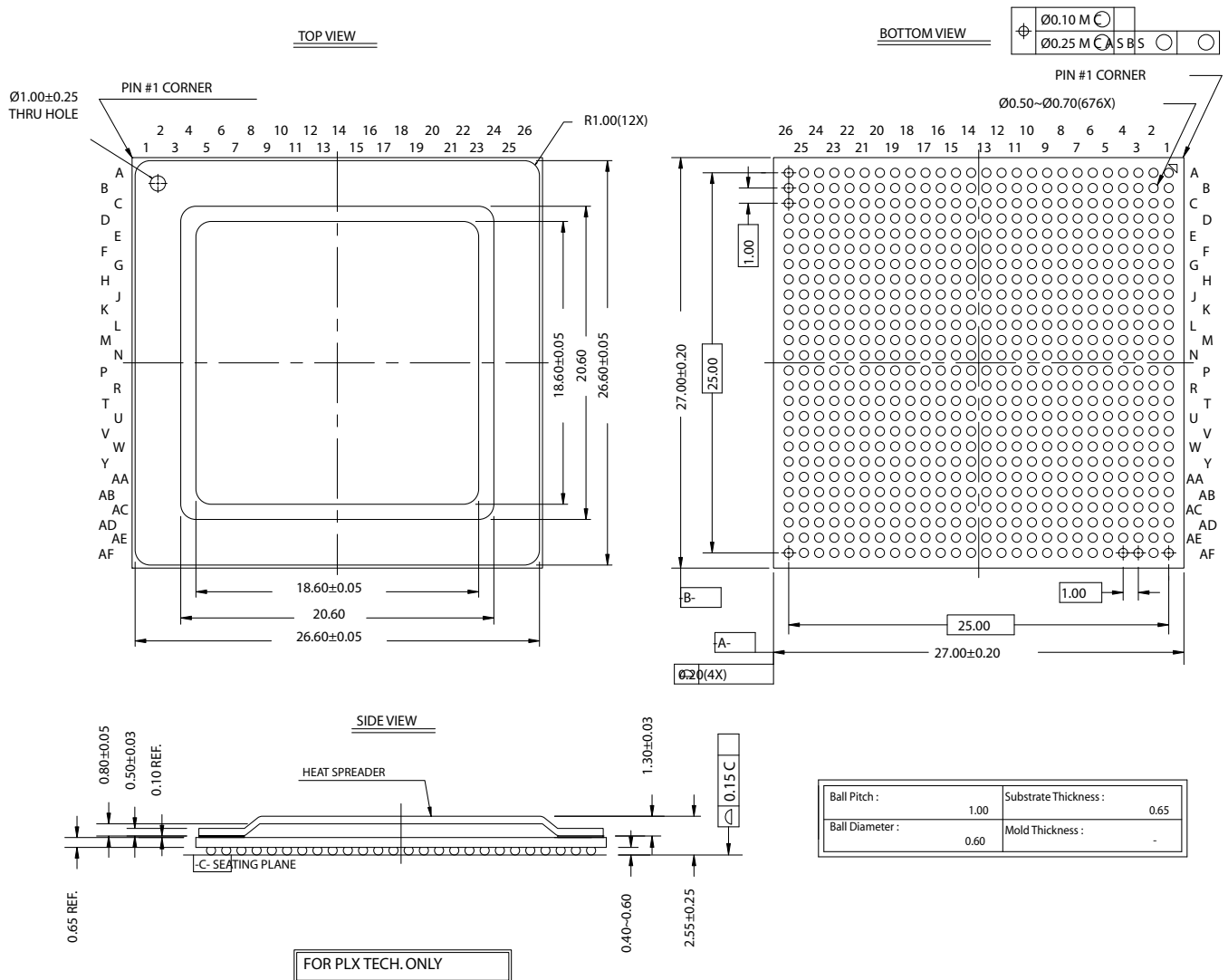


Figure 14-2. Mechanical Dimensions – 19 x 21 mm² Package with Heat Spreader

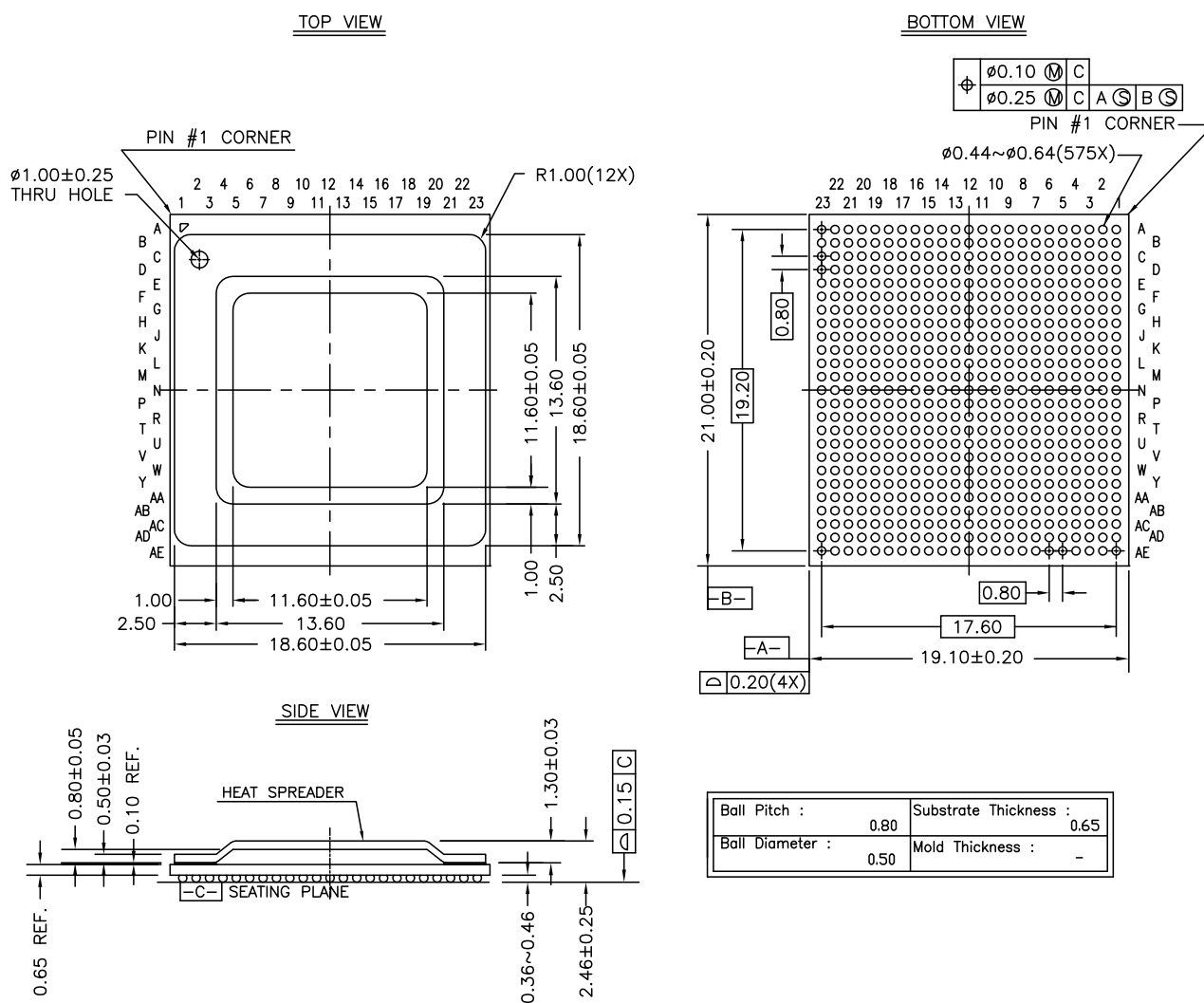
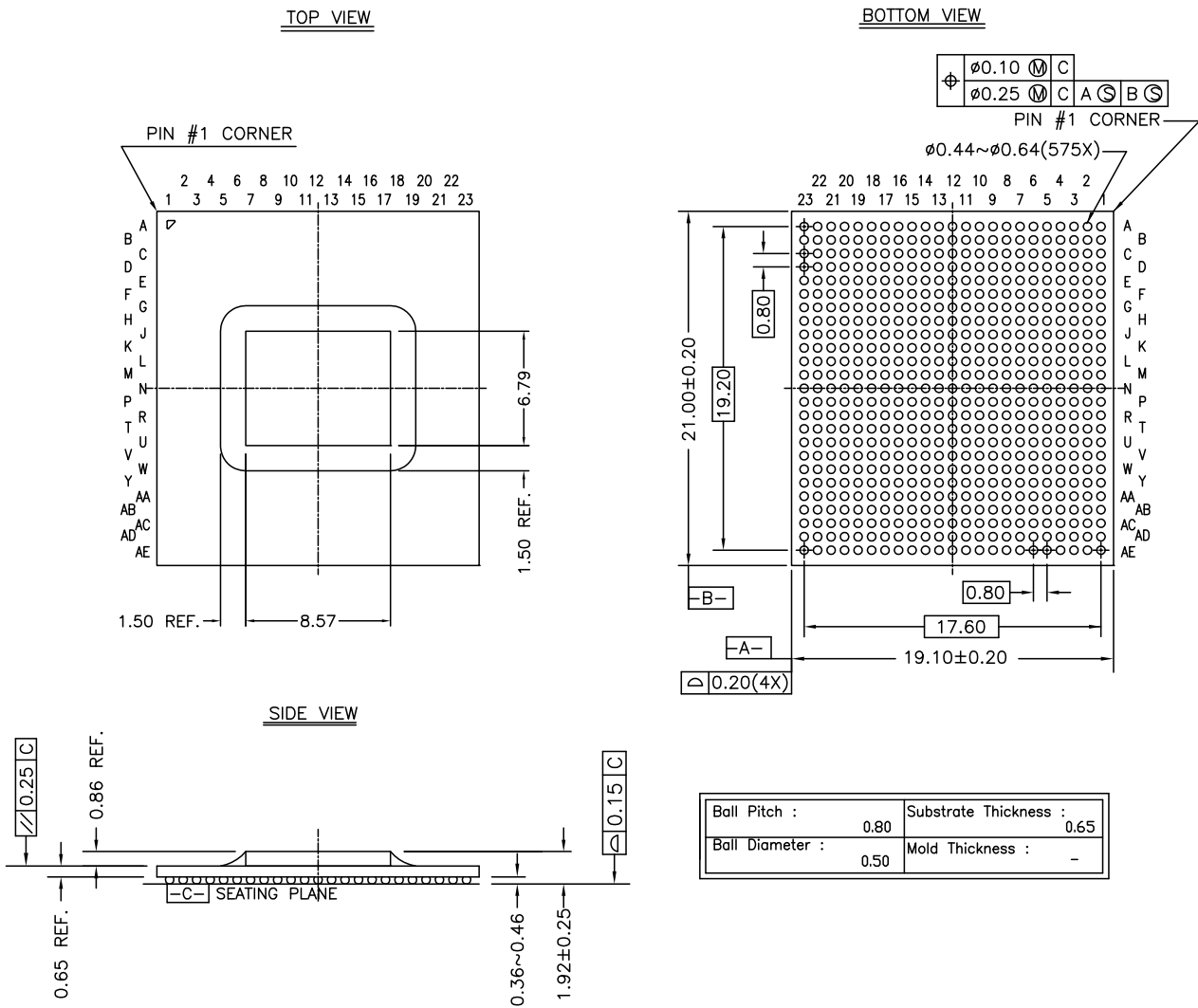


Figure 14-3. Mechanical Dimensions – 19 x 21 mm² Package without Heat Spreader

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Appendix A General Information

A.1 Product Ordering Information

Contact your local [PLX Sales Representative](#) for ordering information.

Table A-1. Product Ordering Information

Part Numbers	Description
PEX8747-BA80BC G PEX8747-CA80BC G	PEX 8747 48-Lane, 5-Port PCI Express Gen 3 Switch Lead-Free HFC-BGA Package (27 x 27 mm ² , 676-ball)
PEX8747-BA80FBC G PEX8747-CA80FBC G	PEX 8747 48-Lane, 5-Port PCI Express Gen 3 Switch Lead-Free Fine-Pitch HFC-BGA Package (19 x 21 mm ² , 575-ball)
PEX8747-BA80BFBC G PEX8747-CA80BFBC G	PEX 8747 48-Lane, 5-Port PCI Express Gen 3 Switch Lead-Free Fine-Pitch FC-BGA Package (19 x 21 mm ² , 575-ball)
<i>where</i>	PEX – PCI Express Product Family 8747 – Part Number BA, CA – Silicon Revision 80 – Signaling Rate (8.0 GT/s) B – Flip-Chip Ball Grid Array F – Fine-Pitch (both 19 x 21 mm ² packages only) B – Without Heat Spreader (19 x 21 mm ² FC-BGA package only) C – Commercial Temperature G – Lead-free (RoHS 6/6 and Green compliant)
PEX 8747-BA RDK	PEX 8747 Rapid Development Kit with x16 Edge Connector (27 x 27 mm ² package)
PEX 8747-CA RDK	PEX 8747 Rapid Development Kit with x16 Edge Connector (27 x 27 mm ² package)
x1 Adapter	PCI Express x16 to x1 Adapter
x4 Adapter	PCI Express x16 to x4 Adapter
x8 Adapter	PCI Express x16 to x8 Adapter

A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

PLX Technology, Inc., technical support information is listed at www.plxtech.com/support, or call 800 759-3735 (domestic only) or 408 774-9060.