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056 CPU2\_DDR4\_CH\_I2  
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059 CPU2\_DDR4\_CH\_K1  
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064 CPU2\_DDR4\_CH\_M2  
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067 CPU2\_DDR4\_CH\_O1  
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071 NVDIMM1  
072 CPU\_Sideband1  
073 CPU\_Sideband2  
074 CPU\_Sideband3  
075 CPU\_Sideband4  
076 Blank  
077 === PCH ===  
078 PCH\_isCLK  
079 PCH\_MISC\_MAC  
080 PCH\_DMI/PCIE/USB3/UPLINK  
081 PCH\_LPC\_SMB\_SGPIO  
082 PCH\_SPI\_RTC\_NCSI  
083 PCH\_POWER  
084 PCH\_GND  
085 PCH\_PU/PD  
086 PCH\_STRAP  
087 PCH\_HEADER/JUMPER  
088 ESPI/LPC/SMBUS  
089 EULOT6  
090 BOARD\_IDS  
091SMBUS  
092 Blank  
093 ===CLK Buffer ===  
094 CLK\_Buffer0  
095 CLK\_Buffer1  
096 Blank  
097 === BMC ===  
098 BMC-DDR/SMB/SD/ESPI/PCIE  
099 BMC-SPI/UART/MAC/ACPI  
100 BMC-VGA/ADC/PECI/FAN/USB  
101 BMC-Power  
102 BMC-DDR4  
103 FRU/THERMAL SENSOR  
104 HEADER/JUMPER  
105 BMC\_SMB\_MUX  
106 Blank  
107 Blank  
108 === CPLD ===  
109 CPLD-1  
110 CPLD-2  
111 CPLD-3  
112 PE\_DEVICE\_THROTTLE  
113 Blank  
114 Blank  
115 === PCIE ===  
116 PCIE\_SLOT1(X32)  
117 PCIE\_SLOT2(X32)  
118 PCIE\_SLOT3(X16)  
119 SLIMLINE\_PERST\_LOGIC  
120 Blank  
121 MICRO\_SD  
122 M.2 E-KEY  
123 Blank  
124 M.2\_1(X4)  
125 M.2\_2(X4)  
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127 Slimline1  
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130 Slimline4  
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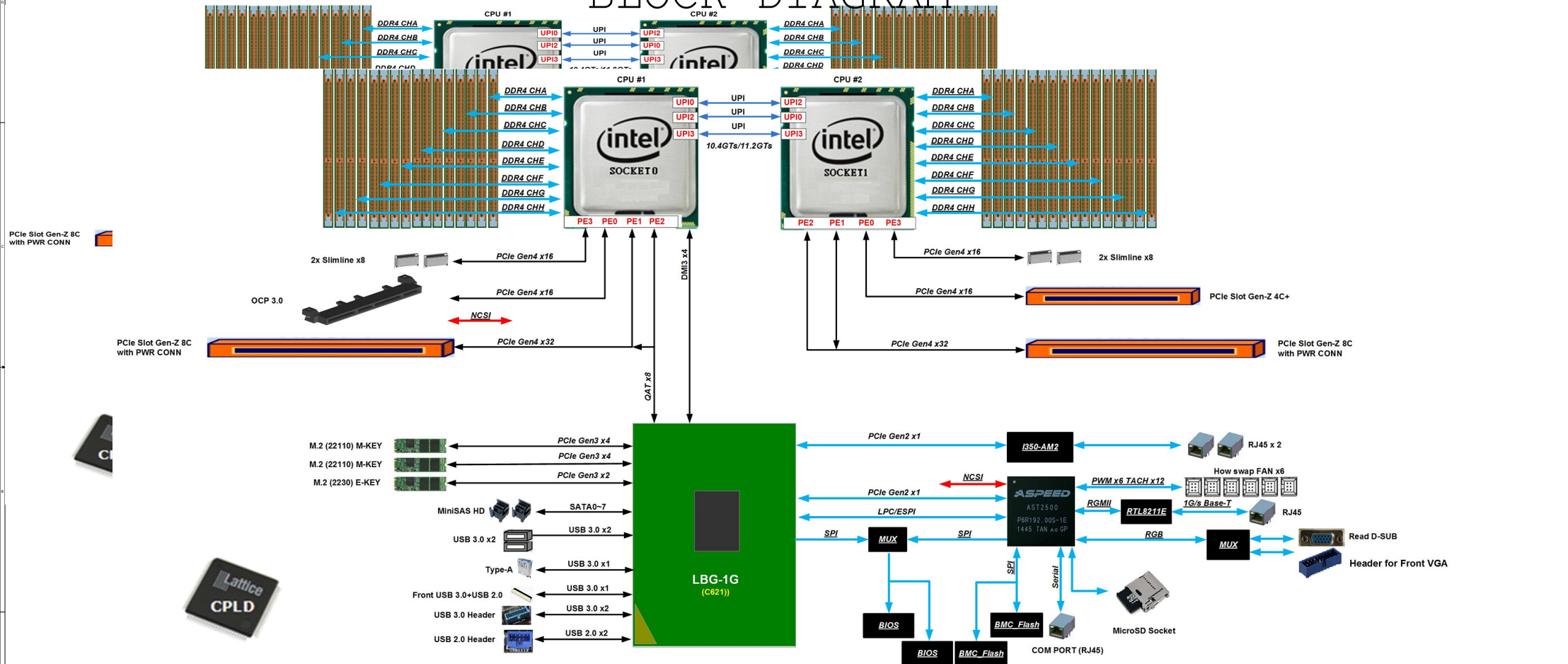
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137 LAN\_I350  
138 LAN\_I350\_PORT  
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143 Blank  
144 Blank  
145 Blank  
146 === SATA & SAS ===  
147 SATA\_DOM&Mimi\_SAS  
148 Blank  
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150 ===I/O & HEADER ===  
151 BAT & CLR\_MOS  
152 8211\_IPMI\_LAN  
153 SPEAKER  
154 FRONT\_PANEL  
155 AUX\_PANEL  
156 COM\_VGA\_PORT  
157 REAR\_USB\_CONN  
158 FRONT\_USB\_CONN  
159 FAN  
160 FAN\_1U  
161 HSBP\_PWR\_CONNECTOR  
162 CRPS\_POWER\_CONN1  
163 CRPS\_POWER\_CONN2  
164 Blank  
165 Blank  
166 Blank  
167 Blank  
168 === PFR\_FLASH ===  
169 PCH/BMC/PFR\_BIOS\_SPI\_MUX\_1  
170 PCH/BMC/ROT\_SPI\_MUX\_2  
171 BIOS\_Flash  
172 BMC\_Flash  
173 Blank  
174 Blank  
175 === XDP ===  
176 XDP  
177 XDP\_MUX\_1  
178 XDP\_MUX\_2  
179 XDP\_BP  
180 Blank  
181 Blank  
182 === OTHERS ===  
183 SCREW\_HOLE  
184 COUPON  
185 VR\_TEST\_PIN  
186 Blank  
187 Blank  
188 Blank  
189 Blank  
190 Blank  
191 Blank  
192 Blank  
193 Blank  
194 === OtherPower ===  
195 12V\_AUX  
196 3VSB\_BAT(AP431)  
197 5VSB/3VSB(TPS53355)  
198 BMC\_2V5(TPS74810)

199 BMC\_1V2(TPS62130)  
200 BMC\_1V15(TPS62130)  
201 PCH\_1V8(TPS62130)  
202 PCH\_PVNN(TPS53355)  
203 PCH\_1V05(TPS53353)  
204 OCP3.0\_HSWP  
205 5V/3V(MOS-SWITCH)  
206 === CPU1\_DIMM ===  
207 ABCD\_VCCM+VPP(PXE1410C)  
208 ABCD\_SPS\_VCCM(TDA21462)  
209 ABCD\_SPS\_VPPM(TDA21462)  
210 ABCD\_POL\_VTTM(MP8626)  
211 ABCD\_CAP\_VCCM\_VPP+VTT  
212 EFGH\_VCCM+VPP(PXE1410C)  
213 EFGH\_SPS\_VCCM(TDA21462)  
214 EFGH\_SPS\_VTTM(TDA21462)  
215 EFGH\_POL\_VTTM(MP8626)  
216 EFGH\_CAP\_VCCM+VPP+VTT  
217 === CPU1\_VCORE ===  
218 CPU1\_VCCIO(PXE1410C)  
219 CPU1\_SPS\_VCCIO(TDA21462)  
220 CPU1\_CAP\_VCCIO  
221 CPU1\_VCC1P8+VCCANA(PXE1410)  
222 CPU1\_SPS\_VCC1P8(TDA21462)  
223 CPU1\_SPS\_VCCANA(TDA21462)  
224 CPU1\_CAP\_VCC1V8+VCCANA  
225 CPU1\_VCCIN+VCCSA(XDPE12284)  
226 CPU1\_SPS1~3\_VCCIN(TDA21490)  
227 CPU1\_SPS4~7\_VCCIN(TDA21490)  
228 CPU1\_SPS\_VCCSA(TDA21462)  
229 CPU1\_CAP\_VCCIN\_VCCSA  
230 === CPU2\_DIMM ===  
231 IJKL\_VCCM+VPP(PXE1410C)  
232 IJKL\_SPS\_VCCM(TDA21462)  
233 IJKL\_CAP\_VCCM+VPP+VTT  
234 IJKL\_POL\_VTTM(MP8626)  
235 IJKL\_SPS\_VPPM(TDA21462)  
236 MNOP\_VCCM+VPP(PXE1410C)  
237 MNOP\_SPS\_VCCM(TDA21462)  
238 MNOP\_SPS\_VPPM(TDA21462)  
239 MNOP\_POL\_VTTM(MP8626)  
240 EFGH\_CAP\_VCCM+VPP+VTT  
241 === CPU2\_VCORE ===  
242 CPU2\_VCCIO(PXE1410C)  
243 CPU2\_SPS\_VCCIO(TDA21462)  
244 CPU2\_CAP\_VCCIO  
245 CPU2\_VCC1P8+VCCANA(PXE1410)  
246 CPU2\_SPS\_VCC1P8(TDA21462)  
247 CPU2\_SPS\_VCCANA(TDA21462)  
248 CPU2\_CAP\_VCC1V8+VCCANA  
249 CPU2\_VCCIN+VCCSA(XDPE12284)  
250 CPU2\_SPS1~3\_VCCIN(TDA21490)  
251 CPU2\_SPS4~7\_VCCIN(TDA21490)  
252 CPU2\_SPS\_VCCSA(TDA21462)  
253 CPU2\_CAP\_VCCIN\_VCCSA

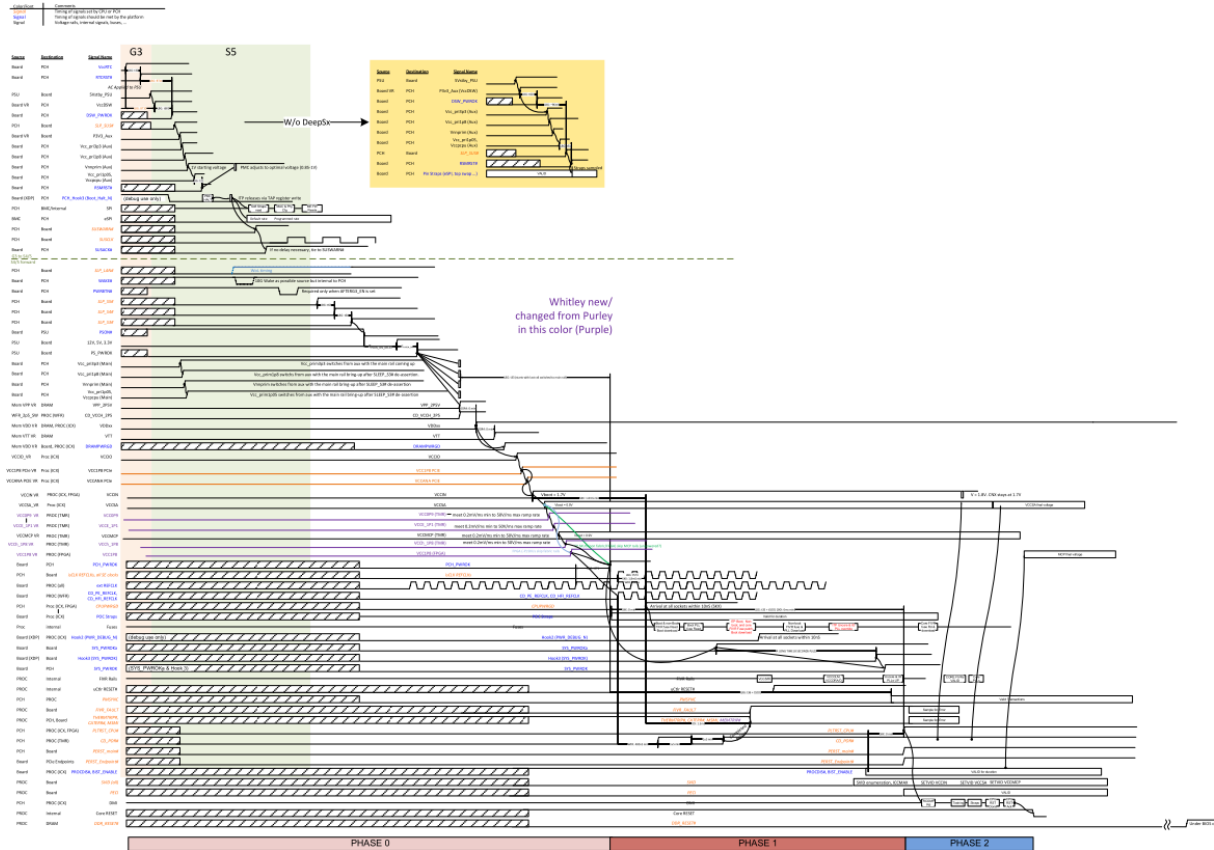
DPC621-BV

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# BLOCK DIAGRAM



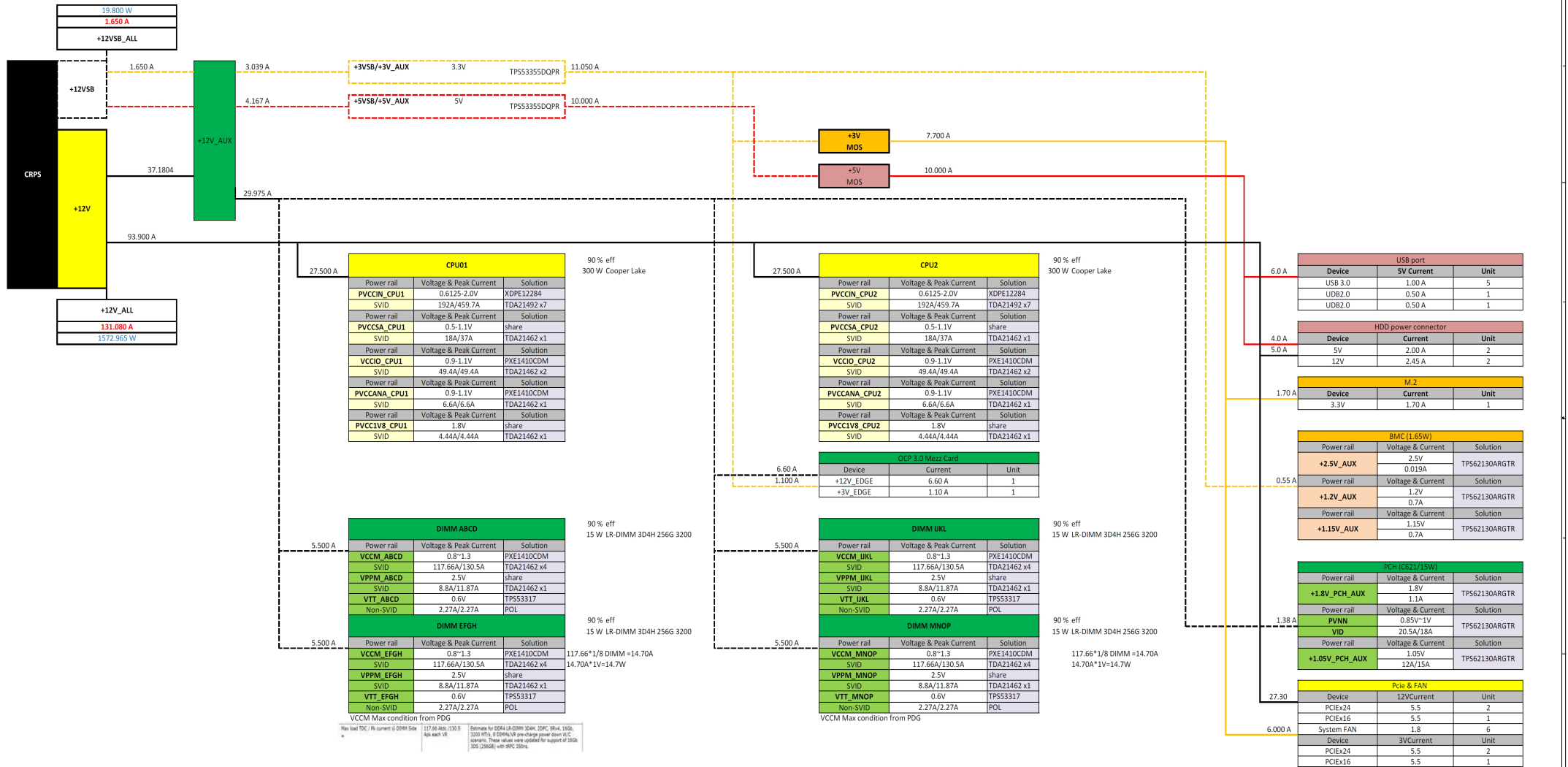
# Power Sequence



Reference: CRB-wilson-city p.10





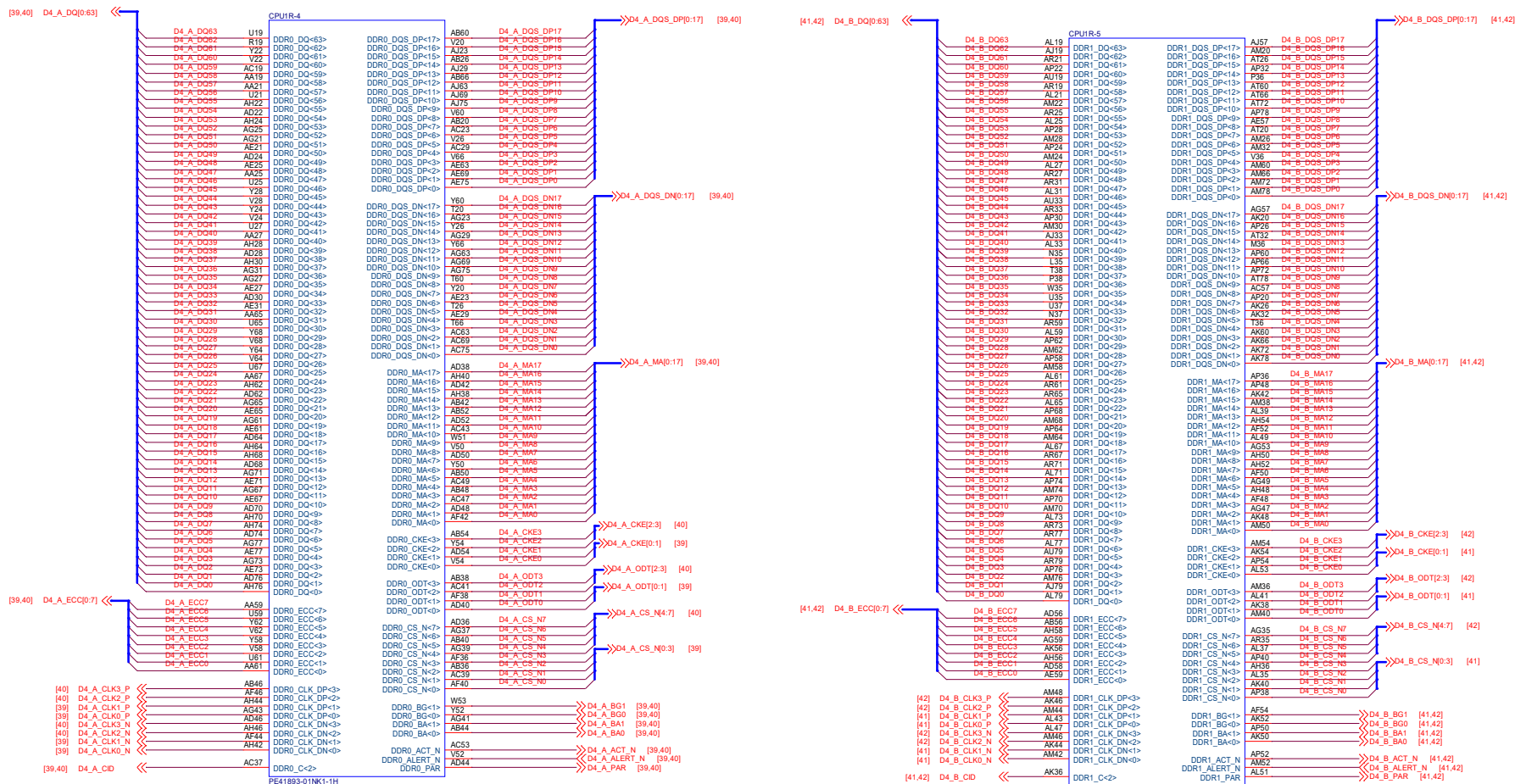


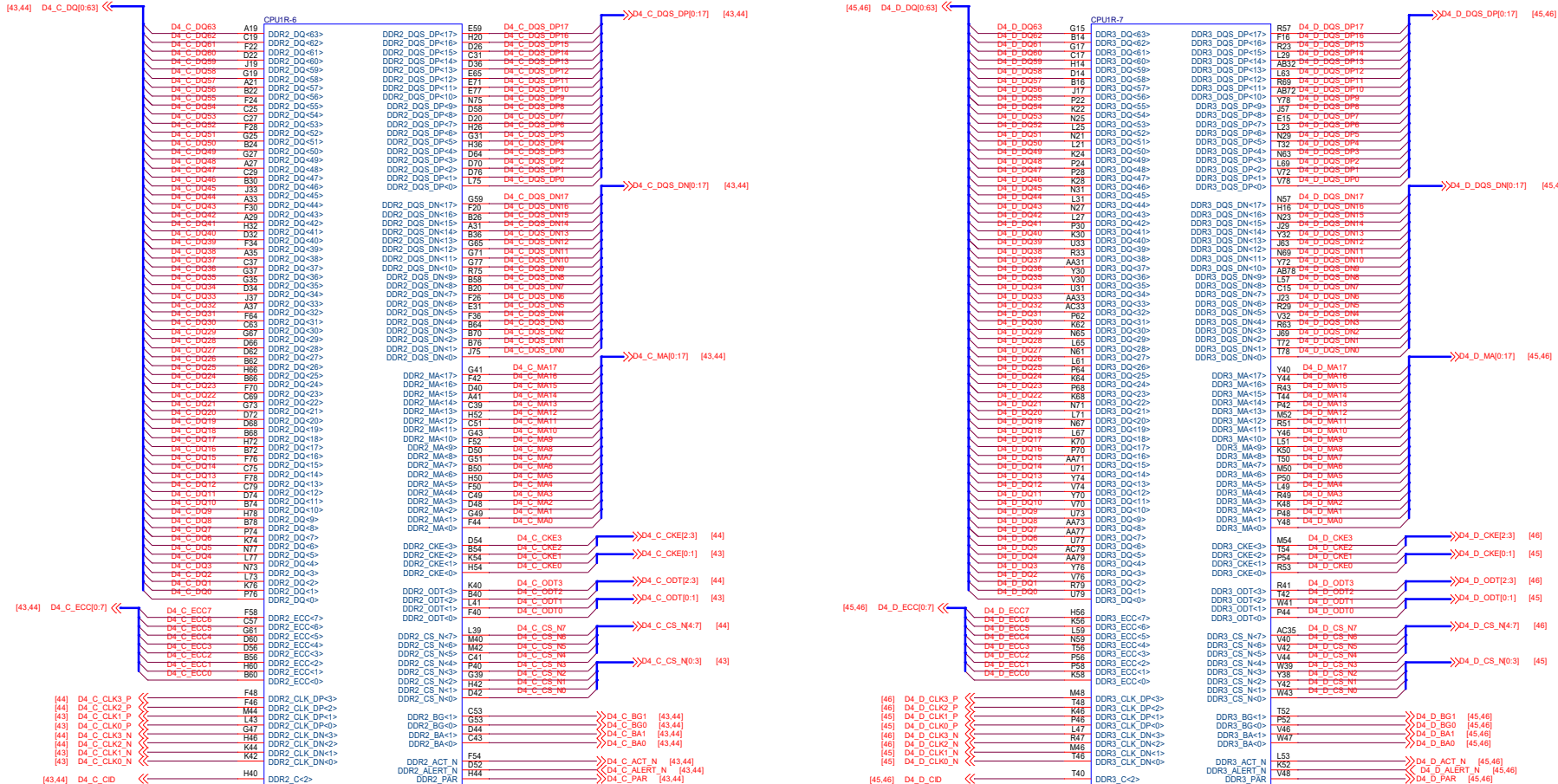


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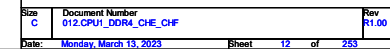
===CPU & DIMM===



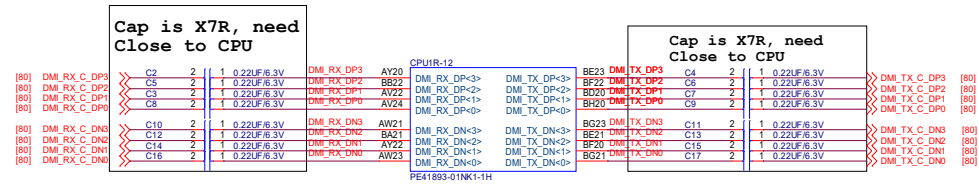












PE0 A X16 connect to OCP3.0 conn

PE1 A x16 connect to PCIe Slot x32 (RISER1)

PE_C0PU1_P0TA_RS0R1_TX_DP15	C19	2	1	0.22U/6.3V	
PE_C0PU1_P0TA_RS0R1_TX_DP14	C21	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP15 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP13	C23	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP14 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP12	C25	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP13 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP11	C27	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP12 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP10	C29	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP11 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP09	C31	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP10 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP08	C33	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP09 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP07	C35	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP08 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP06	C37	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP07 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP05	C39	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP06 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP04	C41	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP05 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP03	C43	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP04 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP02	C45	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP03 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP01	C47	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP02 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP00	C49	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP01 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP15	C51	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP15 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP14	C53	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP14 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP13	C55	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP13 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP12	C57	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP12 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP11	C59	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP11 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP10	C61	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP10 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP09	C63	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP09 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP08	C65	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP08 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP07	C67	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP07 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP06	C69	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP06 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP05	C71	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP05 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP04	C73	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP04 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP03	C75	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP03 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP02	C77	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP02 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP01	C79	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP01 (116)
PE_C0PU1_P0TA_RS0R1_TX_DP00	C81	2	1	0.22U/6.3V	▶PE_C0PU1_P0TA_RS0R1_C_TX_DP00 (116)

	P4E_CPU01	PE2B_RISER1	RX_DP6	DM2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2B_RISER1	RX_DP7	DH2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2B_RISER1	RX_DP8	DH2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2B_RISER1	RX_DP9	DF2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2B_RISER1	RX_DP10	DF2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2B_RISER1	RX_DP11	CY2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2A_RISER1	RX_DP12	CB2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2A_RISER1	RX_DP13	CV2	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2A_RISER1	RX_DP14	G12	PE2_RX_DP<P>	PE2_TX_DP<P>
(1)16	P4E_CPU01	PE2A_RISER1	RX_DP15	G12	PE2_RX_DP<P>	PE2_TX_DP<P>

[127]	P4E_CPU1_PES3_SLM0_RX_DP8	DG87	P3E_RX_DP-8
[126]	P4E_CPU1_PES3_SLM0_RX_DP7	DE87	P3E_RX_DP-7
[125]	P4E_CPU1_PES3_SLM0_RX_DP6	DC87	P3E_RX_DP-6
[124]	P4E_CPU1_PES3_SLM0_RX_DP5	DA87	P3E_RX_DP-5
[123]	P4E_CPU1_PES3_SLM0_RX_DP4	CW87	P3E_RX_DP-4
[122]	P4E_CPU1_PES3_SLM0_RX_DP3	CU87	P3E_RX_DP-3
[121]	P4E_CPU1_PES3_SLM0_RX_DP2	CB87	P3E_RX_DP-2
[120]	P4E_CPU1_PES3_SLM0_RX_DP1	CA87	P3E_RX_DP-1
[119]	P4E_CPU1_PES3_SLM0_RX_DP0	CM84	P3E_RX_DP-0

PE2 A-D x16 connect to PCIe Slot x32 (RISER1)  
PE2 C-D x8 connect to PCIe Slot or PCH (QAT)

```
PE3 A x4 connect to Slimline4
PE3 B x4 connect to Slimline3
PE3 C x4 connect to Slimline2
PE3 D x4 connect to Slimline1
```

P4E_CPU1_PE2B_RISER1_TX_0N7	C103	2	1	0.22UF/6.3V			
P4E_CPU1_PE2B_RISER1_TX_DN6	C109	2	1	0.22UF/6.3V			
P4E_CPU1_PE2B_RISER1_TX_DN5	C109	2	1	0.22UF/6.3V			
P4E_CPU1_PE2B_RISER1_TX_DN4	C109	2	1	0.22UF/6.3V			
P4E_CPU1_PE2A_RISER1_TX_DN3	C110	2	1	0.22UF/6.3V			
P4E_CPU1_PE2A_RISER1_TX_DN2	C112	2	1	0.22UF/6.3V			
P4E_CPU1_PE2A_RISER1_TX_DN1	C114	2	1	0.22UF/6.3V			
P4E_CPU1_PE2A_RISER1_TX_DN0	C116	2	1	0.22UF/6.3V			
P4E_CPU1_PE2B_RISER1_C_TX_DN7							[116]
P4E_CPU1_PE2B_RISER1_C_TX_DN6							[116]
P4E_CPU1_PE2B_RISER1_C_TX_DN5							[116]
P4E_CPU1_PE2B_RISER1_C_TX_DN4							[116]
P4E_CPU1_PE2A_RISER1_C_TX_DN3							[116]
P4E_CPU1_PE2A_RISER1_C_TX_DN2							[116]
P4E_CPU1_PE2A_RISER1_C_TX_DN1							[116]
P4E_CPU1_PE2A_RISER1_C_TX_DN0							[116]

PE2 C-D x8 connect to Slimline1

P4E_CPU1_P2D2_RISER1_C_TX_DN15	C146	2	1	0.22UF/6.3V	P4E_CPU1_P2D2_RISER1_C_TX_DN15	[116]
P4E_CPU1_P2D2_RISER1_C_TX_DN14	C147	2	1	0.22UF/6.3V	P4E_CPU1_P2D2_RISER1_C_TX_DN14	[116]
P4E_CPU1_P2D2_RISER1_C_TX_DN13	C148	2	1	0.22UF/6.3V	P4E_CPU1_P2D2_RISER1_C_TX_DN13	[116]
P4E_CPU1_P2D2_RISER1_C_TX_DN12	C151	2	1	0.22UF/6.3V	P4E_CPU1_P2D2_RISER1_C_TX_DN12	[116]
P4E_CPU1_P2D2_RISER1_C_TX_DN11	C153	2	1	0.22UF/6.3V	P4E_CPU1_P2D2_RISER1_C_TX_DN11	[116]
P4E_CPU1_P2C2_RISER1_C_TX_DN10	C155	2	1	0.22UF/6.3V	P4E_CPU1_P2C2_RISER1_C_TX_DN10	[116]
P4E_CPU1_P2C2_RISER1_C_TX_DN9	C157	2	1	0.22UF/6.3V	P4E_CPU1_P2C2_RISER1_C_TX_DN9	[116]
P4E_CPU1_P2C2_RISER1_C_TX_DN8	C159	2	1	0.22UF/6.3V	P4E_CPU1_P2C2_RISER1_C_TX_DN8	[116]

PE2 C-D x8 connect to PCH (QAT)

PAE_CPU1_P2D0_RISER1_TX_DP15	XC132	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DP15	
PAE_CPU1_P2D0_RISER1_TX_DP16	XC134	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DP16	
PAE_CPU1_P2D0_RISER1_TX_DP17	XC135	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DP17	
PAE_CPU1_P2D0_RISER1_TX_DP18	XC136	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DP18	
PAE_CPU1_P2C0_RISER1_TX_DP11	XC140	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP11	
PAE_CPU1_P2C0_RISER1_TX_DP12	XC141	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP12	
PAE_CPU1_P2C0_RISER1_TX_DP13	XC142	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP13	
PAE_CPU1_P2C0_RISER1_TX_DP14	XC143	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP14	
PAE_CPU1_P2C0_RISER1_TX_DP15	XC144	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP15	
PAE_CPU1_P2C0_RISER1_TX_DP16	XC145	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP16	
PAE_CPU1_P2C0_RISER1_TX_DP17	XC146	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP17	
PAE_CPU1_P2C0_RISER1_TX_DP18	XC147	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DP18	
PAE_CPU1_P2D0_RISER1_TX_DM15	XC148	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DM15	
PAE_CPU1_P2D0_RISER1_TX_DM16	XC149	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DM16	
PAE_CPU1_P2D0_RISER1_TX_DM17	XC150	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DM17	
PAE_CPU1_P2D0_RISER1_TX_DM18	XC151	0.22UF/6.3V	>=ME_CPU1_P2D0_PCH_C_TX_DM18	
PAE_CPU1_P2C0_RISER1_TX_DM11	XC152	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM11	
PAE_CPU1_P2C0_RISER1_TX_DM12	XC153	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM12	
PAE_CPU1_P2C0_RISER1_TX_DM13	XC154	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM13	
PAE_CPU1_P2C0_RISER1_TX_DM14	XC155	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM14	
PAE_CPU1_P2C0_RISER1_TX_DM15	XC156	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM15	
PAE_CPU1_P2C0_RISER1_TX_DM16	XC157	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM16	
PAE_CPU1_P2C0_RISER1_TX_DM17	XC158	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM17	
PAE_CPU1_P2C0_RISER1_TX_DM18	XC159	0.22UF/6.3V	>=ME_CPU1_P2C0_PCH_C_TX_DM18	

[80]	P4E_CPU1_P#2D_PCH_C_RX_DN15	JXC162	0.22UF/6.3V	P4E_CPU1_P#2D_RS1R1_RX_DN15
[80]	P4E_CPU1_P#2D_PCH_C_RX_DN14	JXC163	0.22UF/6.3V	P4E_CPU1_P#2D_RS1R1_RX_DN14
[80]	P4E_CPU1_P#2D_PCH_C_RX_DN13	JXC164	0.22UF/6.3V	P4E_CPU1_P#2D_RS1R1_RX_DN13
[80]	P4E_CPU1_P#2D_PCH_C_RX_DN12	JXC165	0.22UF/6.3V	P4E_CPU1_P#2D_RS1R1_RX_DN12
[80]	P4E_CPU1_P#2C_PCH_C_RX_DN11	JXC166	0.22UF/6.3V	P4E_CPU1_P#2C_RS1R1_RX_DN11
[80]	P4E_CPU1_P#2C_PCH_C_RX_DN10	JXC167	0.22UF/6.3V	P4E_CPU1_P#2C_RS1R1_RX_DN10
[80]	P4E_CPU1_P#2C_PCH_C_RX_DN8	JXC168	0.22UF/6.3V	P4E_CPU1_P#2C_RS1R1_RX_DN8
[80]	P4E_CPU1_P#2C_PCH_C_RX_DN8	JXC169	0.22UF/6.3V	P4E_CPU1_P#2C_RS1R1_RX_DN8

[80]	P4E_CPU1_P2DZ_PCH_C_RX_DP15	ICX170	0.22U/6.3V	P4E_CPU1_P2DZ_RSISRI_RX_DP15
[80]	P4E_CPU1_P2DZ_PCH_C_RX_DP14	ICX171	0.22U/6.3V	P4E_CPU1_P2DZ_RSISRI_RX_DP14
[80]	P4E_CPU1_P2DZ_PCH_C_RX_DP13	ICX172	0.22U/6.3V	P4E_CPU1_P2DZ_RSISRI_RX_DP13
[80]	P4E_CPU1_P2DZ_PCH_C_RX_DP12	ICX173	0.22U/6.3V	P4E_CPU1_P2DZ_RSISRI_RX_DP12
[80]	P4E_CPU1_P2DZ_PCH_C_RX_DP12	ICX174	0.22U/6.3V	P4E_CPU1_P2CZ_RSISRI_RX_DP11
[80]	P4E_CPU1_P2CZ_PCH_C_RX_DP11	ICX175	0.22U/6.3V	P4E_CPU1_P2CZ_RSISRI_RX_DP10
[80]	P4E_CPU1_P2CZ_PCH_C_RX_DP10	ICX176	0.22U/6.3V	P4E_CPU1_P2CZ_RSISRI_RX_DP9
[80]	P4E_CPU1_P2CZ_PCH_C_RX_DP8	ICX177	0.22U/6.3V	P4E_CPU1_P2CZ_RSISRI_RX_DP8

RAE_CPU1_PES3D_SLIM.TX_DP15	C82	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP15	(127)
RAE_CPU1_PES3D_SLIM.TX_DP14	C83	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP14	(127)
RAE_CPU1_PES3D_SLIM.TX_DP13	C85	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP13	(127)
RAE_CPU1_PES3D_SLIM.TX_DP12	C86	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP12	(127)
RAE_CPU1_PES3D_SLIM.TX_DP11	C87	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP11	(127)
RAE_CPU1_PES3D_SLIM.TX_DP10	C81	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP10	(127)
RAE_CPU1_PES3D_SLIM.TX_DP9	C82	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP9	(127)
RAE_CPU1_PES3D_SLIM.TX_DP8	C85	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP8	(127)
RAE_CPU1_PES3D_SLIM.TX_DP7	C87	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP7	(128)
RAE_CPU1_PES3D_SLIM.TX_DP6	C100	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP6	(128)
RAE_CPU1_PES3D_SLIM.TX_DP5	C101	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP5	(128)
RAE_CPU1_PES3D_SLIM.TX_DP4	C102	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP4	(128)
RAE_CPU1_PES3D_SLIM.TX_DP3	C104	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP3	(128)
RAE_CPU1_PES3D_SLIM.TX_DP2	C105	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP2	(128)
RAE_CPU1_PES3D_SLIM.TX_DP1	C106	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP1	(128)
RAE_CPU1_PES3D_SLIM.TX_DP0	C112	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DP0	(128)
RAE_CPU1_PES3D_SLIM.TX_DN15	C112	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN15	(127)
RAE_CPU1_PES3D_SLIM.TX_DN14	C113	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN14	(127)
RAE_CPU1_PES3D_SLIM.TX_DN13	C114	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN13	(127)
RAE_CPU1_PES3D_SLIM.TX_DN12	C117	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN12	(127)
RAE_CPU1_PES3D_SLIM.TX_DN11	C118	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN11	(127)
RAE_CPU1_PES3D_SLIM.TX_DN10	C119	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN10	(127)
RAE_CPU1_PES3D_SLIM.TX_DN9	C120	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN9	(127)
RAE_CPU1_PES3D_SLIM.TX_DN8	C121	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN8	(127)
RAE_CPU1_PES3D_SLIM.TX_DN7	C122	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN7	(128)
RAE_CPU1_PES3D_SLIM.TX_DN6	C123	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN6	(128)
RAE_CPU1_PES3D_SLIM.TX_DN5	C124	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN5	(128)
RAE_CPU1_PES3D_SLIM.TX_DN4	C125	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN4	(128)
RAE_CPU1_PES3D_SLIM.TX_DN3	C126	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN3	(128)
RAE_CPU1_PES3D_SLIM.TX_DN2	C127	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN2	(128)
RAE_CPU1_PES3D_SLIM.TX_DN1	C128	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN1	(128)
RAE_CPU1_PES3D_SLIM.TX_DN0	C129	2	1	0.22U/F-3V	>>>RAE_CPU1_PES3D_SLIM.C.TX_DN0	(128)



CPU1R-17			
(32)	UPL CPU2_CPU1_P2P0_DP19	T16	UPL0_RX_DP<19> UPL0_TX_DP<19>
(32)	UPL CPU2_CPU1_P2P0_DP18	N15	UPL0_RX_DP<18> UPL0_TX_DP<18>
(32)	UPL CPU2_CPU1_P2P0_DP17	M14	UPL0_RX_DP<17> UPL0_TX_DP<17>
(32)	UPL CPU2_CPU1_P2P0_DP16	R15	UPL0_RX_DP<16> UPL0_TX_DP<16>
(32)	UPL CPU2_CPU1_P2P0_DP15	V14	UPL0_RX_DP<15> UPL0_TX_DP<15>
(32)	UPL CPU2_CPU1_P2P0_DP14	AX15	UPL0_RX_DP<14> UPL0_TX_DP<14>
(32)	UPL CPU2_CPU1_P2P0_DP13	AB14	UPL0_RX_DP<13> UPL0_TX_DP<13>
(32)	UPL CPU2_CPU1_P2P0_DP12	AG15	UPL0_RX_DP<12> UPL0_TX_DP<12>
(32)	UPL CPU2_CPU1_P2P0_DP11	AD14	UPL0_RX_DP<11> UPL0_TX_DP<11>
(32)	UPL CPU2_CPU1_P2P0_DP10	AG13	UPL0_RX_DP<10> UPL0_TX_DP<10>
(32)	UPL CPU2_CPU1_P2P0_DP9	AF14	UPL0_RX_DP<9> UPL0_TX_DP<9>
(32)	UPL CPU2_CPU1_P2P0_DP8	AL15	UPL0_RX_DP<8> UPL0_TX_DP<8>
(32)	UPL CPU2_CPU1_P2P0_DP7	AK14	UPL0_RX_DP<7> UPL0_TX_DP<7>
(32)	UPL CPU2_CPU1_P2P0_DP6	AN15	UPL0_RX_DP<6> UPL0_TX_DP<6>
(32)	UPL CPU2_CPU1_P2P0_DP5	AT14	UPL0_RX_DP<5> UPL0_TX_DP<5>
(32)	UPL CPU2_CPU1_P2P0_DP4	AJ17	UPL0_RX_DP<4> UPL0_TX_DP<4>
(32)	UPL CPU2_CPU1_P2P0_DP3	AP16	UPL0_RX_DP<3> UPL0_TX_DP<3>
(32)	UPL CPU2_CPU1_P2P0_DP2	AUT7	UPL0_RX_DP<2> UPL0_TX_DP<2>
(32)	UPL CPU2_CPU1_P2P0_DP1	AN17	UPL0_RX_DP<1> UPL0_TX_DP<1>
(32)	UPL CPU2_CPU1_P2P0_D0		UPL0_RX_DP<0> UPL0_TX_DP<0>

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CPU1R-19			
(32)	UPL CPU2_CPU1_P0P2_DP19	ED12	UPL2_RX_DP<19> UPL2_TX_DP<19>
(32)	UPL CPU2_CPU1_P0P2_DP18	EB11	UPL2_RX_DP<18> UPL2_TX_DP<18>
(32)	UPL CPU2_CPU1_P0P2_DP17	EC13	UPL2_RX_DP<17> UPL2_TX_DP<17>
(32)	UPL CPU2_CPU1_P0P2_DP16	EE9	UPL2_RX_DP<16> UPL2_TX_DP<16>
(32)	UPL CPU2_CPU1_P0P2_DP15	EB10	UPL2_RX_DP<15> UPL2_TX_DP<15>
(32)	UPL CPU2_CPU1_P0P2_DP14	DV10	UPL2_RX_DP<14> UPL2_TX_DP<14>
(32)	UPL CPU2_CPU1_P0P2_DP13	DW9	UPL2_RX_DP<13> UPL2_TX_DP<13>
(32)	UPL CPU2_CPU1_P0P2_DP12	DW11	UPL2_RX_DP<12> UPL2_TX_DP<12>
(32)	UPL CPU2_CPU1_P0P2_DP11	DT12	UPL2_RX_DP<11> UPL2_TX_DP<11>
(32)	UPL CPU2_CPU1_P0P2_DP10	DN9	UPL2_RX_DP<10> UPL2_TX_DP<10>
(32)	UPL CPU2_CPU1_P0P2_DP9	DN11	UPL2_RX_DP<9> UPL2_TX_DP<9>
(32)	UPL CPU2_CPU1_P0P2_DP8	DM10	UPL2_RX_DP<8> UPL2_TX_DP<8>
(32)	UPL CPU2_CPU1_P0P2_DP7	DH10	UPL2_RX_DP<7> UPL2_TX_DP<7>
(32)	UPL CPU2_CPU1_P0P2_DP6	DM12	UPL2_RX_DP<6> UPL2_TX_DP<6>
(32)	UPL CPU2_CPU1_P0P2_DP5	DG11	UPL2_RX_DP<5> UPL2_TX_DP<5>
(32)	UPL CPU2_CPU1_P0P2_DP4	DE11	UPL2_RX_DP<4> UPL2_TX_DP<4>
(32)	UPL CPU2_CPU1_P0P2_DP3	CB11	UPL2_RX_DP<3> UPL2_TX_DP<3>
(32)	UPL CPU2_CPU1_P0P2_DP2	CB11	UPL2_RX_DP<2> UPL2_TX_DP<2>
(32)	UPL CPU2_CPU1_P0P2_DP1	DB12	UPL2_RX_DP<1> UPL2_TX_DP<1>
(32)	UPL CPU2_CPU1_P0P2_D0	DC13	UPL2_RX_DP<0> UPL2_TX_DP<0>

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CPU1R-18			
(32)	UPL CPU2_CPU1_P1P1_DP19	R81	UPL1_RX_DP<19> UPL1_TX_DP<19>
(32)	UPL CPU2_CPU1_P1P1_DP18	W81	UPL1_RX_DP<18> UPL1_TX_DP<18>
(32)	UPL CPU2_CPU1_P1P1_DP17	Y82	UPL1_RX_DP<17> UPL1_TX_DP<17>
(32)	UPL CPU2_CPU1_P1P1_DP16	Y84	UPL1_RX_DP<16> UPL1_TX_DP<16>
(32)	UPL CPU2_CPU1_P1P1_DP15	W83	UPL1_RX_DP<15> UPL1_TX_DP<15>
(32)	UPL CPU2_CPU1_P1P1_DP14	AA85	UPL1_RX_DP<14> UPL1_TX_DP<14>
(32)	UPL CPU2_CPU1_P1P1_DP13	AA83	UPL1_RX_DP<13> UPL1_TX_DP<13>
(32)	UPL CPU2_CPU1_P1P1_DP12	Y86	UPL1_RX_DP<12> UPL1_TX_DP<12>
(32)	UPL CPU2_CPU1_P1P1_DP11	Y88	UPL1_RX_DP<11> UPL1_TX_DP<11>
(32)	UPL CPU2_CPU1_P1P1_DP10	U85	UPL1_RX_DP<10> UPL1_TX_DP<10>
(32)	UPL CPU2_CPU1_P1P1_DP9	P86	UPL1_RX_DP<9> UPL1_TX_DP<9>
(32)	UPL CPU2_CPU1_P1P1_DP8	R85	UPL1_RX_DP<8> UPL1_TX_DP<8>
(32)	UPL CPU2_CPU1_P1P1_DP7	N87	UPL1_RX_DP<7> UPL1_TX_DP<7>
(32)	UPL CPU2_CPU1_P1P1_DP6	N85	UPL1_RX_DP<6> UPL1_TX_DP<6>
(32)	UPL CPU2_CPU1_P1P1_DP5	U85	UPL1_RX_DP<5> UPL1_TX_DP<5>
(32)	UPL CPU2_CPU1_P1P1_DP4	H84	UPL1_RX_DP<4> UPL1_TX_DP<4>
(32)	UPL CPU2_CPU1_P1P1_DP3	M84	UPL1_RX_DP<3> UPL1_TX_DP<3>
(32)	UPL CPU2_CPU1_P1P1_DP2	H82	UPL1_RX_DP<2> UPL1_TX_DP<2>
(32)	UPL CPU2_CPU1_P1P1_DP1	G81	UPL1_RX_DP<1> UPL1_TX_DP<1>
(32)	UPL CPU2_CPU1_P1P1_D0		UPL1_RX_DP<0> UPL1_TX_DP<0>

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CPU1R-20			
(32)	UPL CPU2_CPU1_P3P3_D0	DB18	UPL3_RX_DP<19> UPL3_TX_DP<19>
(32)	UPL CPU2_CPU1_P3P3_D01	DV20	UPL3_RX_DP<18> UPL3_TX_DP<18>
(32)	UPL CPU2_CPU1_P3P3_D02	DU19	UPL3_RX_DP<17> UPL3_TX_DP<17>
(32)	UPL CPU2_CPU1_P3P3_D03	DP18	UPL3_RX_DP<16> UPL3_TX_DP<16>
(32)	UPL CPU2_CPU1_P3P3_D04	DL17	UPL3_RX_DP<15> UPL3_TX_DP<15>
(32)	UPL CPU2_CPU1_P3P3_D05	DJ17	UPL3_RX_DP<14> UPL3_TX_DP<14>
(32)	UPL CPU2_CPU1_P3P3_D06	DM16	UPL3_RX_DP<13> UPL3_TX_DP<13>
(32)	UPL CPU2_CPU1_P3P3_D07	DF16	UPL3_RX_DP<12> UPL3_TX_DP<12>
(32)	UPL CPU2_CPU1_P3P3_D08	DM14	UPL3_RX_DP<11> UPL3_TX_DP<11>
(32)	UPL CPU2_CPU1_P3P3_D09	DO18	UPL3_RX_DP<10> UPL3_TX_DP<10>
(32)	UPL CPU2_CPU1_P3P3_D10	DJ13	UPL3_RX_DP<9> UPL3_TX_DP<9>
(32)	UPL CPU2_CPU1_P3P3_D11	DO15	UPL3_RX_DP<8> UPL3_TX_DP<8>
(32)	UPL CPU2_CPU1_P3P3_D12	DC15	UPL3_RX_DP<7> UPL3_TX_DP<7>
(32)	UPL CPU2_CPU1_P3P3_D13	DA17	UPL3_RX_DP<6> UPL3_TX_DP<6>
(32)	UPL CPU2_CPU1_P3P3_D14	CH17	UPL3_RX_DP<5> UPL3_TX_DP<5>
(32)	UPL CPU2_CPU1_P3P3_D15	CR17	UPL3_RX_DP<4> UPL3_TX_DP<4>
(32)	UPL CPU2_CPU1_P3P3_D16	CP18	UPL3_RX_DP<3> UPL3_TX_DP<3>
(32)	UPL CPU2_CPU1_P3P3_D17	CP16	UPL3_RX_DP<2> UPL3_TX_DP<2>
(32)	UPL CPU2_CPU1_P3P3_D18		UPL3_RX_DP<1> UPL3_TX_DP<1>
(32)	UPL CPU2_CPU1_P3P3_D19		UPL3_RX_DP<0> UPL3_TX_DP<0>

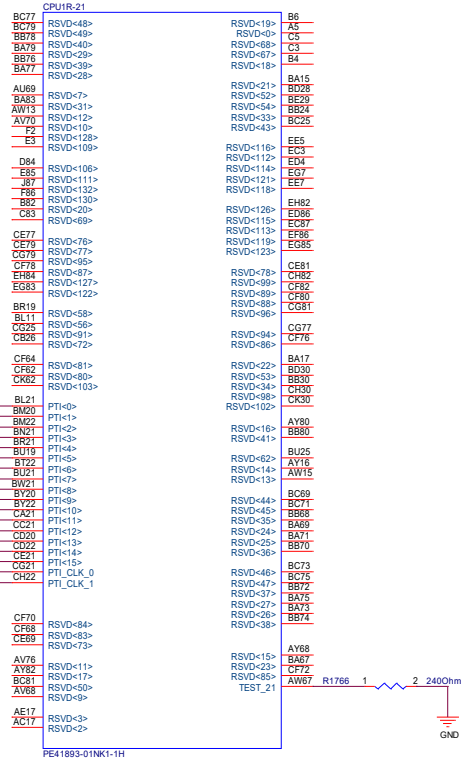
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CPU1R-18			
(32)	UPL CPU1_CPU2_P1P1_DP19	AI81	UPL1_CPU1_CPU2_P1P1_DP19
(32)	UPL CPU1_CPU2_P1P1_DP18	AI82	UPL1_CPU1_CPU2_P1P1_DP18
(32)	UPL CPU1_CPU2_P1P1_DP17	AI83	UPL1_CPU1_CPU2_P1P1_DP17
(32)	UPL CPU1_CPU2_P1P1_DP16	AI84	UPL1_CPU1_CPU2_P1P1_DP16
(32)	UPL CPU1_CPU2_P1P1_DP15	AI85	UPL1_CPU1_CPU2_P1P1_DP15
(32)	UPL CPU1_CPU2_P1P1_DP14	AI86	UPL1_CPU1_CPU2_P1P1_DP14
(32)	UPL CPU1_CPU2_P1P1_DP13	AI87	UPL1_CPU1_CPU2_P1P1_DP13
(32)	UPL CPU1_CPU2_P1P1_DP12	AI88	UPL1_CPU1_CPU2_P1P1_DP12
(32)	UPL CPU1_CPU2_P1P1_DP11	AI89	UPL1_CPU1_CPU2_P1P1_DP11
(32)	UPL CPU1_CPU2_P1P1_DP10	AI90	UPL1_CPU1_CPU2_P1P1_DP10
(32)	UPL CPU1_CPU2_P1P1_DP9	AI91	UPL1_CPU1_CPU2_P1P1_DP9
(32)	UPL CPU1_CPU2_P1P1_DP8	AI92	UPL1_CPU1_CPU2_P1P1_DP8
(32)	UPL CPU1_CPU2_P1P1_DP7	AI93	UPL1_CPU1_CPU2_P1P1_DP7
(32)	UPL CPU1_CPU2_P1P1_DP6	AI94	UPL1_CPU1_CPU2_P1P1_DP6
(32)	UPL CPU1_CPU2_P1P1_DP5	AI95	UPL1_CPU1_CPU2_P1P1_DP5
(32)	UPL CPU1_CPU2_P1P1_DP4	AI96	UPL1_CPU1_CPU2_P1P1_DP4
(32)	UPL CPU1_CPU2_P1P1_DP3	AI97	UPL1_CPU1_CPU2_P1P1_DP3
(32)	UPL CPU1_CPU2_P1P1_DP2	AI98	UPL1_CPU1_CPU2_P1P1_DP2
(32)	UPL CPU1_CPU2_P1P1_DP1	AI99	UPL1_CPU1_CPU2_P1P1_DP1
(32)	UPL CPU1_CPU2_P1P1_D0	AI00	UPL1_CPU1_CPU2_P1P1_D0

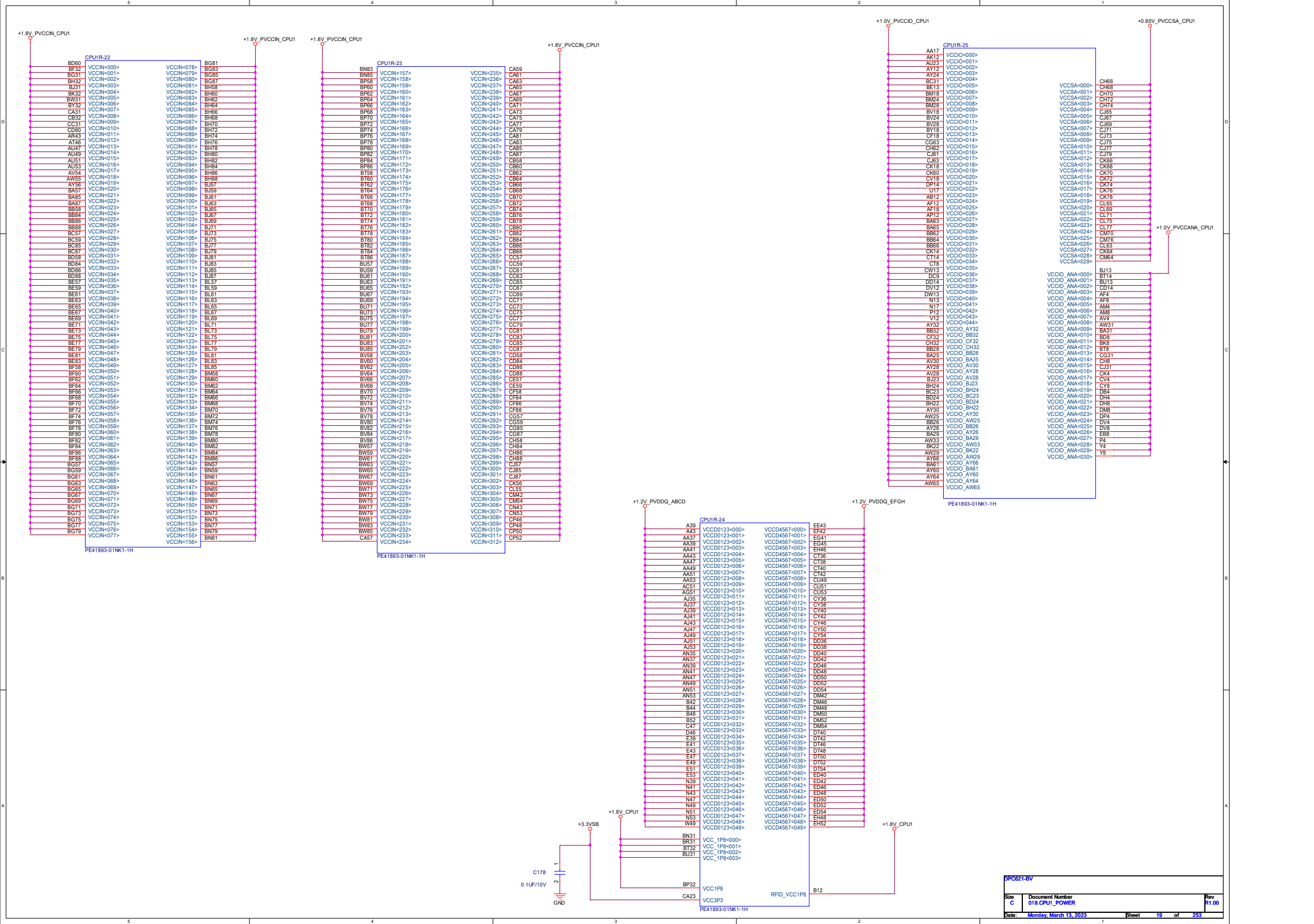
CPU1R-20			
(32)	UPL CPU2_CPU1_P3P3_D0	CJ17	UPL3_CPU1_CPU2_P3P3_D0
(32)	UPL CPU2_CPU1_P3P3_D01	CH18	UPL3_CPU1_CPU2_P3P3_D01
(32)	UPL CPU2_CPU1_P3P3_D02	CH19	UPL3_CPU1_CPU2_P3P3_D02
(32)	UPL CPU2_CPU1_P3P3_D03	CG15	UPL3_CPU1_CPU2_P3P3_D03
(32)	UPL CPU2_CPU1_P3P3_D04	CG17	UPL3_CPU1_CPU2_P3P3_D04
(32)	UPL CPU2_CPU1_P3P3_D05	CE15	UPL3_CPU1_CPU2_P3P3_D05
(32)	UPL CPU2_CPU1_P3P3_D06	CB18	UPL3_CPU1_CPU2_P3P3_D06
(32)	UPL CPU2_CPU1_P3P3_D07	BY14	UPL3_CPU1_CPU2_P3P3_D07
(32)	UPL CPU2_CPU1_P3P3_D08	BU17	UPL3_CPU1_CPU2_P3P3_D08
(32)	UPL CPU2_CPU1_P3P3_D09	BR15	UPL3_CPU1_CPU2_P3P3_D09
(32)	UPL CPU2_CPU1_P3P3_D10	BN15	UPL3_CPU1_CPU2_P3P3_D10
(32)	UPL CPU2_CPU1_P3P3_D11	BL17	UPL3_CPU1_CPU2_P3P3_D11
(32)	UPL CPU2_CPU1_P3P3_D12	BL15	UPL3_CPU1_CPU2_P3P3_D12
(32)	UPL CPU2_CPU1_P3P3_D13	BT14	UPL3_CPU1_CPU2_P3P3_D13
(32)	UPL CPU2_CPU1_P3P3_D14	BA18	UPL3_CPU1_CPU2_P3P3_D14
(32)	UPL CPU2_CPU1_P3P3_D15	BA15	UPL3_CPU1_CPU2_P3P3_D15
(32)	UPL CPU2_CPU1_P3P3_D16	BA13	UPL3_CPU1_CPU2_P3P3_D16
(32)	UPL CPU2_CPU1_P3P3_D17	BD14	UPL3_CPU1_CPU2_P3P3_D17
(32)	UPL CPU2_CPU1_P3P3_D18	BE16	UPL3_CPU1_CPU2_P3P3_D18
(32)	UPL CPU2_CPU1_P3P3_D19		UPL3_CPU1_CPU2_P3P3_D19

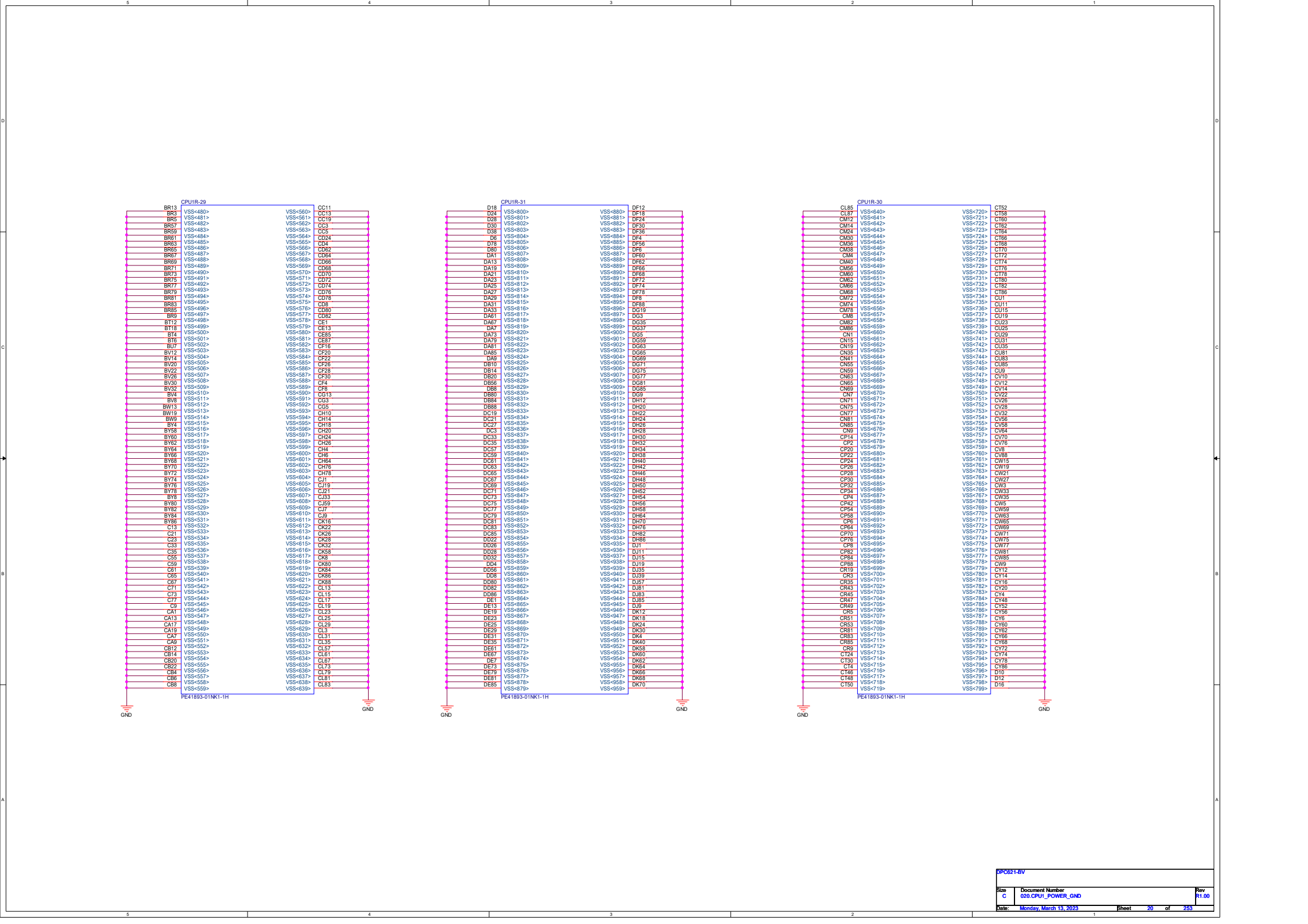
JPC021-3V

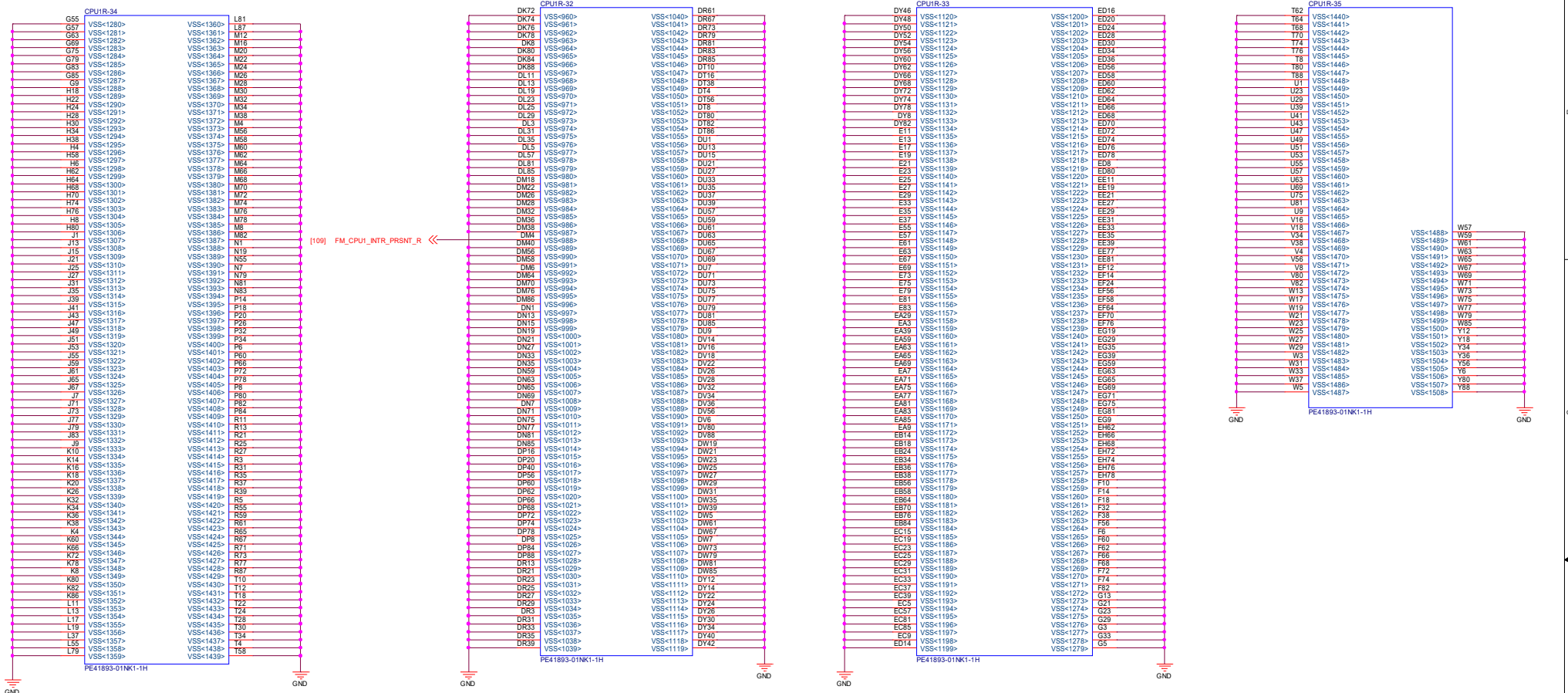
R1.01 Tony 200205  
修改MIPI 線路. 新增PTI\_DATA[8:15] to CPU

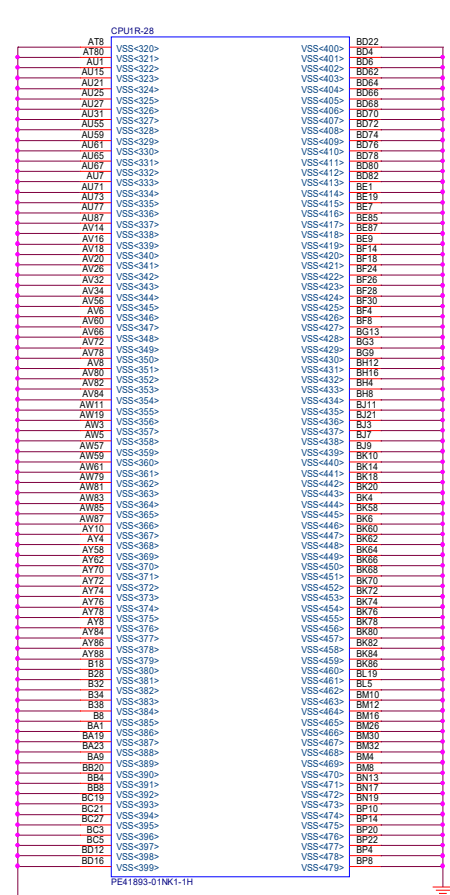
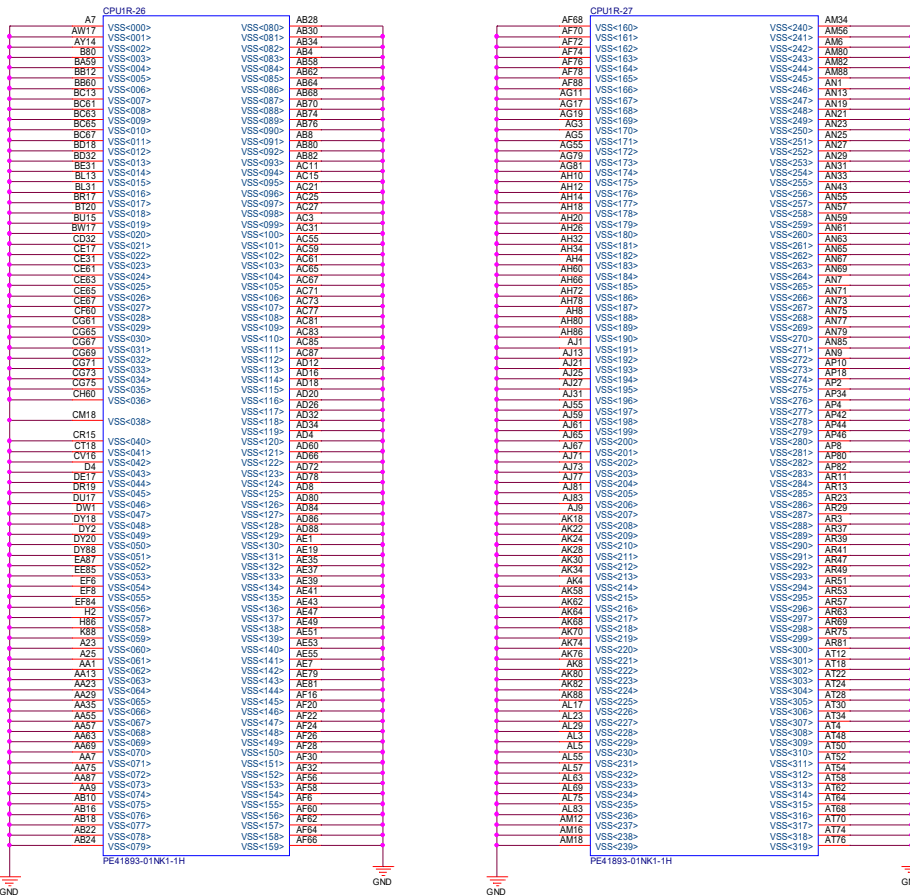




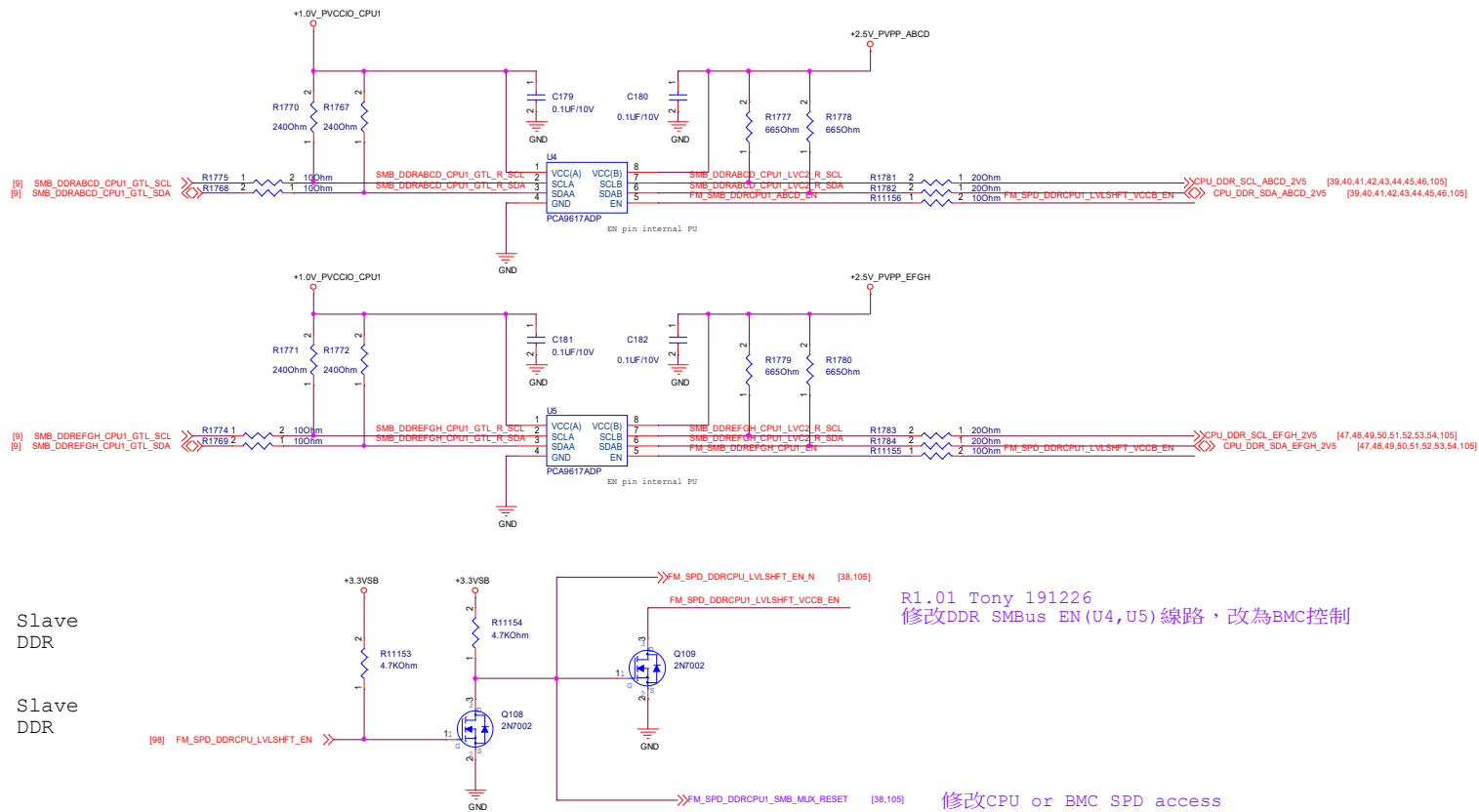








1 NP NC 1  
2 NP NC 2  
3 NP NC 3  
4 NP NC 4  
5 NP NC 5  
6 NP NC 6

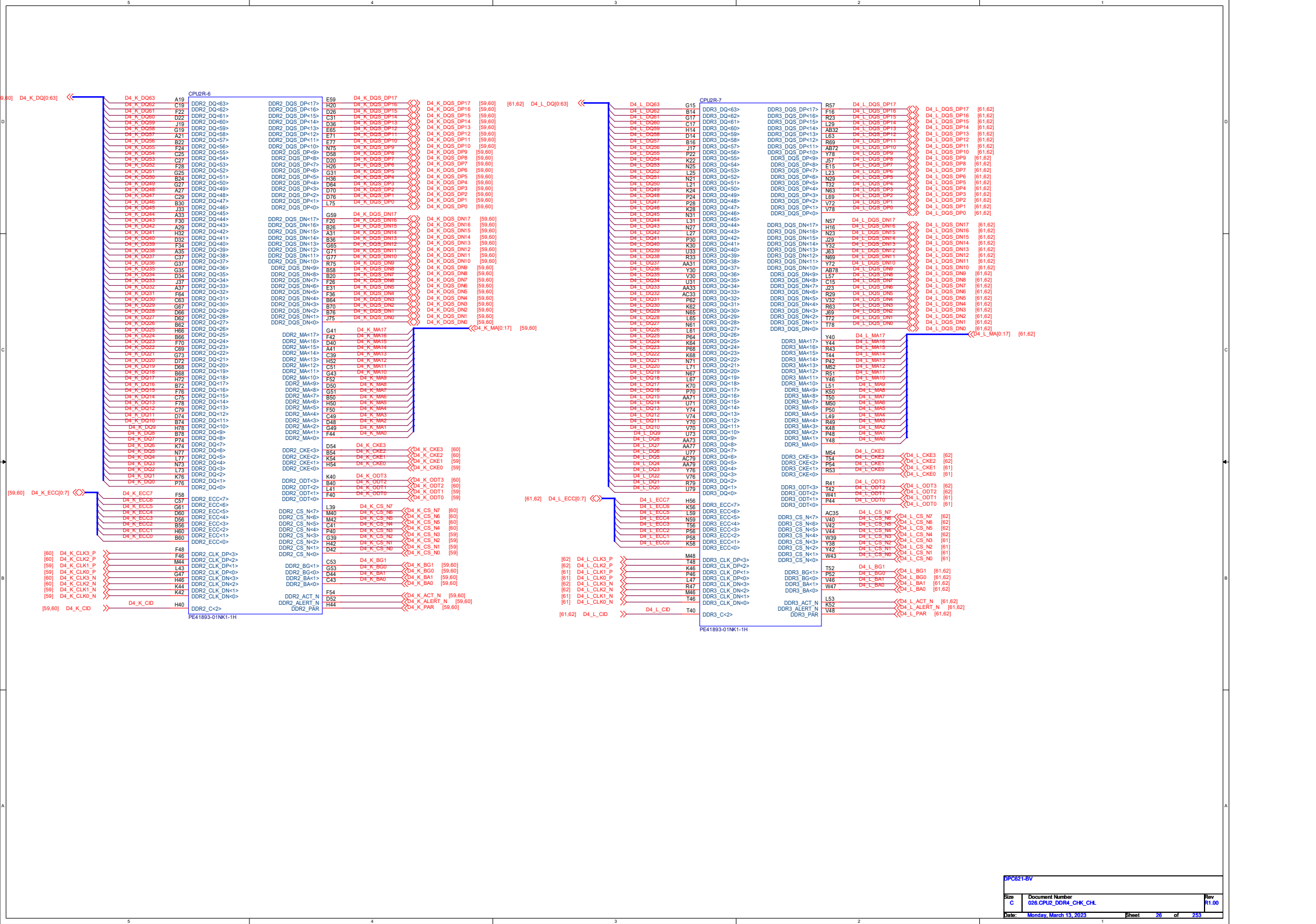




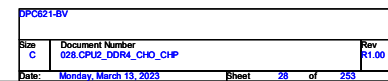


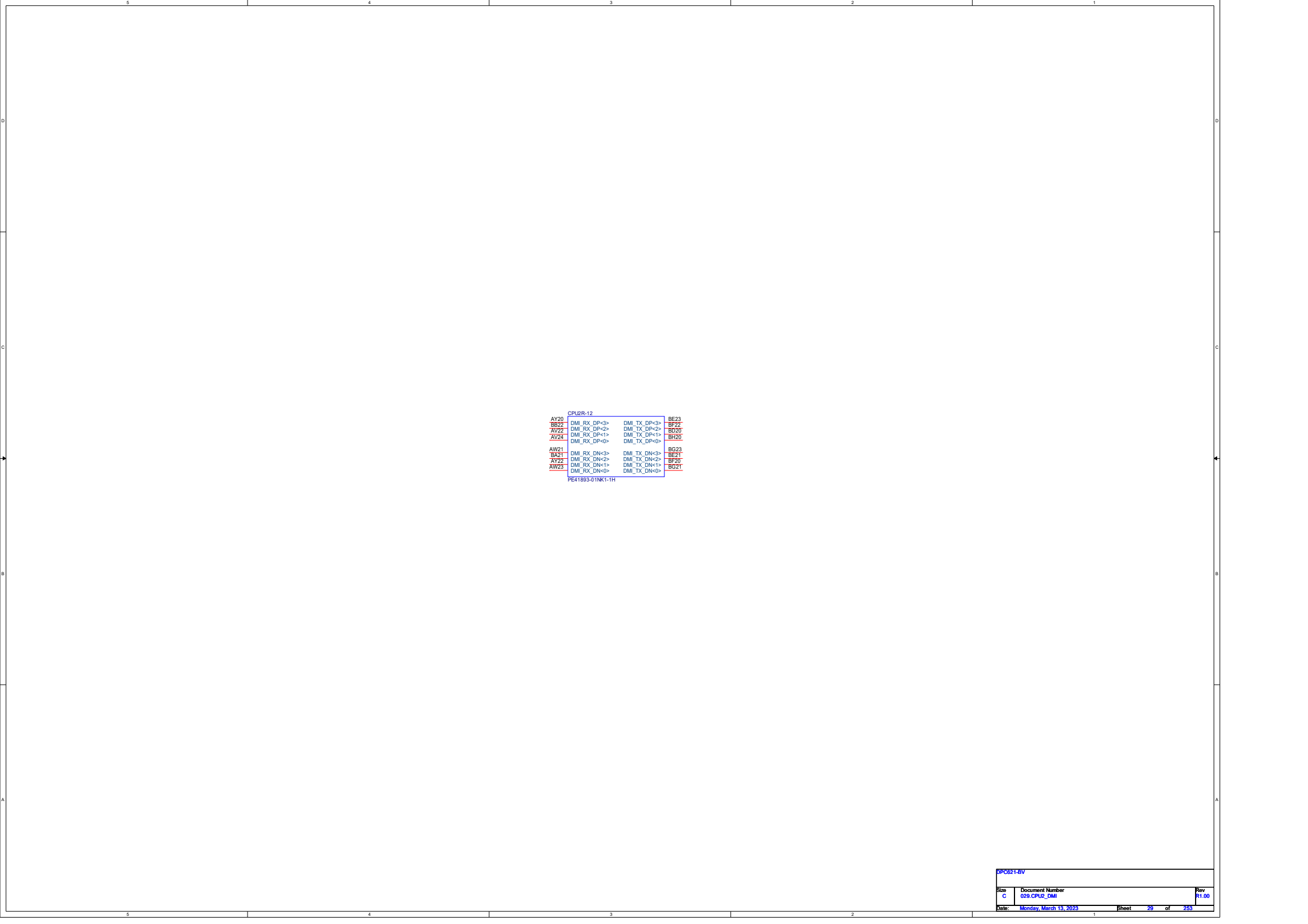












CPL2R-12			
AY20	DMI_RX_DP<3>	DMI_TX_DP<3>	BE23
BE22	DMI_RX_DP<2>	DMI_TX_DP<2>	BE22
AV22	DMI_RX_DP<1>	DMI_TX_DP<1>	BD20
AV24	DMI_RX_DP<0>	DMI_TX_DP<0>	BH20
PE41893-01NK1-1H			
AW21	DMI_RX_DN<3>	DMI_TX_DN<3>	BG23
BA21	DMI_RX_DN<2>	DMI_TX_DN<2>	BE21
AY22	DMI_RX_DN<1>	DMI_TX_DN<1>	BE20
AW23	DMI_RX_DN<0>	DMI_TX_DN<0>	BE21

CPU2R-13			
(118) P4E_CPU2_PEGA_RX_DP15	AM0	PE0_RX_DP<15>	AR7 P4E_CPU2_PEGA_TX_DP15
(118) P4E_CPU2_PEGA_RX_DP14	AH2	PE0_RX_DP<14>	AL7 P4E_CPU2_PEGA_TX_DP14
(118) P4E_CPU2_PEGA_RX_DP13	AH2	PE0_RX_DP<13>	AJ5 P4E_CPU2_PEGA_TX_DP13
(118) P4E_CPU2_PEGA_RX_DP12	AD2	PE0_RX_DP<12>	AE5 P4E_CPU2_PEGA_TX_DP12
(118) P4E_CPU2_PEGA_RX_DP11	AB2	PE0_RX_DP<11>	AA5 P4E_CPU2_PEGA_TX_DP11
(118) P4E_CPU2_PEGA_RX_DP10	Y2	PE0_RX_DP<10>	AY7 P4E_CPU2_PEGA_TX_DP10
(118) P4E_CPU2_PEGA_RX_DP9	V2	PE0_RX_DP<9>	W7 P4E_CPU2_PEGA_TX_DP9
(118) P4E_CPU2_PEGA_RX_DP8	T2	PE0_RX_DP<8>	U5 P4E_CPU2_PEGA_TX_DP8
(118) P4E_CPU2_PEGA_RX_DP7	T2	PE0_RX_DP<7>	RT P4E_CPU2_PEGA_TX_DP7
(118) P4E_CPU2_PEGA_RX_DP6	M2	PE0_RX_DP<6>	NS P4E_CPU2_PEGA_TX_DP6
(118) P4E_CPU2_PEGA_RX_DP5	K2	PE0_RX_DP<5>	MS P4E_CPU2_PEGA_TX_DP5
(118) P4E_CPU2_PEGA_RX_DP4	J3	PE0_RX_DP<4>	M6 P4E_CPU2_PEGA_TX_DP4
(118) P4E_CPU2_PEGA_RX_DP3	D8	PE0_RX_DP<3>	J11 P4E_CPU2_PEGA_TX_DP3
(118) P4E_CPU2_PEGA_RX_DP2	B9	PE0_RX_DP<2>	G11 P4E_CPU2_PEGA_TX_DP2
(118) P4E_CPU2_PEGA_RX_DP1	E7	PE0_RX_DP<1>	H12 P4E_CPU2_PEGA_TX_DP1
(118) P4E_CPU2_PEGA_RX_DP0	E7	PE0_RX_DP<0>	PE0_TX_DP<0>
PE41893-01NK1-1H			
(118) P4E_CPU2_PEGA_RX_DN15	AN3	PE0_RX_DN<15>	AP6 P4E_CPU2_PEGA_TX_DN15
(118) P4E_CPU2_PEGA_RX_DN14	AL7	PE0_RX_DN<14>	AK6 P4E_CPU2_PEGA_TX_DN14
(118) P4E_CPU2_PEGA_RX_DN13	AJ3	PE0_RX_DN<13>	AH6 P4E_CPU2_PEGA_TX_DN13
(118) P4E_CPU2_PEGA_RX_DN12	AG1	PE0_RX_DN<12>	AJ7 P4E_CPU2_PEGA_TX_DN12
(118) P4E_CPU2_PEGA_RX_DN11	AE6	PE0_RX_DN<11>	AD6 P4E_CPU2_PEGA_TX_DN11
(118) P4E_CPU2_PEGA_RX_DN10	AC1	PE0_RX_DN<10>	AC5 P4E_CPU2_PEGA_TX_DN10
(118) P4E_CPU2_PEGA_RX_DN9	AX3	PE0_RX_DN<9>	AB6 P4E_CPU2_PEGA_TX_DN9
(118) P4E_CPU2_PEGA_RX_DN8	W7	PE0_RX_DN<8>	V8 P4E_CPU2_PEGA_TX_DN8
(118) P4E_CPU2_PEGA_RX_DN7	U3	PE0_RX_DN<7>	T6 P4E_CPU2_PEGA_TX_DN7
(118) P4E_CPU2_PEGA_RX_DN6	R1	PE0_RX_DN<6>	LT P4E_CPU2_PEGA_TX_DN6
(118) P4E_CPU2_PEGA_RX_DN5	N3	PE0_RX_DN<5>	L5 P4E_CPU2_PEGA_TX_DN5
(118) P4E_CPU2_PEGA_RX_DN4	L1	PE0_RX_DN<4>	J5 P4E_CPU2_PEGA_TX_DN4
(118) P4E_CPU2_PEGA_RX_DN3	L3	PE0_RX_DN<3>	H10 P4E_CPU2_PEGA_TX_DN3
(118) P4E_CPU2_PEGA_RX_DN2	C7	PE0_RX_DN<2>	F12 P4E_CPU2_PEGA_TX_DN2
(118) P4E_CPU2_PEGA_RX_DN1	GB	PE0_RX_DN<1>	K12 P4E_CPU2_PEGA_TX_DN1
(118) P4E_CPU2_PEGA_RX_DN0	GT	PE0_RX_DN<0>	PE0_TX_DN<0>

CPU2R-14			
(117) P4E_CPU2_PE1D_RISER2_RX_DP15	AT2	PE1_TX_DP<15>	AN5 P4E_CPU2_PE1D_RISER2_TX_DP15
(117) P4E_CPU2_PE1D_RISER2_RX_DP14	AV2	PE1_TX_DP<14>	AU5 P4E_CPU2_PE1D_RISER2_TX_DP14
(117) P4E_CPU2_PE1D_RISER2_RX_DP13	BB2	PE1_TX_DP<13>	AW7 P4E_CPU2_PE1D_RISER2_TX_DP13
(117) P4E_CPU2_PE1D_RISER2_RX_DP12	B02	PE1_TX_DP<12>	BC7 P4E_CPU2_PE1C_RISER2_TX_DP12
(117) P4E_CPU2_PE1C_RISER2_RX_DP11	BF2	PE1_TX_DP<11>	BG7 P4E_CPU2_PE1C_RISER2_TX_DP11
(117) P4E_CPU2_PE1C_RISER2_RX_DP10	B02	PE1_TX_DP<10>	BE5 P4E_CPU2_PE1C_RISER2_TX_DP10
(117) P4E_CPU2_PE1C_RISER2_RX_DP9	BN3	PE1_TX_DP<9>	BJ5 P4E_CPU2_PE1C_RISER2_TX_DP9
(117) P4E_CPU2_PE1C_RISER2_RX_DP8	CA3	PE1_TX_DP<8>	BL7 P4E_CPU2_PE1B_RISER2_TX_DP8
(117) P4E_CPU2_PE1B_RISER2_RX_DP7	BW3	PE1_TX_DP<7>	BM5 P4E_CPU2_PE1B_RISER2_TX_DP7
(117) P4E_CPU2_PE1B_RISER2_RX_DP6	CC1	PE1_TX_DP<6>	BR7 P4E_CPU2_PE1B_RISER2_TX_DP6
(117) P4E_CPU2_PE1C_RISER2_RX_DP5	CA3	PE1_TX_DP<5>	BS5 P4E_CPU2_PE1C_RISER2_TX_DP5
(117) P4E_CPU2_PE1B_RISER2_RX_DP4	CC3	PE1_TX_DP<4>	BV6 P4E_CPU2_PE1A_RISER2_TX_DP4
(117) P4E_CPU2_PE1A_RISER2_RX_DP3	CJ3	PE1_TX_DP<3>	BWS P4E_CPU2_PE1A_RISER2_TX_DP3
(117) P4E_CPU2_PE1A_RISER2_RX_DP2	CL1	PE1_TX_DP<2>	CC7 P4E_CPU2_PE1A_RISER2_TX_DP2
(117) P4E_CPU2_PE1A_RISER2_RX_DP1	CK3	PE1_TX_DP<1>	CE5 P4E_CPU2_PE1A_RISER2_TX_DP1
(117) P4E_CPU2_PE1A_RISER2_RX_DP0	CK3	PE1_TX_DP<0>	PE1_TX_DP<0>
PE41893-01NK1-1H			
(117) P4E_CPU2_PE1D_RISER2_RX_DN15	AR1	PE1_TX_DN<15>	AR5 P4E_CPU2_PE1D_RISER2_TX_DN15
(117) P4E_CPU2_PE1D_RISER2_RX_DN14	AL3	PE1_TX_DN<14>	AT6 P4E_CPU2_PE1D_RISER2_TX_DN14
(117) P4E_CPU2_PE1D_RISER2_RX_DN13	AW1	PE1_TX_DN<13>	BA7 P4E_CPU2_PE1D_RISER2_TX_DN13
(117) P4E_CPU2_PE1D_RISER2_RX_DN12	BA3	PE1_TX_DN<12>	YB6 P4E_CPU2_PE1D_RISER2_TX_DN12
(117) P4E_CPU2_PE1C_RISER2_RX_DN11	BC1	PE1_TX_DN<11>	BB8 P4E_CPU2_PE1C_RISER2_TX_DN11
(117) P4E_CPU2_PE1C_RISER2_RX_DN10	BE3	PE1_TX_DN<10>	BF6 P4E_CPU2_PE1C_RISER2_TX_DN10
(117) P4E_CPU2_PE1C_RISER2_RX_DN9	BS1	PE1_TX_DN<9>	BG5 P4E_CPU2_PE1C_RISER2_TX_DN9
(117) P4E_CPU2_PE1C_RISER2_RX_DN8	BL3	PE1_TX_DN<8>	BH6 P4E_CPU2_PE1C_RISER2_TX_DN8
(117) P4E_CPU2_PE1C_RISER2_RX_DN7	BU3	PE1_TX_DN<7>	BN7 P4E_CPU2_PE1B_RISER2_TX_DN7
(117) P4E_CPU2_PE1B_RISER2_RX_DN6	BY2	PE1_TX_DN<6>	BM5 P4E_CPU2_PE1B_RISER2_TX_DN6
(117) P4E_CPU2_PE1B_RISER2_RX_DN5	CB2	PE1_TX_DN<5>	BP6 P4E_CPU2_PE1B_RISER2_TX_DN5
(117) P4E_CPU2_PE1B_RISER2_RX_DN4	CD2	PE1_TX_DN<4>	BW7 P4E_CPU2_PE1B_RISER2_TX_DN4
(117) P4E_CPU2_PE1A_RISER2_RX_DN3	CH2	PE1_TX_DN<3>	BUS P4E_CPU2_PE1A_RISER2_TX_DN3
(117) P4E_CPU2_PE1A_RISER2_RX_DN2	CL2	PE1_TX_DN<2>	CA5 P4E_CPU2_PE1A_RISER2_TX_DN2
(117) P4E_CPU2_PE1A_RISER2_RX_DN1	CK2	PE1_TX_DN<1>	CE7 P4E_CPU2_PE1A_RISER2_TX_DN1
(117) P4E_CPU2_PE1A_RISER2_RX_DN0	CK2	PE1_TX_DN<0>	PE1_TX_DN<0>

## PE1 A-D x16 connect to PCIe Slot x32 (RISER2)

P4E_CPU2_PEGA_TX_DP15	C183	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP15	(118)
P4E_CPU2_PEGA_TX_DP14	C185	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP14	(118)
P4E_CPU2_PEGA_TX_DP13	C187	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP13	(118)
P4E_CPU2_PEGA_TX_DP12	C189	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP12	(118)
P4E_CPU2_PEGA_TX_DP11	C191	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP11	(118)
P4E_CPU2_PEGA_TX_DP10	C193	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP10	(118)
P4E_CPU2_PEGA_TX_DP9	C195	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP9	(118)
P4E_CPU2_PEGA_TX_DP8	C197	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP8	(118)
P4E_CPU2_PEGA_TX_DP7	C199	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP7	(118)
P4E_CPU2_PEGA_TX_DP6	C201	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP6	(118)
P4E_CPU2_PEGA_TX_DP5	C203	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP5	(118)
P4E_CPU2_PEGA_TX_DP4	C205	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP4	(118)
P4E_CPU2_PEGA_TX_DP3	C207	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP3	(118)
P4E_CPU2_PEGA_TX_DP2	C209	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP2	(118)
P4E_CPU2_PEGA_TX_DP1	C211	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP1	(118)
P4E_CPU2_PEGA_TX_DP0	C213	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DP0	(118)
P4E_CPU2_PEGA_TX_DN15	C215	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN15	(118)
P4E_CPU2_PEGA_TX_DN14	C217	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN14	(118)
P4E_CPU2_PEGA_TX_DN13	C219	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN13	(118)
P4E_CPU2_PEGA_TX_DN12	C221	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN12	(118)
P4E_CPU2_PEGA_TX_DN11	C223	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN11	(118)
P4E_CPU2_PEGA_TX_DN10	C225	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN10	(118)
P4E_CPU2_PEGA_TX_DN9	C227	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN9	(118)
P4E_CPU2_PEGA_TX_DN8	C229	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN8	(118)
P4E_CPU2_PEGA_TX_DN7	C231	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN7	(118)
P4E_CPU2_PEGA_TX_DN6	C233	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN6	(118)
P4E_CPU2_PEGA_TX_DN5	C235	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN5	(118)
P4E_CPU2_PEGA_TX_DN4	C237	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN4	(118)
P4E_CPU2_PEGA_TX_DN3	C239	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN3	(118)
P4E_CPU2_PEGA_TX_DN2	C241	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN2	(118)
P4E_CPU2_PEGA_TX_DN1	C243	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN1	(118)
P4E_CPU2_PEGA_TX_DN0	C245	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN0	(118)
P4E_CPU2_PEGA_TX_DN0	C247	2	1	0.22UF/6.3V	>>>P4E_CPU2_PEGA_C_TX_DN0	(118)

P4E_CPU2_PE1B_RISER2_TX_DP7	C184	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DP7	(117)
P4E_CPU2_PE1B_RISER2_TX_DP6	C186	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DP6	(117)
P4E_CPU2_PE1B_RISER2_TX_DP5	C188	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DP5	(117)
P4E_CPU2_PE1B_RISER2_TX_DP4	C190	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DP4	(117)
P4E_CPU2_PE1A_RISER2_TX_DP3	C192	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DP3	(117)
P4E_CPU2_PE1A_RISER2_TX_DP2	C194	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DP2	(117)
P4E_CPU2_PE1A_RISER2_TX_DP1	C196	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DP1	(117)
P4E_CPU2_PE1A_RISER2_TX_DP0	C198	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DP0	(117)
P4E_CPU2_PE1B_RISER2_TX_DN7	C201	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DN7	(117)
P4E_CPU2_PE1B_RISER2_TX_DN6	C203	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DN6	(117)
P4E_CPU2_PE1B_RISER2_TX_DN5	C205	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DN5	(117)
P4E_CPU2_PE1B_RISER2_TX_DN4	C207	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1B_RISER2_C_TX_DN4	(117)
P4E_CPU2_PE1A_RISER2_TX_DN3	C209	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DN3	(117)
P4E_CPU2_PE1A_RISER2_TX_DN2	C211	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DN2	(117)
P4E_CPU2_PE1A_RISER2_TX_DN1	C213	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DN1	(117)
P4E_CPU2_PE1A_RISER2_TX_DN0	C215	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1A_RISER2_C_TX_DN0	(117)
P4E_CPU2_PE1D_RISER2_TX_DP15	C228	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DP15	(117)
P4E_CPU2_PE1D_RISER2_TX_DP14	C230	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DP14	(117)
P4E_CPU2_PE1D_RISER2_TX_DP13	C232	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DP13	(117)
P4E_CPU2_PE1D_RISER2_TX_DP12	C234	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DP12	(117)
P4E_CPU2_PE1C_RISER2_TX_DP11	C236	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DP11	(117)
P4E_CPU2_PE1C_RISER2_TX_DP10	C238	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DP10	(117)
P4E_CPU2_PE1C_RISER2_TX_DP9	C240	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DP9	(117)
P4E_CPU2_PE1C_RISER2_TX_DP8	C242	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DP8	(117)
P4E_CPU2_PE1D_RISER2_TX_DN15	C239	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DN15	(117)
P4E_CPU2_PE1D_RISER2_TX_DN14	C241	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DN14	(117)
P4E_CPU2_PE1D_RISER2_TX_DN13	C243	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1D_RISER2_C_TX_DN13	(117)
P4E_CPU2_PE1C_RISER2_TX_DN12	C245	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DN12	(117)
P4E_CPU2_PE1C_RISER2_TX_DN11	C247	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DN11	(117)
P4E_CPU2_PE1C_RISER2_TX_DN10	C249	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DN10	(117)
P4E_CPU2_PE1C_RISER2_TX_DN9	C251	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DN9	(117)
P4E_CPU2_PE1C_RISER2_TX_DN8	C253	2	1	0.22UF/6.3V	>>>P4E_CPU2_PE1C_RISER2_C_TX_DN8	(117)

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CPU2R-15			
(117) P4E_CPU2_PE2A_RISER2_RX_DP15	E07	PE2_RX_DP15<15>	PE2_TX_DP15<15>
(117) P4E_CPU2_PE2A_RISER2_RX_DP14	DV6	PE2_RX_DP14<14>	PE2_TX_DP14<14>
(117) P4E_CPU2_PE2A_RISER2_RX_DP13	EAS	PE2_RX_DP13<13>	PE2_TX_DP13<13>
(117) P4E_CPU2_PE2A_RISER2_RX_DP12	DV4	PE2_RX_DP12<12>	PE2_TX_DP12<12>
(117) P4E_CPU2_PE2A_RISER2_RX_DP11	DV2	PE2_RX_DP11<11>	PE2_TX_DP11<11>
(117) P4E_CPU2_PE2A_RISER2_RX_DP10	DV7	PE2_RX_DP10<10>	PE2_TX_DP10<10>
(117) P4E_CPU2_PE2A_RISER2_RX_DP9	DP2	PE2_RX_DP9<9>	PE2_TX_DP9<9>
(117) P4E_CPU2_PE2A_RISER2_RX_DP8	DM2	PE2_RX_DP8<8>	PE2_TX_DP8<8>
(117) P4E_CPU2_PE2A_RISER2_RX_DP7	DM7	PE2_RX_DP7<7>	PE2_TX_DP7<7>
(117) P4E_CPU2_PE2A_RISER2_RX_DP6	DM2	PE2_RX_DP6<6>	PE2_TX_DP6<6>
(117) P4E_CPU2_PE2A_RISER2_RX_DP5	DM7	PE2_RX_DP5<5>	PE2_TX_DP5<5>
(117) P4E_CPU2_PE2A_RISER2_RX_DP4	DM2	PE2_RX_DP4<4>	PE2_TX_DP4<4>
(117) P4E_CPU2_PE2A_RISER2_RX_DP3	DM7	PE2_RX_DP3<3>	PE2_TX_DP3<3>
(117) P4E_CPU2_PE2A_RISER2_RX_DP2	DM2	PE2_RX_DP2<2>	PE2_TX_DP2<2>
(117) P4E_CPU2_PE2A_RISER2_RX_DP1	DM7	PE2_RX_DP1<1>	PE2_TX_DP1<1>
(117) P4E_CPU2_PE2A_RISER2_RX_DP0	DM2	PE2_RX_DP0<0>	PE2_TX_DP0<0>
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CPU2R-16			
(129) P4E_CPU2_PE3D_SLIMS_RX_DP15	E886	PE3_RX_DP15<15>	PE3_TX_DP15<15>
(129) P4E_CPU2_PE3D_SLIMS_RX_DP14	DW87	PE3_RX_DP14<14>	PE3_TX_DP14<14>
(129) P4E_CPU2_PE3D_SLIMS_RX_DP13	DW87	PE3_RX_DP13<13>	PE3_TX_DP13<13>
(129) P4E_CPU2_PE3D_SLIMS_RX_DP12	DW87	PE3_RX_DP12<12>	PE3_TX_DP12<12>
(129) P4E_CPU2_PE3C_SLIMS_RX_DP11	DW87	PE3_RX_DP11<11>	PE3_TX_DP11<11>
(129) P4E_CPU2_PE3C_SLIMS_RX_DP10	DW87	PE3_RX_DP10<10>	PE3_TX_DP10<10>
(129) P4E_CPU2_PE3C_SLIMS_RX_DP9	DW87	PE3_RX_DP9<9>	PE3_TX_DP9<9>
(129) P4E_CPU2_PE3C_SLIMS_RX_DP8	DW87	PE3_RX_DP8<8>	PE3_TX_DP8<8>
(129) P4E_CPU2_PE3C_SLIMS_RX_DP7	DW87	PE3_RX_DP7<7>	PE3_TX_DP7<7>
(129) P4E_CPU2_PE3C_SLIMS_RX_DP6	DW87	PE3_RX_DP6<6>	PE3_TX_DP6<6>
(129) P4E_CPU2_PE3B_SLIMS_RX_DP5	DW87	PE3_RX_DP5<5>	PE3_TX_DP5<5>
(129) P4E_CPU2_PE3B_SLIMS_RX_DP4	DW87	PE3_RX_DP4<4>	PE3_TX_DP4<4>
(129) P4E_CPU2_PE3A_SLIMS_RX_DP3	DW87	PE3_RX_DP3<3>	PE3_TX_DP3<3>
(129) P4E_CPU2_PE3A_SLIMS_RX_DP2	DW87	PE3_RX_DP2<2>	PE3_TX_DP2<2>
(129) P4E_CPU2_PE3A_SLIMS_RX_DP1	DW87	PE3_RX_DP1<1>	PE3_TX_DP1<1>
(129) P4E_CPU2_PE3A_SLIMS_RX_DP0	DW87	PE3_RX_DP0<0>	PE3_TX_DP0<0>
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PE2 A x16 connect to PCIe Slot x32 (RISER2)

PE3 A x4 connect to Slimline8  
PE3 B x4 connect to Slimline7  
PE3 C x4 connect to Slimline6  
PE3 D x4 connect to Slimline5

P4E_CPU2_PE2A_RISER2_TX_DP15	C247	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP15	(117)
P4E_CPU2_PE2A_RISER2_TX_DP14	C248	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP14	(117)
P4E_CPU2_PE2A_RISER2_TX_DP13	C250	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP13	(117)
P4E_CPU2_PE2A_RISER2_TX_DP12	C252	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP12	(117)
P4E_CPU2_PE2A_RISER2_TX_DP11	C254	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP11	(117)
P4E_CPU2_PE2A_RISER2_TX_DP10	C256	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP10	(117)
P4E_CPU2_PE2A_RISER2_TX_DP9	C258	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP9	(117)
P4E_CPU2_PE2A_RISER2_TX_DP8	C260	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP8	(117)
P4E_CPU2_PE2A_RISER2_TX_DP7	C262	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP7	(117)
P4E_CPU2_PE2A_RISER2_TX_DP6	C264	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP6	(117)
P4E_CPU2_PE2A_RISER2_TX_DP5	C266	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP5	(117)
P4E_CPU2_PE2A_RISER2_TX_DP4	C268	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP4	(117)
P4E_CPU2_PE2A_RISER2_TX_DP3	C270	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP3	(117)
P4E_CPU2_PE2A_RISER2_TX_DP2	C272	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP2	(117)
P4E_CPU2_PE2A_RISER2_TX_DP1	C274	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP1	(117)
P4E_CPU2_PE2A_RISER2_TX_DP0	C276	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DP0	(117)
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P4E_CPU2_PE3D_SLIMS_TX_DP15	C249	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3D_SLIMS_C_TX_DP15	(129)
P4E_CPU2_PE3D_SLIMS_TX_DP14	C251	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3D_SLIMS_C_TX_DP14	(129)
P4E_CPU2_PE3D_SLIMS_TX_DP13	C253	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3D_SLIMS_C_TX_DP13	(129)
P4E_CPU2_PE3D_SLIMS_TX_DP12	C255	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3D_SLIMS_C_TX_DP12	(129)
P4E_CPU2_PE3C_SLIMS_TX_DP11	C257	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3C_SLIMS_C_TX_DP11	(129)
P4E_CPU2_PE3C_SLIMS_TX_DP10	C259	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3C_SLIMS_C_TX_DP10	(129)
P4E_CPU2_PE3C_SLIMS_TX_DP9	C261	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3C_SLIMS_C_TX_DP9	(129)
P4E_CPU2_PE3B_SLIMS_TX_DP8	C263	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3B_SLIMS_C_TX_DP8	(129)
P4E_CPU2_PE3B_SLIMS_TX_DP7	C265	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3B_SLIMS_C_TX_DP7	(129)
P4E_CPU2_PE3B_SLIMS_TX_DP6	C267	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3B_SLIMS_C_TX_DP6	(129)
P4E_CPU2_PE3B_SLIMS_TX_DP5	C269	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3B_SLIMS_C_TX_DP5	(129)
P4E_CPU2_PE3B_SLIMS_TX_DP4	C271	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3B_SLIMS_C_TX_DP4	(129)
P4E_CPU2_PE3A_SLIMS_TX_DP3	C273	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3A_SLIMS_C_TX_DP3	(129)
P4E_CPU2_PE3A_SLIMS_TX_DP2	C275	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3A_SLIMS_C_TX_DP2	(129)
P4E_CPU2_PE3A_SLIMS_TX_DP1	C277	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3A_SLIMS_C_TX_DP1	(129)
P4E_CPU2_PE3A_SLIMS_TX_DP0	C279	2	1	0.22UF/6.3V	>>P4E_CPU2_PE3A_SLIMS_C_TX_DP0	(129)
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P4E_CPU2_PE2A_RISER2_TX_DN15	C279	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN15	(117)
P4E_CPU2_PE2A_RISER2_TX_DN14	C280	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN14	(117)
P4E_CPU2_PE2A_RISER2_TX_DN13	C282	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN13	(117)
P4E_CPU2_PE2A_RISER2_TX_DN12	C284	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN12	(117)
P4E_CPU2_PE2A_RISER2_TX_DN11	C286	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN11	(117)
P4E_CPU2_PE2A_RISER2_TX_DN10	C288	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN10	(117)
P4E_CPU2_PE2A_RISER2_TX_DN9	C290	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN9	(117)
P4E_CPU2_PE2A_RISER2_TX_DN8	C292	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN8	(117)
P4E_CPU2_PE2A_RISER2_TX_DN7	C294	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN7	(117)
P4E_CPU2_PE2A_RISER2_TX_DN6	C296	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN6	(117)
P4E_CPU2_PE2A_RISER2_TX_DN5	C298	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN5	(117)
P4E_CPU2_PE2A_RISER2_TX_DN4	C300	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN4	(117)
P4E_CPU2_PE2A_RISER2_TX_DN3	C302	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN3	(117)
P4E_CPU2_PE2A_RISER2_TX_DN2	C304	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN2	(117)
P4E_CPU2_PE2A_RISER2_TX_DN1	C306	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN1	(117)
P4E_CPU2_PE2A_RISER2_TX_DN0	C308	2	1	0.22UF/6.3V	>>P4E_CPU2_PE2A_RISER2_C_TX_DN0	(117)



CPU2R-17			
(17) UPL CPU1_CPU2_P2P0_DP19	T16	UPIO_RX_DP<19>	UPIO_TX_DP<19>
(17) UPL CPU1_CPU2_P2P0_DP18	N14	UPIO_RX_DP<18>	UPIO_TX_DP<18>
(17) UPL CPU1_CPU2_P2P0_DP17	R15	UPIO_RX_DP<17>	UPIO_TX_DP<17>
(17) UPL CPU1_CPU2_P2P0_DP16	V14	UPIO_RX_DP<16>	UPIO_TX_DP<16>
(17) UPL CPU1_CPU2_P2P0_DP15	U13	UPIO_RX_DP<15>	UPIO_TX_DP<15>
(17) UPL CPU1_CPU2_P2P0_DP14	AX15	UPIO_RX_DP<14>	UPIO_TX_DP<14>
(17) UPL CPU1_CPU2_P2P0_DP13	AB14	UPIO_RX_DP<13>	UPIO_TX_DP<13>
(17) UPL CPU1_CPU2_P2P0_DP12	AG15	UPIO_RX_DP<12>	UPIO_TX_DP<12>
(17) UPL CPU1_CPU2_P2P0_DP11	AD14	UPIO_RX_DP<11>	UPIO_TX_DP<11>
(17) UPL CPU1_CPU2_P2P0_DP10	AG13	UPIO_RX_DP<10>	UPIO_TX_DP<10>
(17) UPL CPU1_CPU2_P2P0_DP9	AF14	UPIO_RX_DP<9>	UPIO_TX_DP<9>
(17) UPL CPU1_CPU2_P2P0_DP8	AL15	UPIO_RX_DP<8>	UPIO_TX_DP<8>
(17) UPL CPU1_CPU2_P2P0_DP7	AW15	UPIO_RX_DP<7>	UPIO_TX_DP<7>
(17) UPL CPU1_CPU2_P2P0_DP6	AN15	UPIO_RX_DP<6>	UPIO_TX_DP<6>
(17) UPL CPU1_CPU2_P2P0_DP5	AT14	UPIO_RX_DP<5>	UPIO_TX_DP<5>
(17) UPL CPU1_CPU2_P2P0_DP4	AB14	UPIO_RX_DP<4>	UPIO_TX_DP<4>
(17) UPL CPU1_CPU2_P2P0_DP3	AP16	UPIO_RX_DP<3>	UPIO_TX_DP<3>
(17) UPL CPU1_CPU2_P2P0_DP2	AU17	UPIO_RX_DP<2>	UPIO_TX_DP<2>
(17) UPL CPU1_CPU2_P2P0_DP1	AN17	UPIO_RX_DP<1>	UPIO_TX_DP<1>
(17) UPL CPU1_CPU2_P2P0_D0	RI17	UPIO_RX_DP<0>	UPIO_TX_DP<0>
(17) UPL CPU1_CPU2_P2P0_DN19	R16	UPIO_RX_DN<19>	UPIO_TX_DN<19>
(17) UPL CPU1_CPU2_P2P0_DN18	L15	UPIO_RX_DN<18>	UPIO_TX_DN<18>
(17) UPL CPU1_CPU2_P2P0_DN17	U15	UPIO_RX_DN<17>	UPIO_TX_DN<17>
(17) UPL CPU1_CPU2_P2P0_DN16	W15	UPIO_RX_DN<16>	UPIO_TX_DN<16>
(17) UPL CPU1_CPU2_P2P0_DN15	Y14	UPIO_RX_DN<15>	UPIO_TX_DN<15>
(17) UPL CPU1_CPU2_P2P0_DN14	Y14	UPIO_RX_DN<14>	UPIO_TX_DN<14>
(17) UPL CPU1_CPU2_P2P0_DN13	Y14	UPIO_RX_DN<13>	UPIO_TX_DN<13>
(17) UPL CPU1_CPU2_P2P0_DN12	Y14	UPIO_RX_DN<12>	UPIO_TX_DN<12>
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(17) UPL CPU1_CPU2_P2P0_DN5	Y14	UPIO_RX_DN<5>	UPIO_TX_DN<5>
(17) UPL CPU1_CPU2_P2P0_DN4	Y14	UPIO_RX_DN<4>	UPIO_TX_DN<4>
(17) UPL CPU1_CPU2_P2P0_DN3	Y14	UPIO_RX_DN<3>	UPIO_TX_DN<3>
(17) UPL CPU1_CPU2_P2P0_DN2	Y14	UPIO_RX_DN<2>	UPIO_TX_DN<2>
(17) UPL CPU1_CPU2_P2P0_DN1	Y14	UPIO_RX_DN<1>	UPIO_TX_DN<1>
(17) UPL CPU1_CPU2_P2P0_D0	Y14	UPIO_RX_DN<0>	UPIO_TX_DN<0>

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CPU2R-19			
(17) UPL CPU1_CPU2_P2P2_DP19	ED12	UPI2_RX_DP<19>	UPI2_TX_DP<19>
(17) UPL CPU1_CPU2_P2P2_DP18	EB12	UPI2_RX_DP<18>	UPI2_TX_DP<18>
(17) UPL CPU1_CPU2_P2P2_DP17	EC13	UPI2_RX_DP<17>	UPI2_TX_DP<17>
(17) UPL CPU1_CPU2_P2P2_DP16	EB10	UPI2_RX_DP<16>	UPI2_TX_DP<16>
(17) UPL CPU1_CPU2_P2P2_DP15	DY10	UPI2_RX_DP<15>	UPI2_TX_DP<15>
(17) UPL CPU1_CPU2_P2P2_DP14	DW9	UPI2_RX_DP<14>	UPI2_TX_DP<14>
(17) UPL CPU1_CPU2_P2P2_DP13	DW11	UPI2_RX_DP<13>	UPI2_TX_DP<13>
(17) UPL CPU1_CPU2_P2P2_DP12	DY12	UPI2_RX_DP<12>	UPI2_TX_DP<12>
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(17) UPL CPU1_CPU2_P2P2_DP10	DN11	UPI2_RX_DP<10>	UPI2_TX_DP<10>
(17) UPL CPU1_CPU2_P2P2_DP9	DM10	UPI2_RX_DP<9>	UPI2_TX_DP<9>
(17) UPL CPU1_CPU2_P2P2_DP8	DM10	UPI2_RX_DP<8>	UPI2_TX_DP<8>
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(17) UPL CPU1_CPU2_P2P2_DN17	EF10	UPI2_RX_DN<17>	UPI2_TX_DN<17>
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(17) UPL CPU1_CPU2_P2P2_DN13	DY11	UPI2_RX_DN<13>	UPI2_TX_DN<13>
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CPU2R-18			
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(17) UPL CPU1_CPU2_P1P1_DP3	W83	UPI1_RX_DP<16>	UPI1_TX_DP<16>
(17) UPL CPU1_CPU2_P1P1_DP4	AA85	UPI1_RX_DP<15>	UPI1_TX_DP<15>
(17) UPL CPU1_CPU2_P1P1_DP5	U83	UPI1_RX_DP<14>	UPI1_TX_DP<14>
(17) UPL CPU1_CPU2_P1P1_DP6	Y86	UPI1_RX_DP<13>	UPI1_TX_DP<13>
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(17) UPL CPU1_CPU2_P1P1_DP13	W85	UPI1_RX_DP<6>	UPI1_TX_DP<6>
(17) UPL CPU1_CPU2_P1P1_DP14	N85	UPI1_RX_DP<5>	UPI1_TX_DP<5>
(17) UPL CPU1_CPU2_P1P1_DP15	H84	UPI1_RX_DP<4>	UPI1_TX_DP<4>
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(17) UPL CPU1_CPU2_P1P1_DP18	G81	UPI1_RX_DP<1>	UPI1_TX_DP<1>
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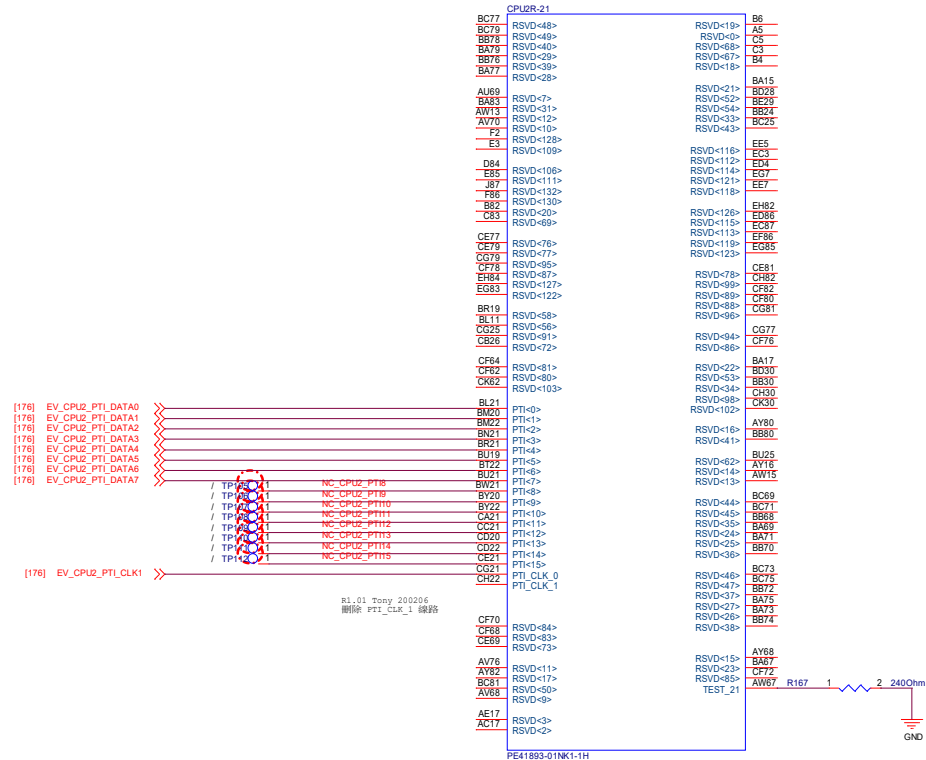
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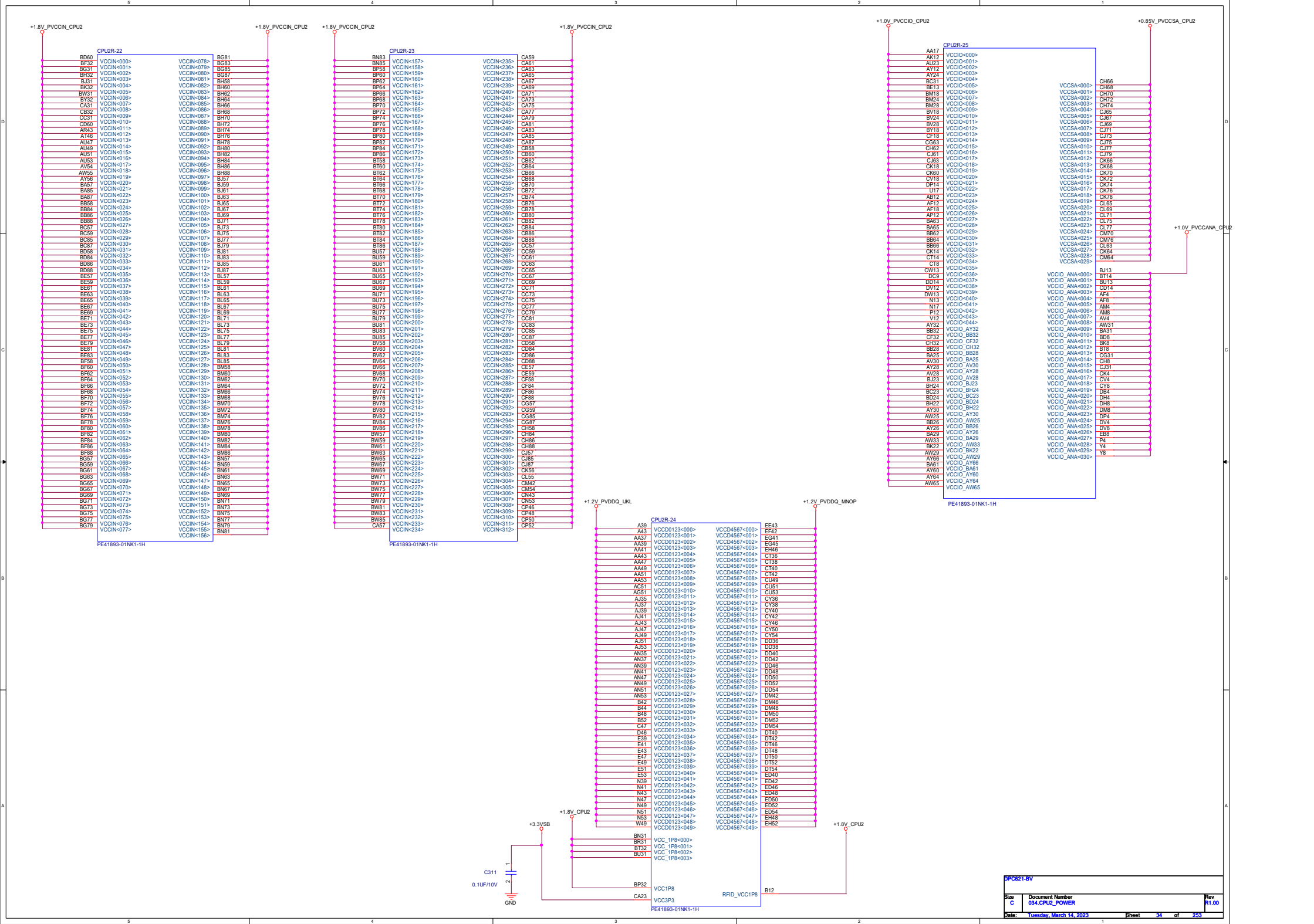
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(17) UPL CPU1_CPU2_P3P3_DP12	L85	UPI3_RX_DP<12>	UPI3_TX_DP<12>
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(17) UPL CPU1_CPU2_P3P3_DN17	DT18	UPI3_RX_DN<17>	UPI3_TX_DN<17>
(17) UPL CPU1_CPU2_P3P3_DN16	DR17	UPI3_RX_DN<16>	UPI3_TX_DN<16>
(17) UPL CPU1_CPU2_P3P3_DN15	DN17	UPI3_RX_DN<15>	UPI3_TX_DN<15>
(17) UPL CPU1_CPU2_P3P3_DN14	DK16	UPI3_RX_DN<14>	UPI3_TX_DN<14>
(17) UPL CPU1_CPU2_P3P3_DN13	DL15	UPI3_RX_DN<13>	UPI3_TX_DN<13>
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(17) UPL CPU1_CPU2_P3P3_DN3	CT16	UPI3_RX_DN<3>	UPI3_TX_DN<3>
(17) UPL CPU1_CPU2_P3P3_DN2	CN17	UPI3_RX_DN<2>	UPI3_TX_DN<2>
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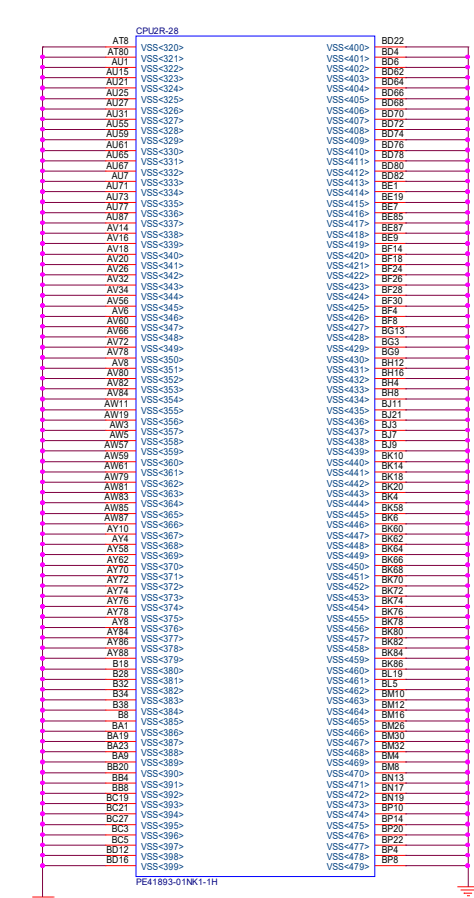
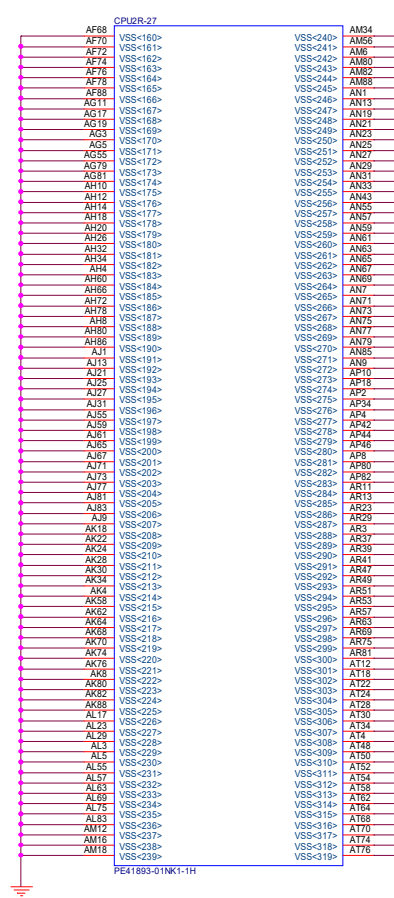
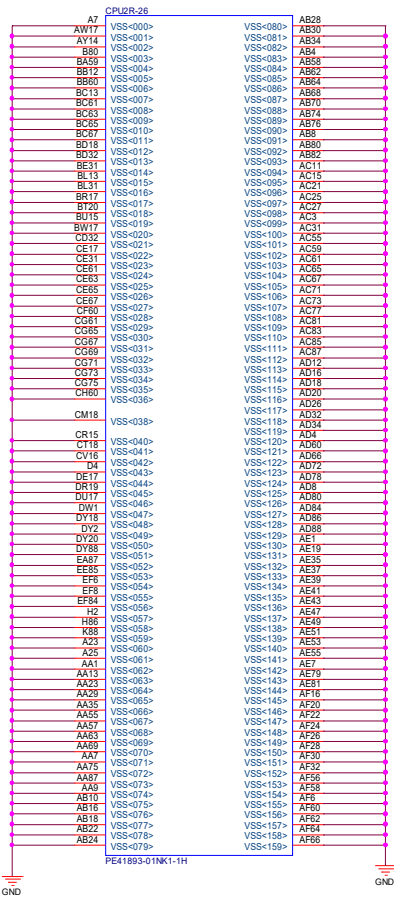
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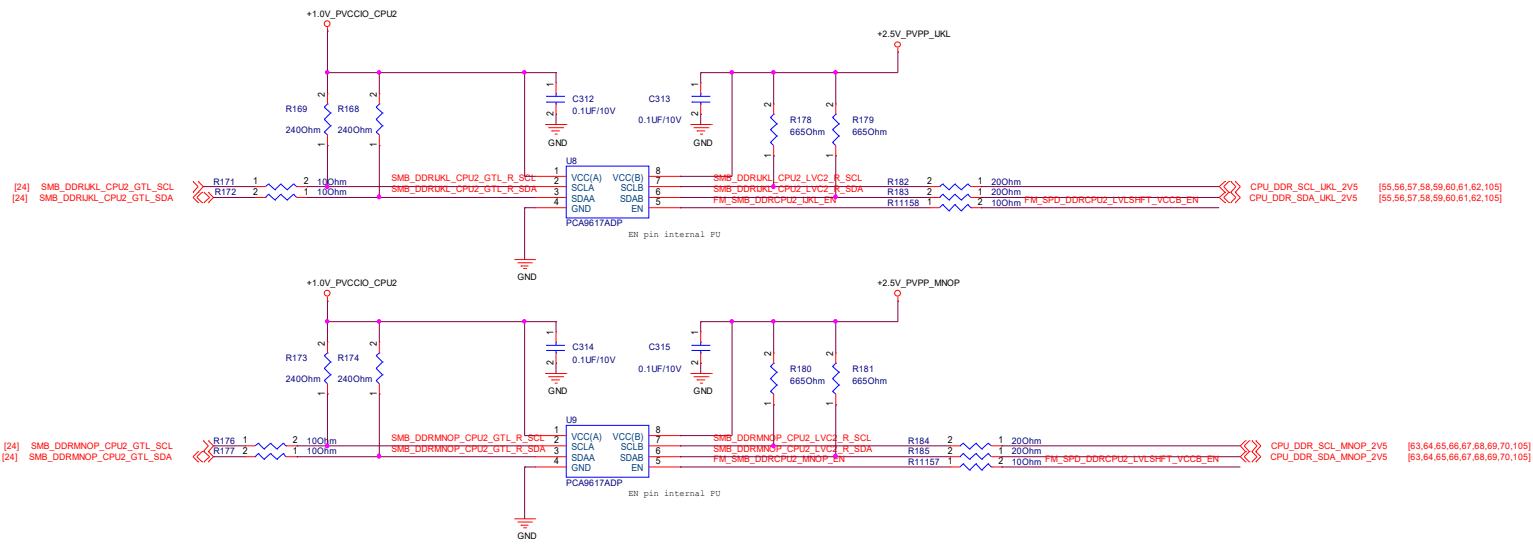




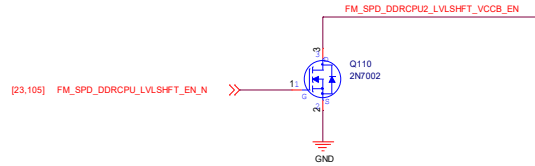






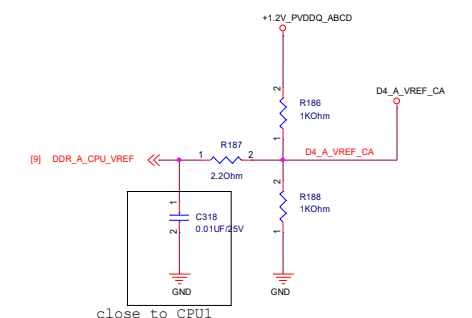
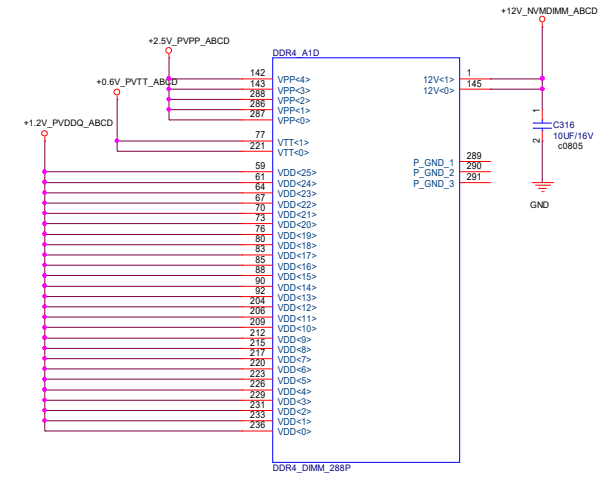


R1.01 Tony 191226  
修改DDR SMBus EN(U8,U9)線路，改為BMC控制





**BOM:Change 12G02411288EAK to 12G02410288XAK**



## DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

DPC621-BV

Size  
C

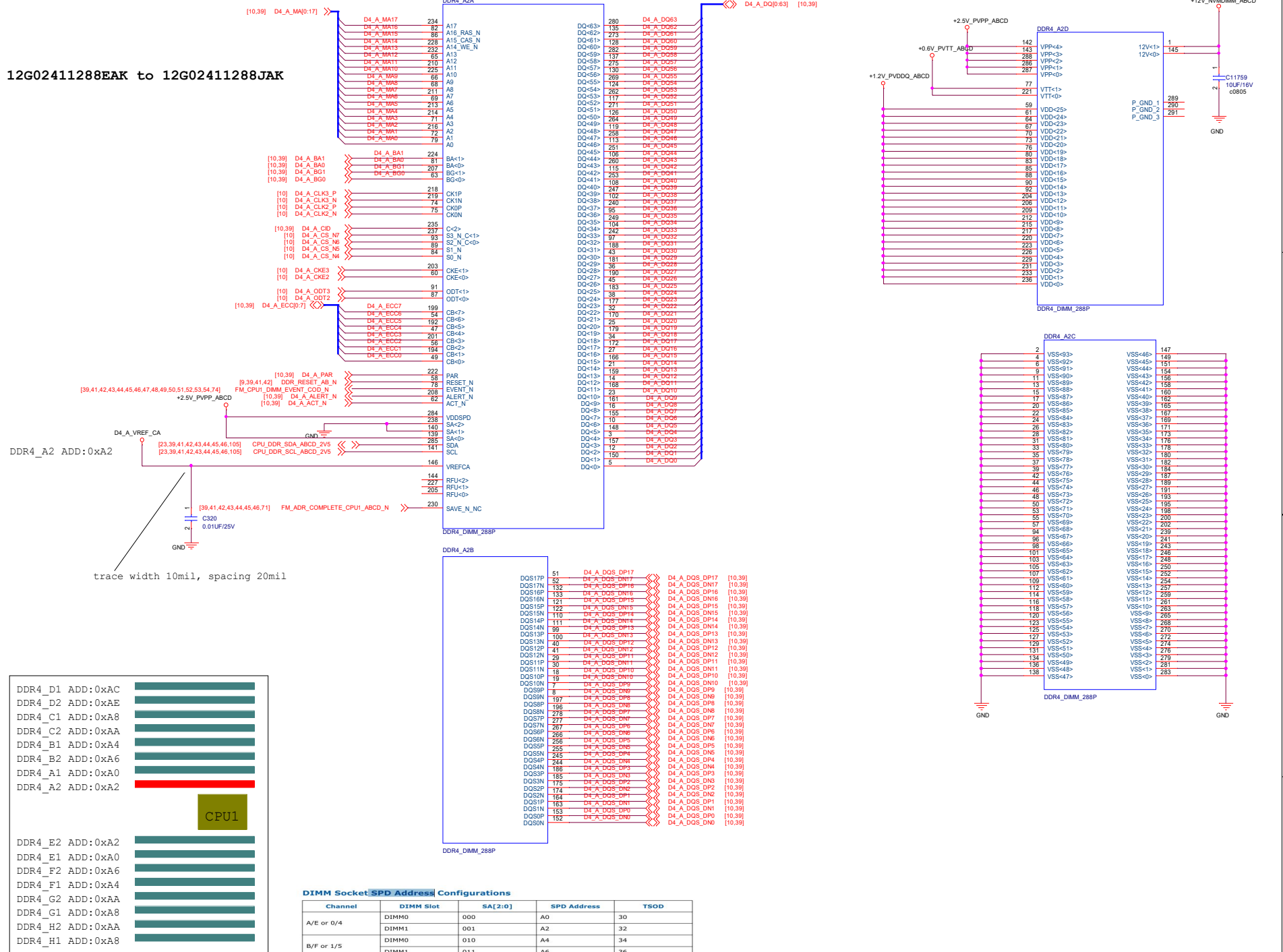
Document Number  
039.CPU1\_DDR4\_CH\_A1

Rev  
R1.00

Date: Tuesday, March 14, 2023

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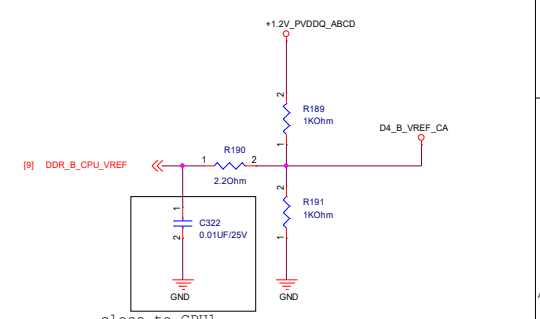
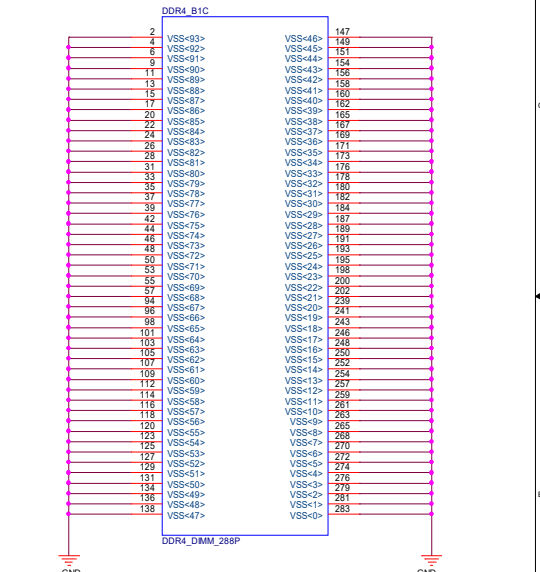
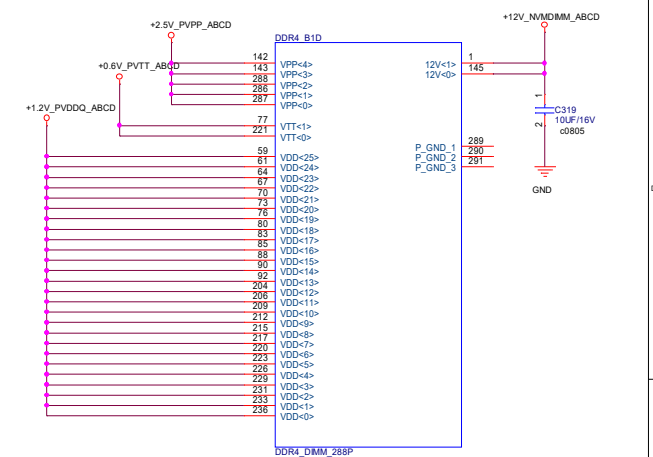
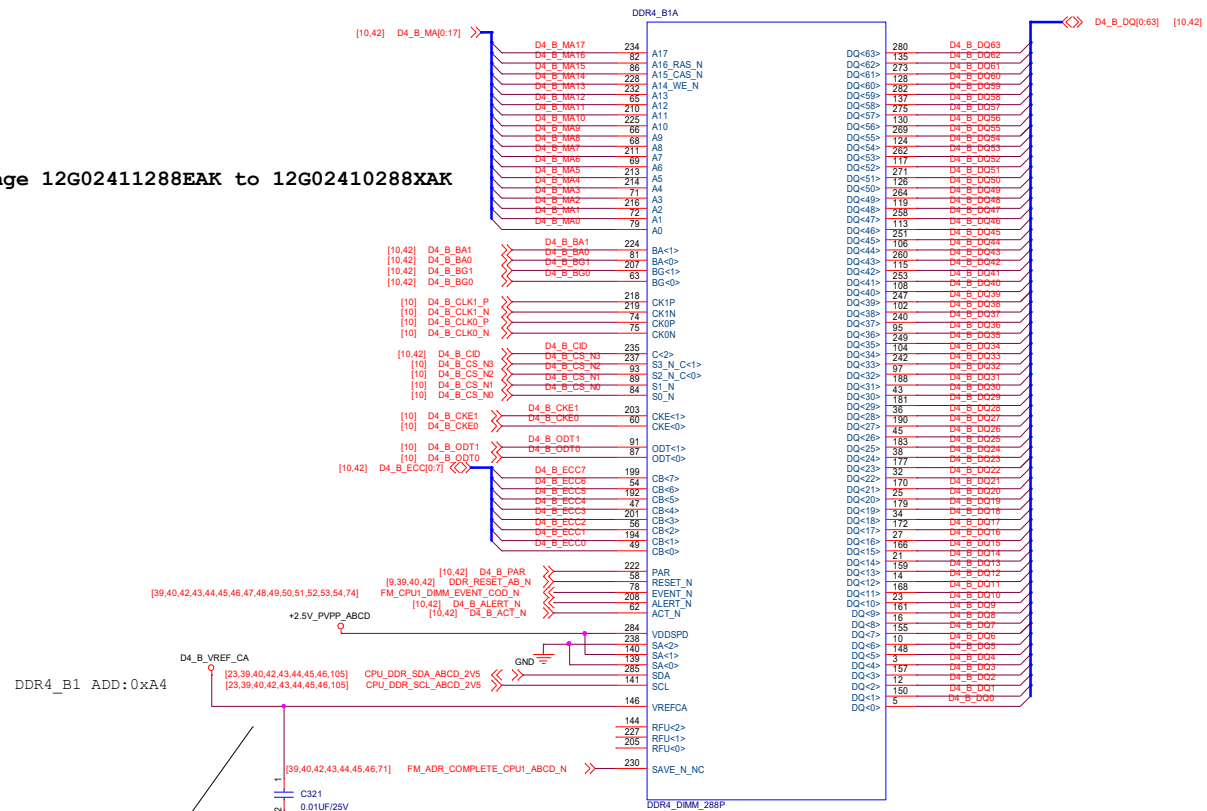
BOM:Change 12G02411288EAK to 12G02411288JAK



### DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

**BOM:Change 12G02411288EAK to 12G02410288XAK**



DDR4_D1	ADD: 0xA	
DDR4_D2	ADD: 0xA	
DDR4_C1	ADD: 0xA	
DDR4_C2	ADD: 0xA	
DDR4_B1	ADD: 0xA	
DDR4_B2	ADD: 0xA	
DDR4_A1	ADD: 0xA	
DDR4_A2	ADD: 0xA	

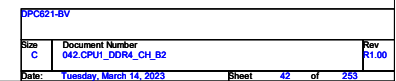
CPU1

DDR4_E2	ADD: 0xA2	
DDR4_E1	ADD: 0xA0	
DDR4_F2	ADD: 0xA6	
DDR4_F1	ADD: 0xA4	
DDR4_G2	ADD: 0xAA	
DDR4_G1	ADD: 0xA8	
DDR4_H2	ADD: 0xA4	
DDR4_H1	ADD: 0xA8	

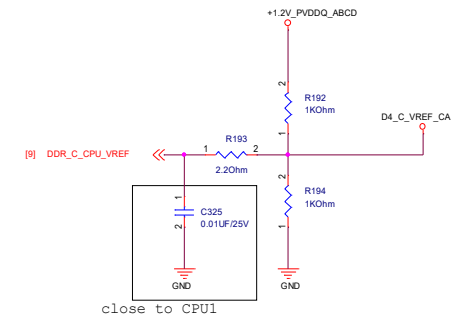
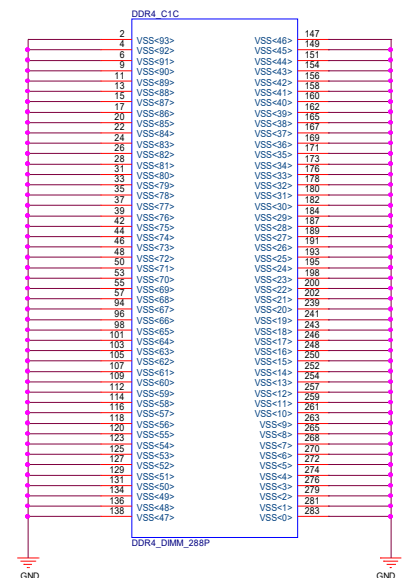
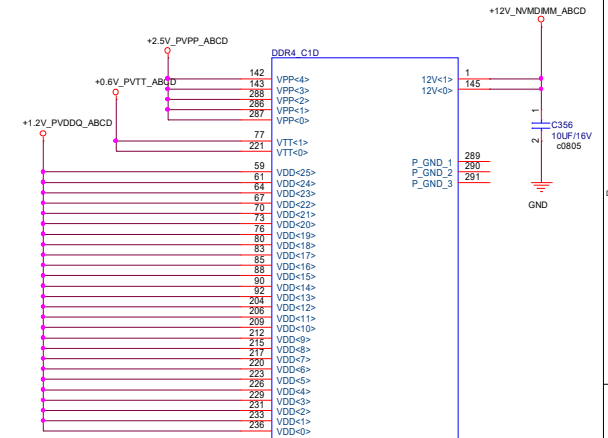
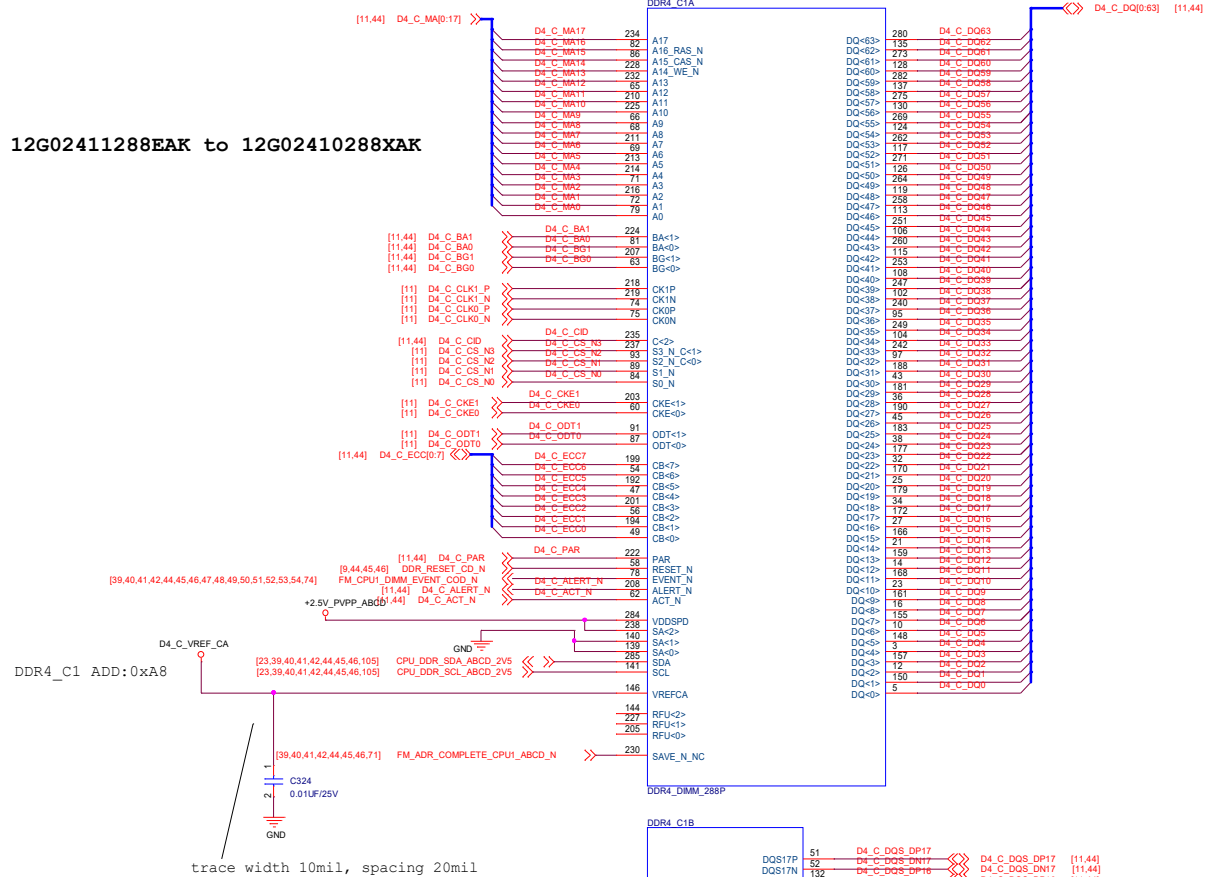
## DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

BOM:Change 12G02411288EAK to 12G02411288JAK



R1.01  
BOM:Change 12G02411288EAK to 12G02410288XAK



## DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

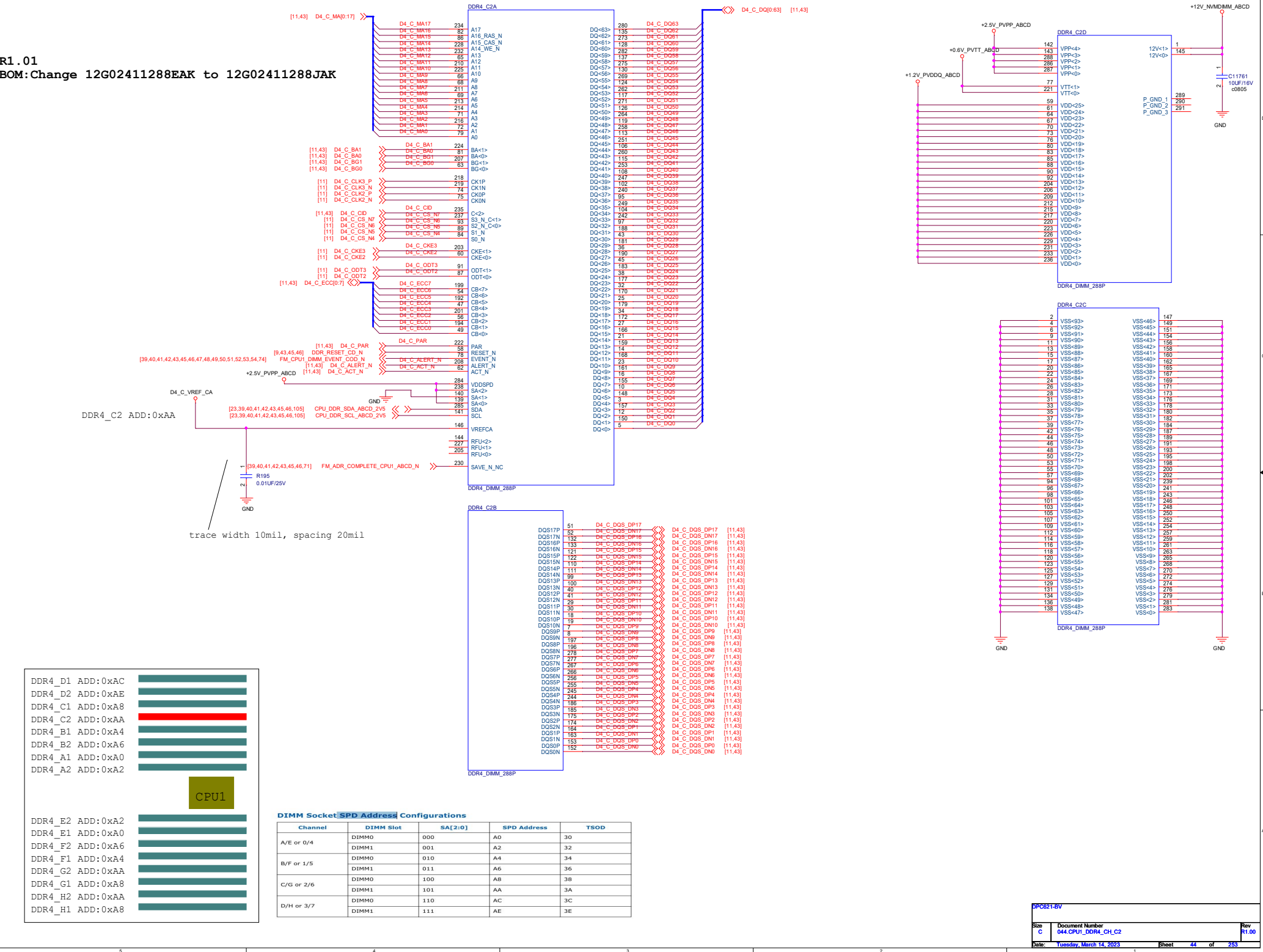
DDR4_D1	ADD: 0xA8	
DDR4_D2	ADD: 0xA8	
DDR4_C1	ADD: 0xA8	
DDR4_C2	ADD: 0xA8	
DDR4_B1	ADD: 0xA4	
DDR4_B2	ADD: 0xA6	
DDR4_A1	ADD: 0xA0	
DDR4_A2	ADD: 0xA2	

CPU1

DDR4_E2	ADD: 0xA2	
DDR4_E1	ADD: 0xA0	
DDR4_F2	ADD: 0xA6	
DDR4_F1	ADD: 0xA4	
DDR4_G2	ADD: 0xAA	
DDR4_G1	ADD: 0xA8	
DDR4_H2	ADD: 0xA4	
DDR4_H1	ADD: 0xA8	

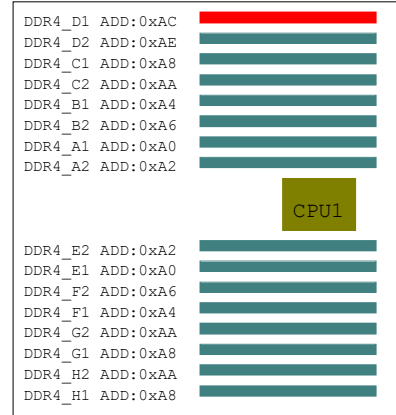
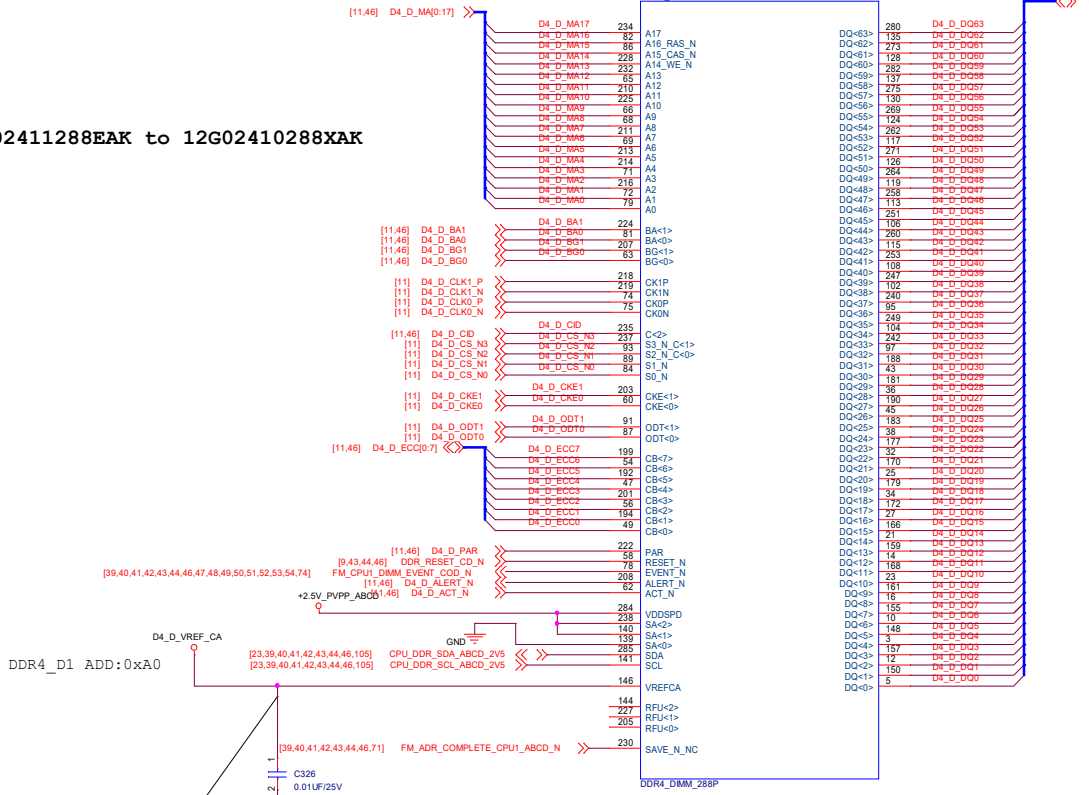


R1.01  
BOM:Change 12G02411288EAK to 12G02411288JAK

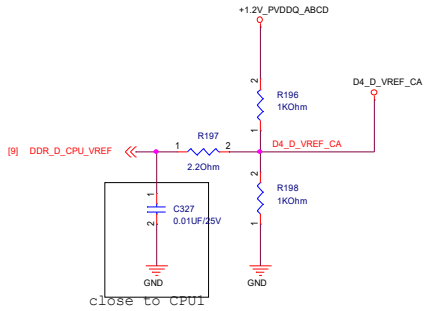
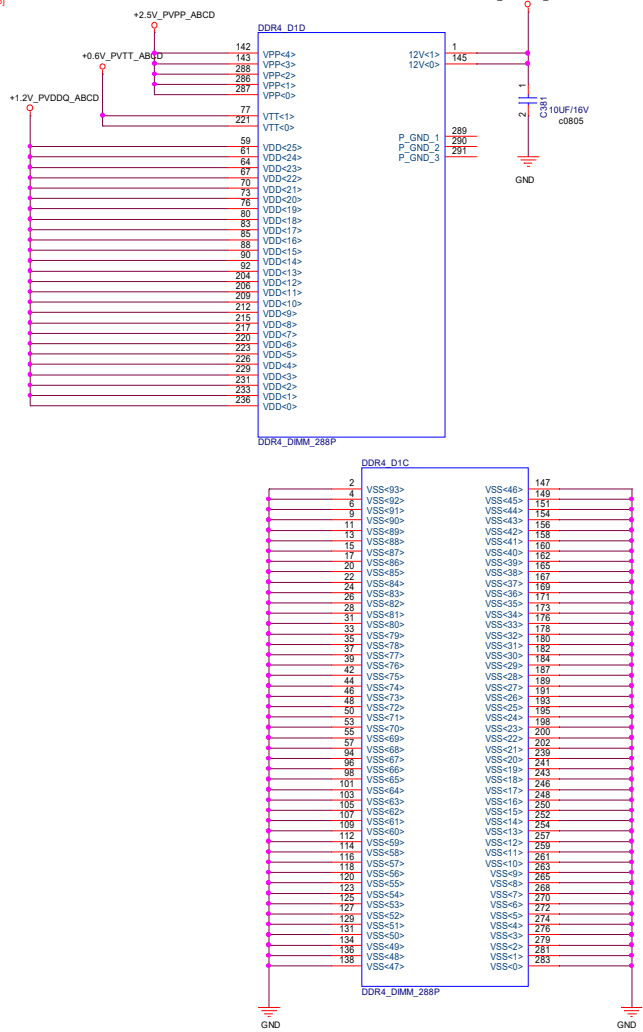




R1.01  
BOM:Change 12G02411288EAK to 12G02410288XAK



DIMM Socket SPD Address Configurations					
Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD	
A/E or 0/4	DIMM0	000	A0	30	
	DIMM1	001	A2	32	
	DIMM0	010	A4	34	
B/F or 1/5	DIMM1	011	A6	36	
	DIMM0	100	A8	38	
C/G or 2/6	DIMM1	101	AA	3A	
	DIMM0	110	AC	3C	
D/H or 3/7	DIMM1	111	AE	3E	

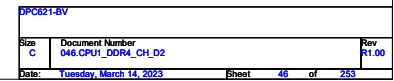


```
DDR4_D1 ADD:0xAC
DDR4_D2 ADD:0xAE
DDR4_C1 ADD:0xA8
DDR4_C2 ADD:0xAA
DDR4_B1 ADD:0xA4
DDR4_B2 ADD:0xA6
DDR4_A1 ADD:0xA0
DDR4_A2 ADD:0xA2
```

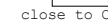
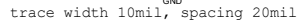
```
DDR4_E2 ADD:0xA2
DDR4_E1 ADD:0xA0
DDR4_F2 ADD:0xA6
DDR4_F1 ADD:0xA4
DDR4_G2 ADD:0xAA
DDR4_G1 ADD:0xA8
DDR4_H2 ADD:0xAA
DDR4_H1 ADD:0xA8
```

## DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



**BOM:Change 12G02411288EAK to 12G02410288XAK**

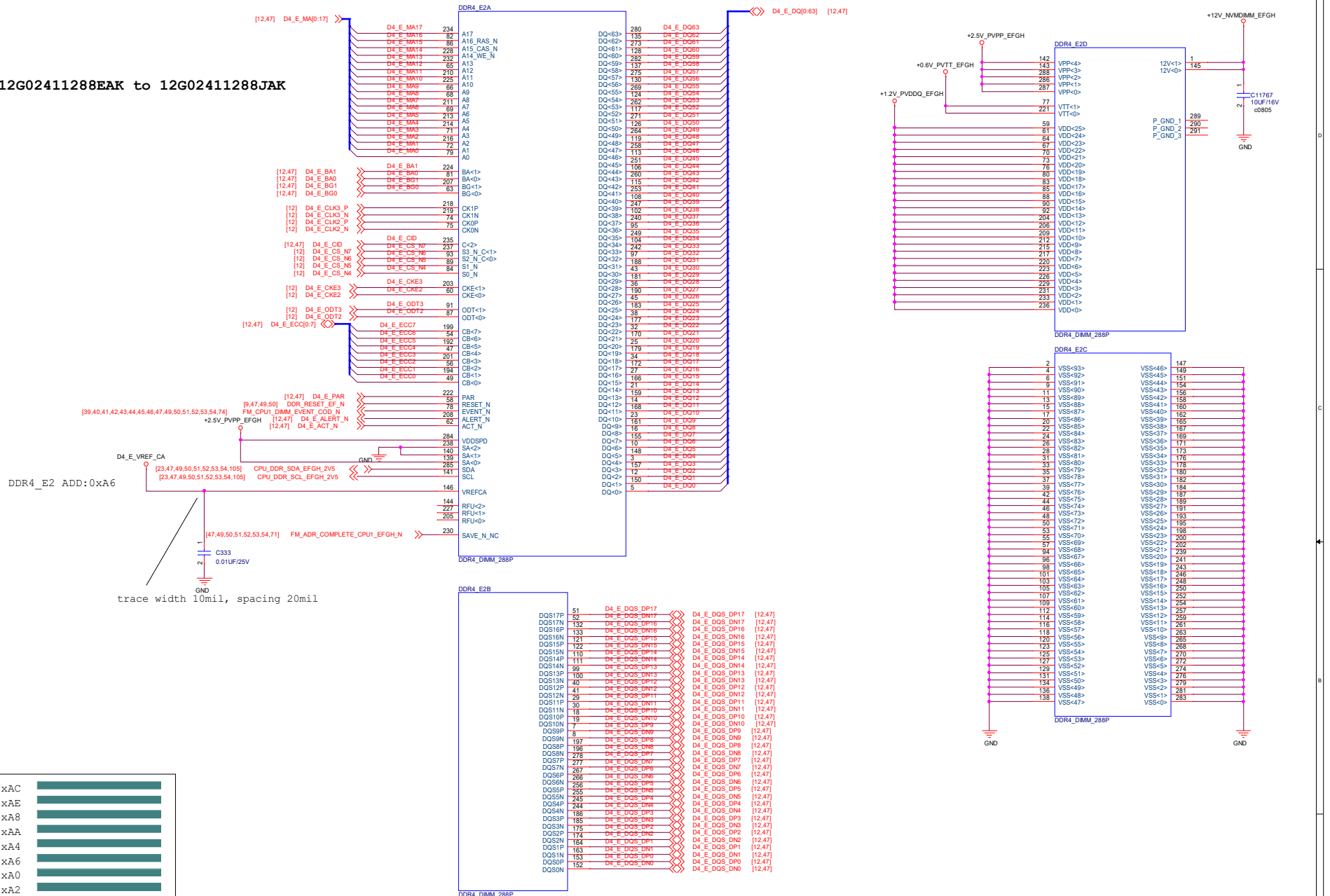


Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

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C	047.CPU1_DDR4_CH_E1	R1.00

R1.01

BOM:Change 12G02411288EAK to 12G02411288JAK



DDR4\_D1 ADD:0xAC  
DDR4\_D2 ADD:0xAE  
DDR4\_C1 ADD:0xA8  
DDR4\_C2 ADD:0xAA  
DDR4\_B1 ADD:0xA4  
DDR4\_B2 ADD:0xA6  
DDR4\_A1 ADD:0xA0  
DDR4\_A2 ADD:0xA2

CPU1

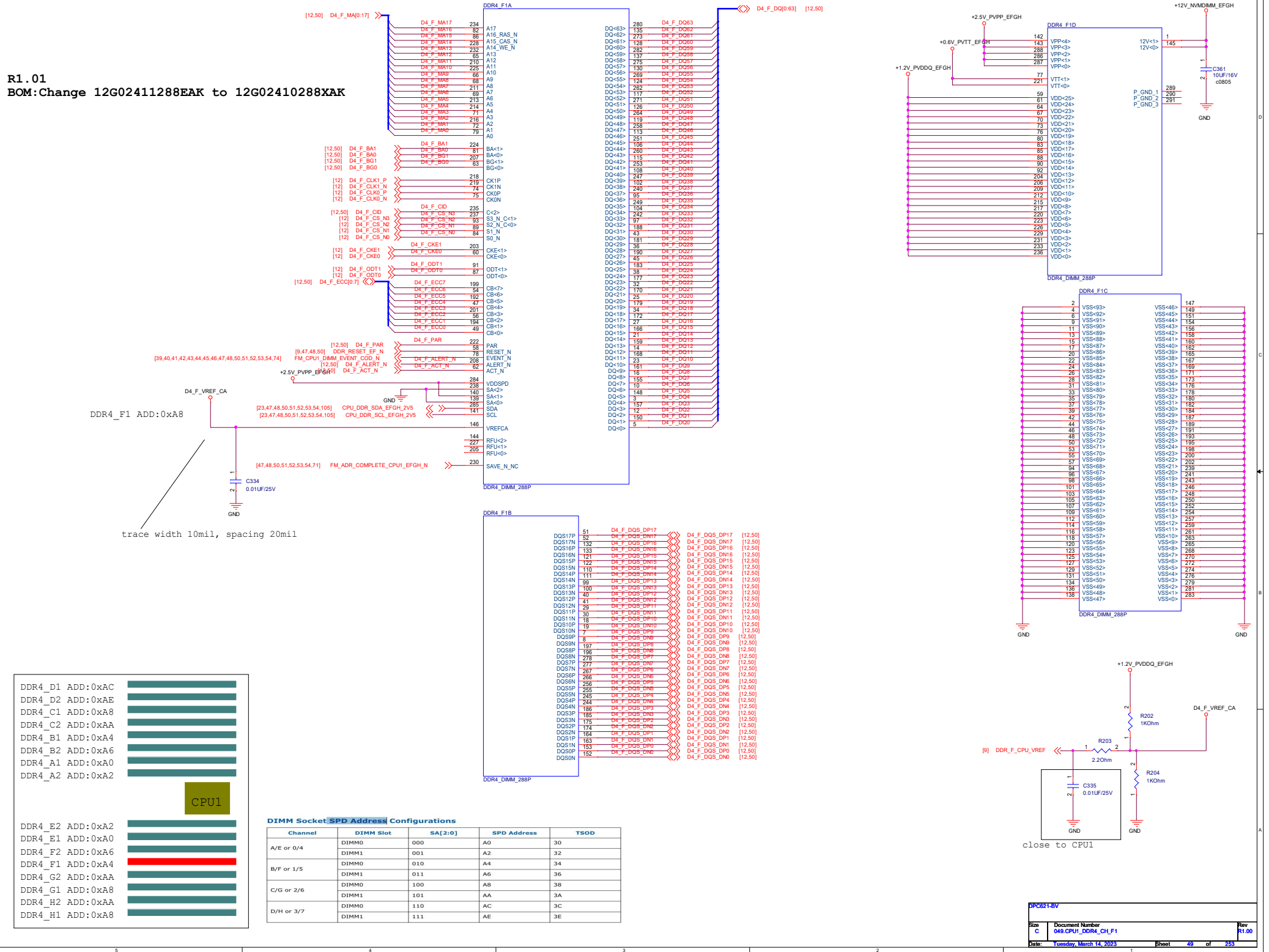
DDR4\_E2 ADD:0xA2  
DDR4\_E1 ADD:0xA0  
DDR4\_F2 ADD:0xA6  
DDR4\_F1 ADD:0xA4  
DDR4\_G2 ADD:0xAA  
DDR4\_G1 ADD:0xA8  
DDR4\_H2 ADD:0xAA  
DDR4\_H1 ADD:0xA8

DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
	DIMM0	010	A4	34
B/F or 1/5	DIMM1	011	A6	36
	DIMM0	100	A8	38
C/G or 2/6	DIMM1	101	AA	3A
	DIMM0	110	AC	3C
D/H or 3/7	DIMM1	111	AE	3E

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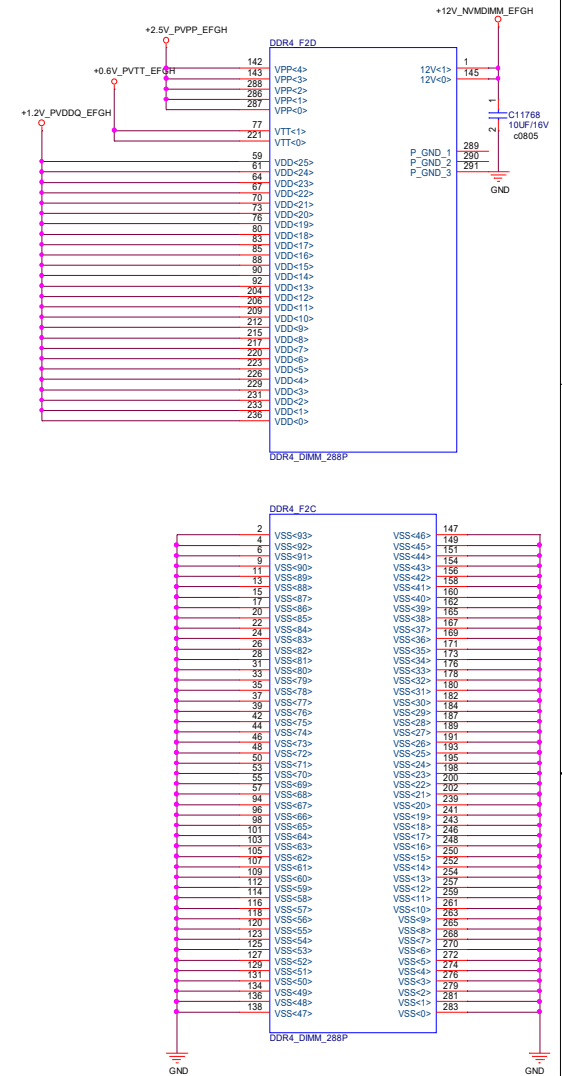
BOM:Change 12G02411288EAK to 12G02410288XAK



Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



**BOM:Change 12G02411288EAK to 12G02411288JAK**

CPU1

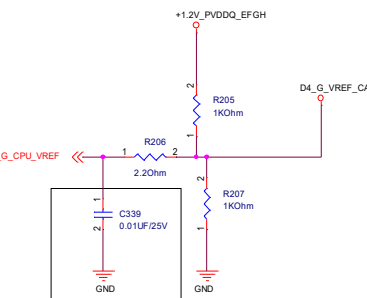
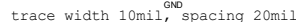
DDR4_E2	ADD: 0xA2	
DDR4_E1	ADD: 0xA0	
DDR4_F2	ADD: 0xA6	
DDR4_F1	ADD: 0xA4	
DDR4_G2	ADD: 0xAA	
DDR4_G1	ADD: 0xA8	
DDR4_H2	ADD: 0xA4	
DDR4_H1	ADD: 0xA8	

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

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C	050.CPU1_DDR4_CH_F2	R1.00
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**BOM:Change 12G02411288EAK to 12G02410288XAK**



close to CPU1

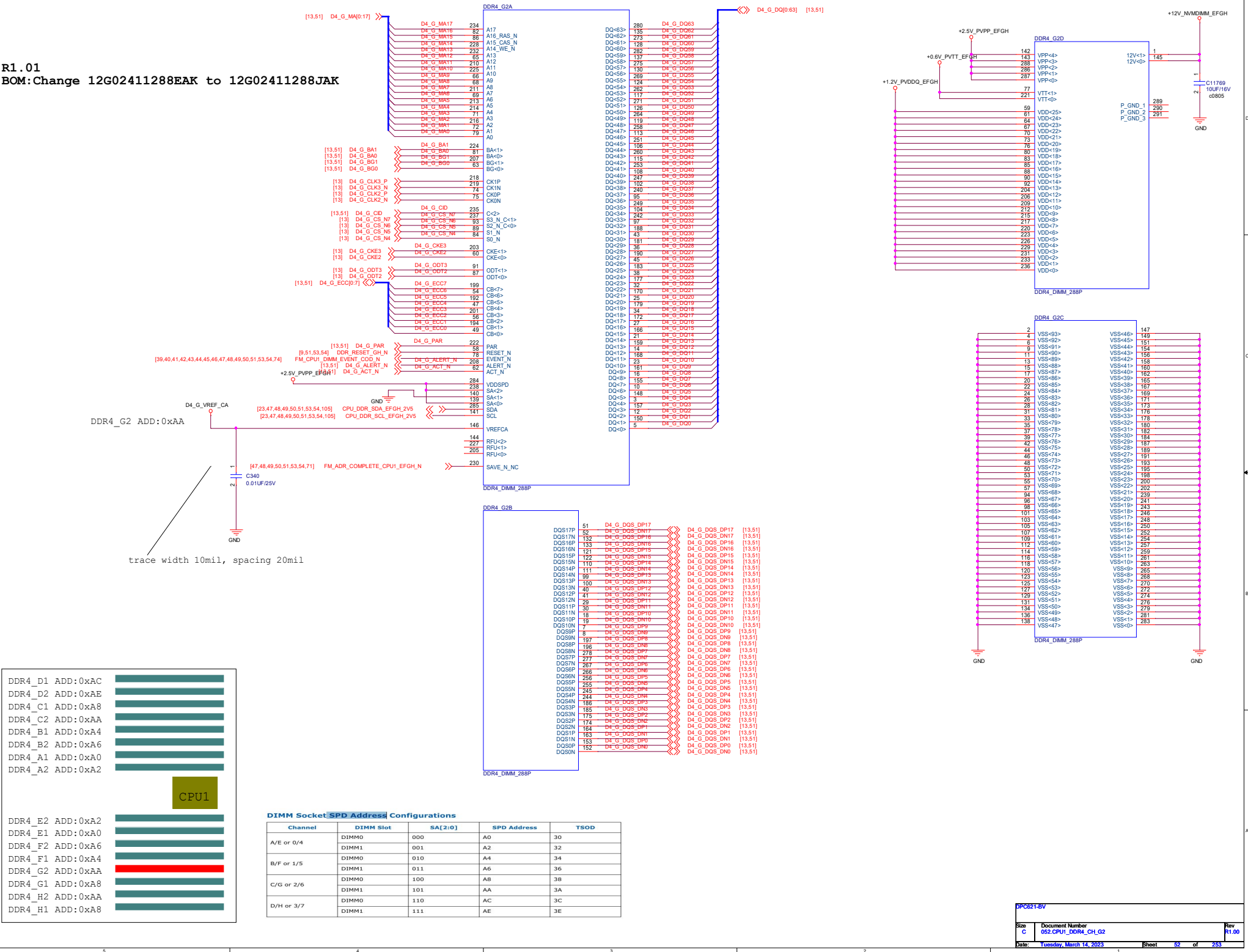
Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

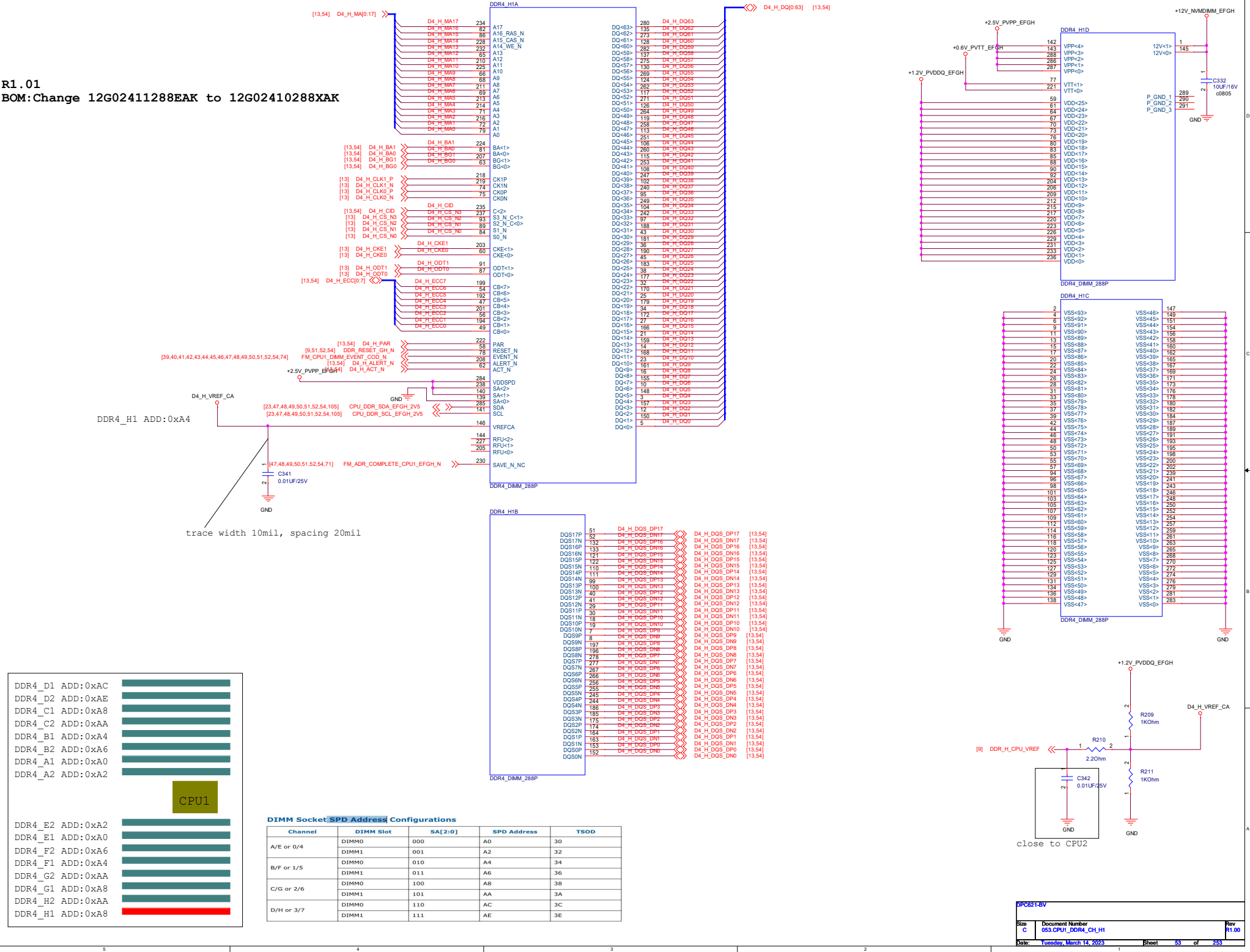
Size	Document Number	Rev
C	051.CPU1_DDR4_CH_G1	R1.0
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Size	Document Number	Rev
C	051.CPU1_DDR4_CH_G1	R1.0
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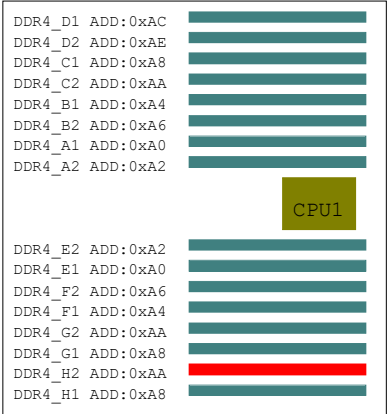
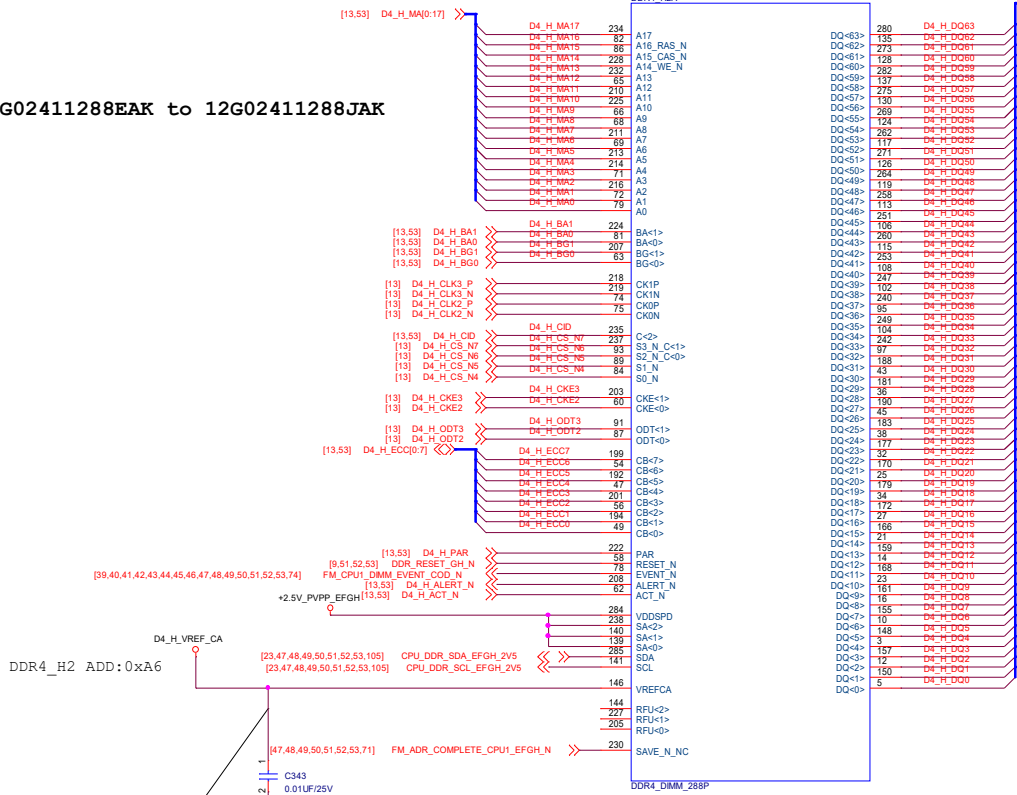
R1.01  
BOM:Change 12G02411288EAK to 12G02411288JAK



R1.01  
BOM:Change 12G02411288EAK to 12G02410288XAK

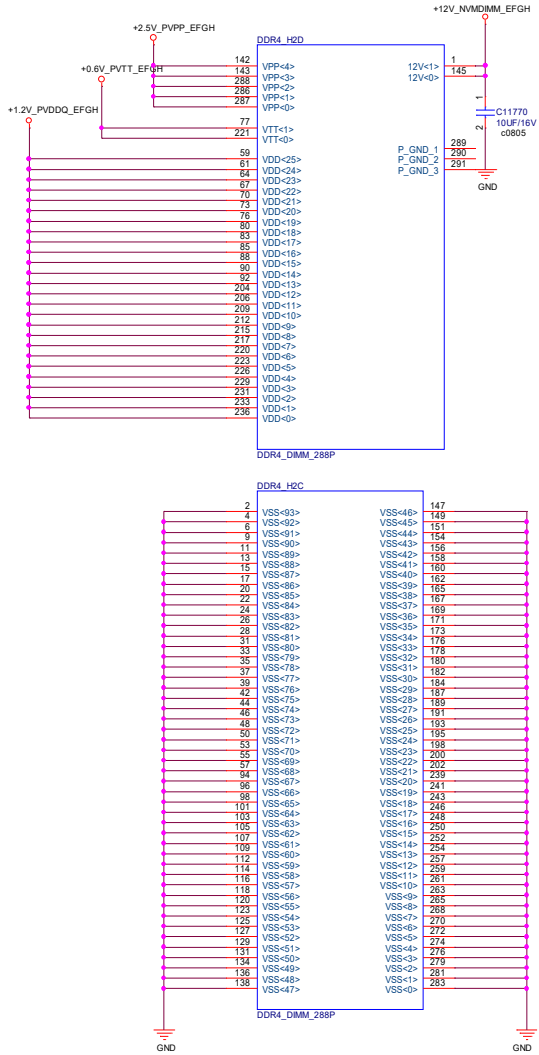


R1.01  
BOM:Change 12G02411288EAK to 12G02411288JAK

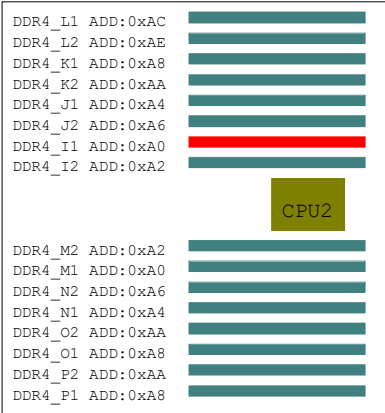


DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
	DIMM0	010	A4	34
B/F or 1/5	DIMM1	011	A6	36
	DIMM0	100	A8	38
	DIMM1	101	AA	3A
C/G or 2/6	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



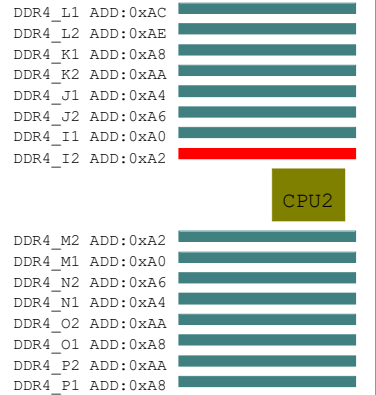
**BOM:Change 12G02411288EAK to 12G02410288XAK**



Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



**BOM:Change 12G02411288EAK to 12G02411288JAK**

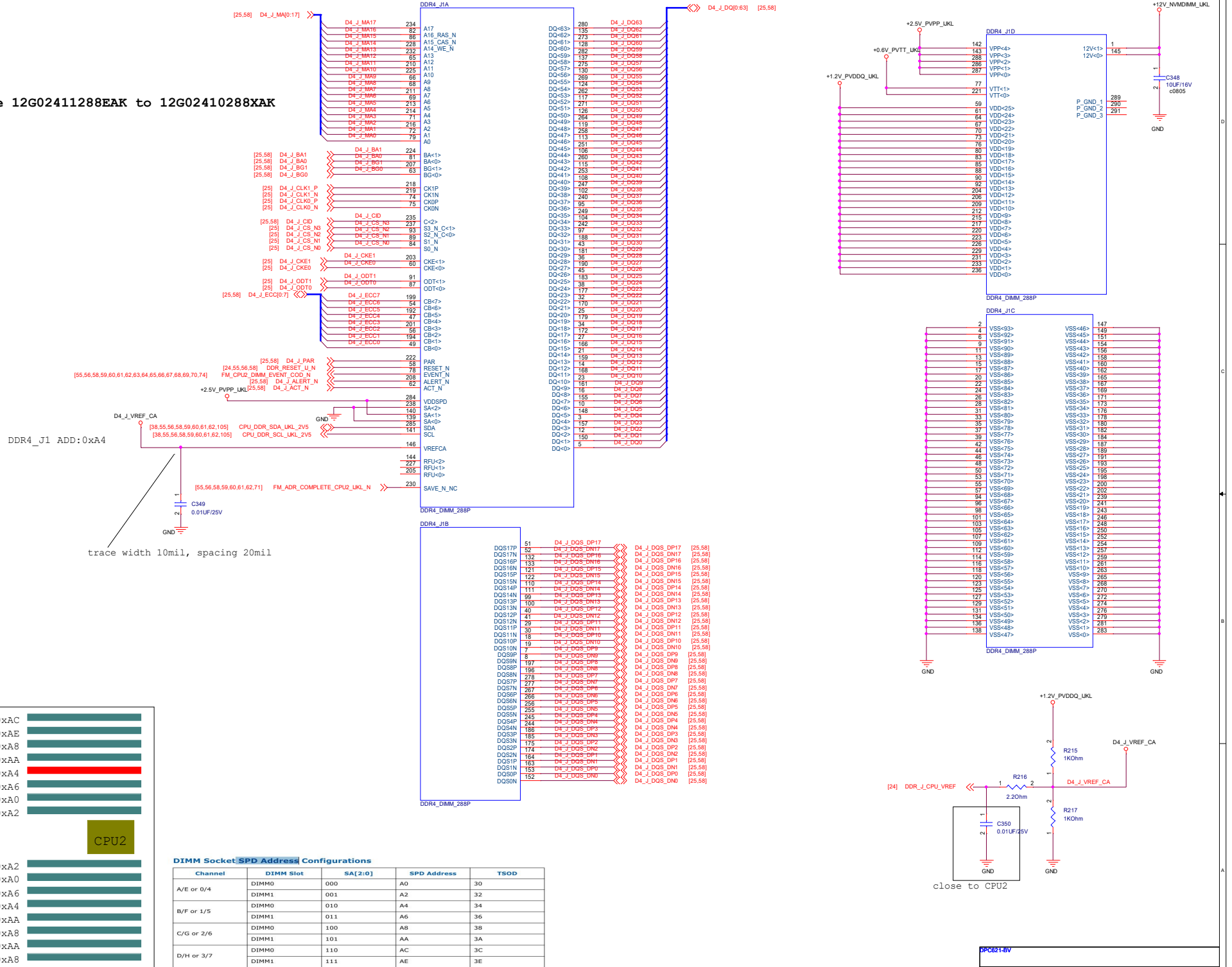


Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



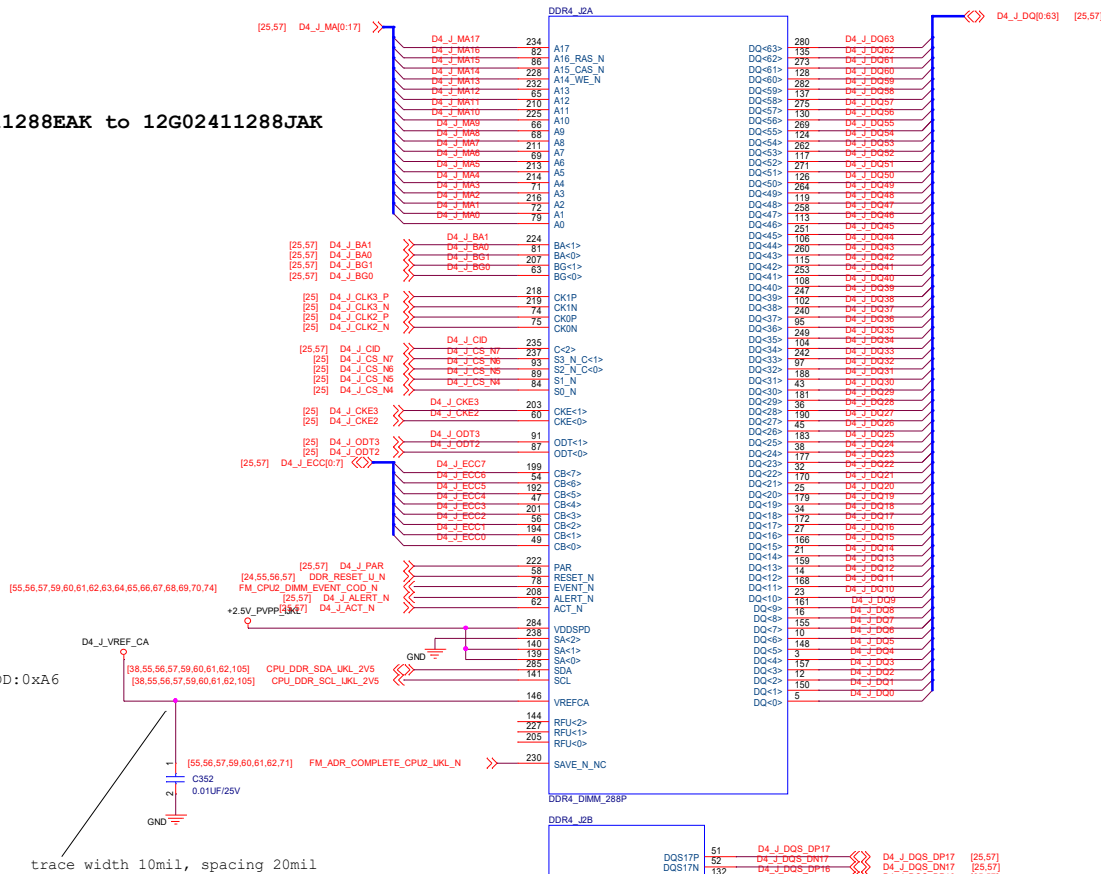
R1.01

BOM:Change 12G02411288EAK to 12G02410288XAK



PCB21-3V

R1.01  
BOM:Change 12G02411288EAK to 12G02411288JAK

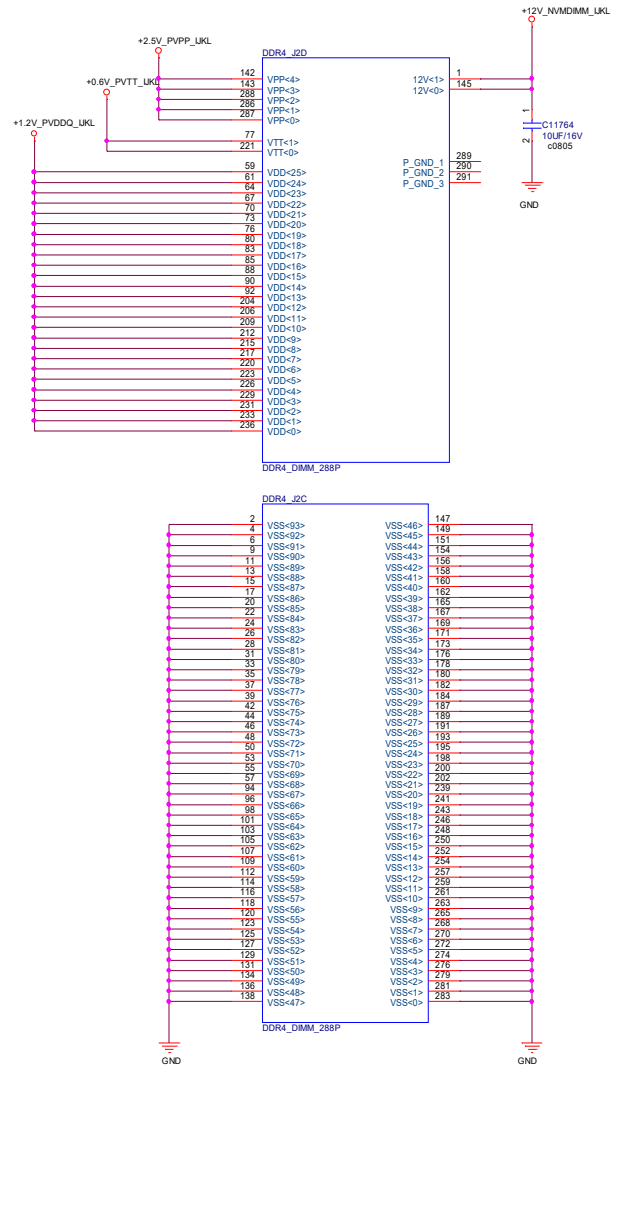


DDR4_L1	ADD:0xA6
DDR4_L2	ADD:0xA6
DDR4_K1	ADD:0xA8
DDR4_K2	ADD:0xA8
DDR4_J1	ADD:0xA4
DDR4_J2	ADD:0xA6
DDR4_I1	ADD:0xA0
DDR4_I2	ADD:0xA2

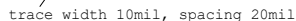
CPU2

DDR4_M2	ADD:0xA2
DDR4_M1	ADD:0xA0
DDR4_N2	ADD:0xA6
DDR4_N1	ADD:0xA4
DDR4_O2	ADD:0xA8
DDR4_O1	ADD:0xA8
DDR4_P2	ADD:0xA8
DDR4_P1	ADD:0xA8

DIMM Socket SPD Address Configurations				
Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

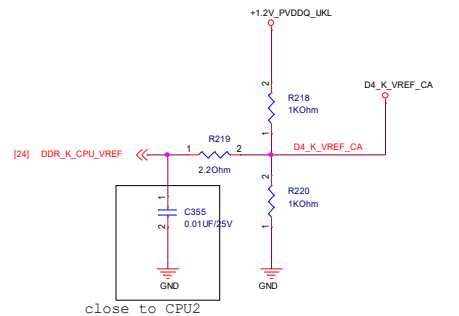


**BOM:Change 12G02411288EAK to 12G02410288XAK**



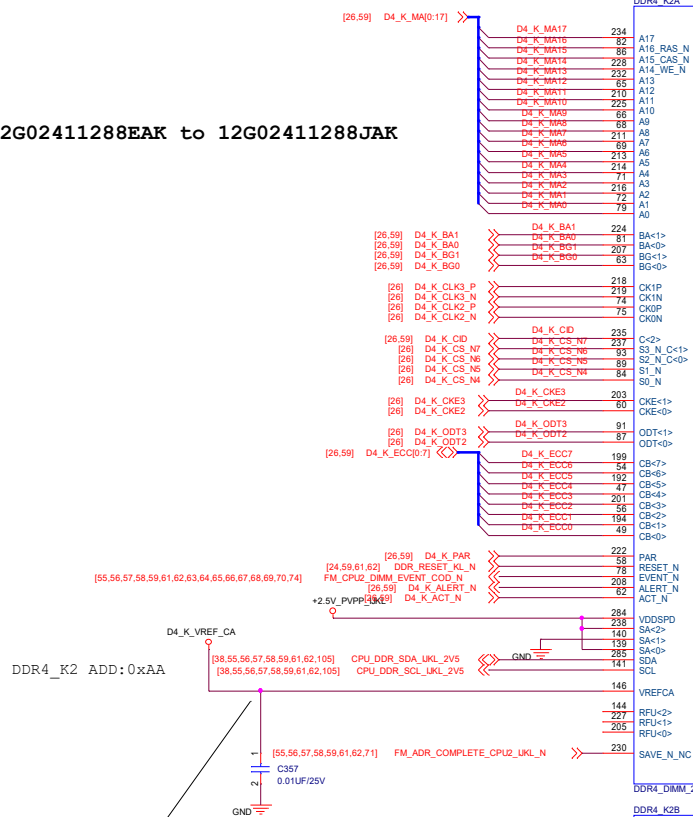
```
DDR4_M2 ADD:0xA2
DDR4_M1 ADD:0xA0
DDR4_N2 ADD:0xA6
DDR4_N1 ADD:0xA4
DDR4_O2 ADD:0xAA
DDR4_O1 ADD:0xA8
DDR4_P2 ADD:0xAA
DDR4_P1 ADD:0xA8
```

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

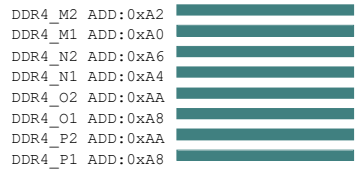
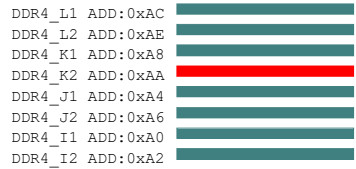


Size C	Document Number 059.CPU2_DDR4_CH_K1	Rev R1.00
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BOM:Change 12G02411288EAK to 12G02411288JAK

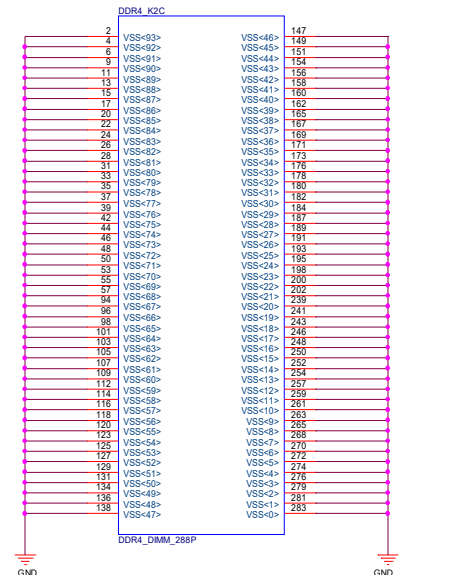
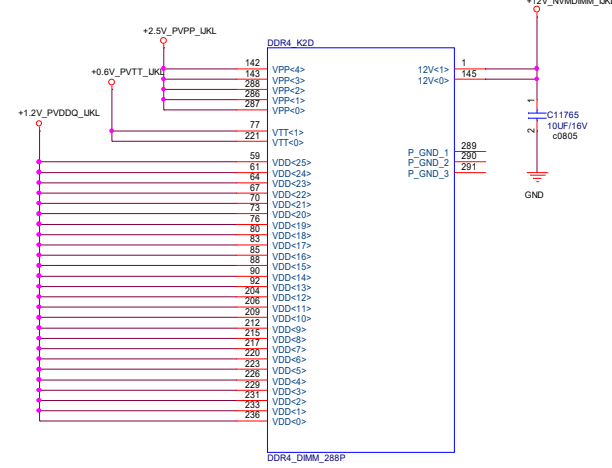
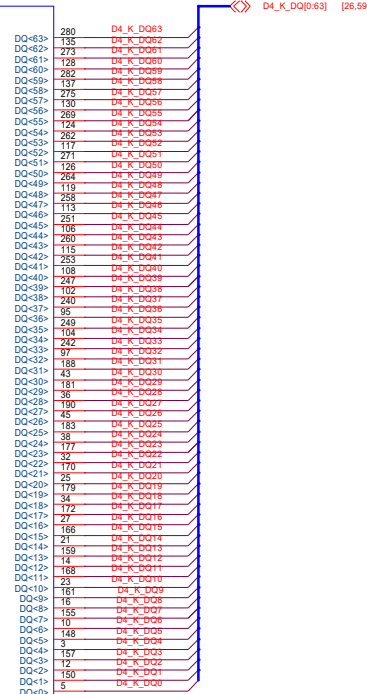


trace width 10mil, spacing 20mil

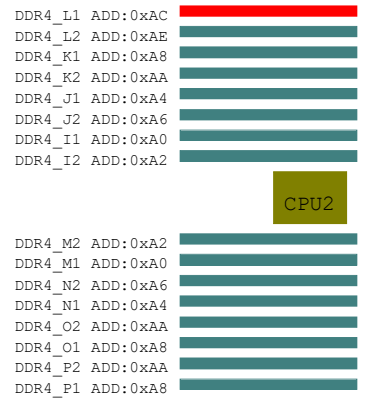


## DIMM Socket SPD Address Configurations

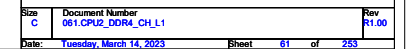
Channel	2TMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



**BOM:Change 12G02411288EAK to 12G02410288XAK**

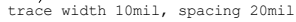


Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E





BOM:Change 12G02411288EAK to 12G02411288JAK

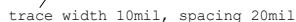
CPU2

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

DPC621-BV			
Size C	Document Number 062.CUP2_DDR4_CH_L2	Rev R1.00	
Date: Tuesday, March 14, 2023	Sheet 62	of 253	



**BOM:Change 12G02411288EAK to 12G02410288XAK**



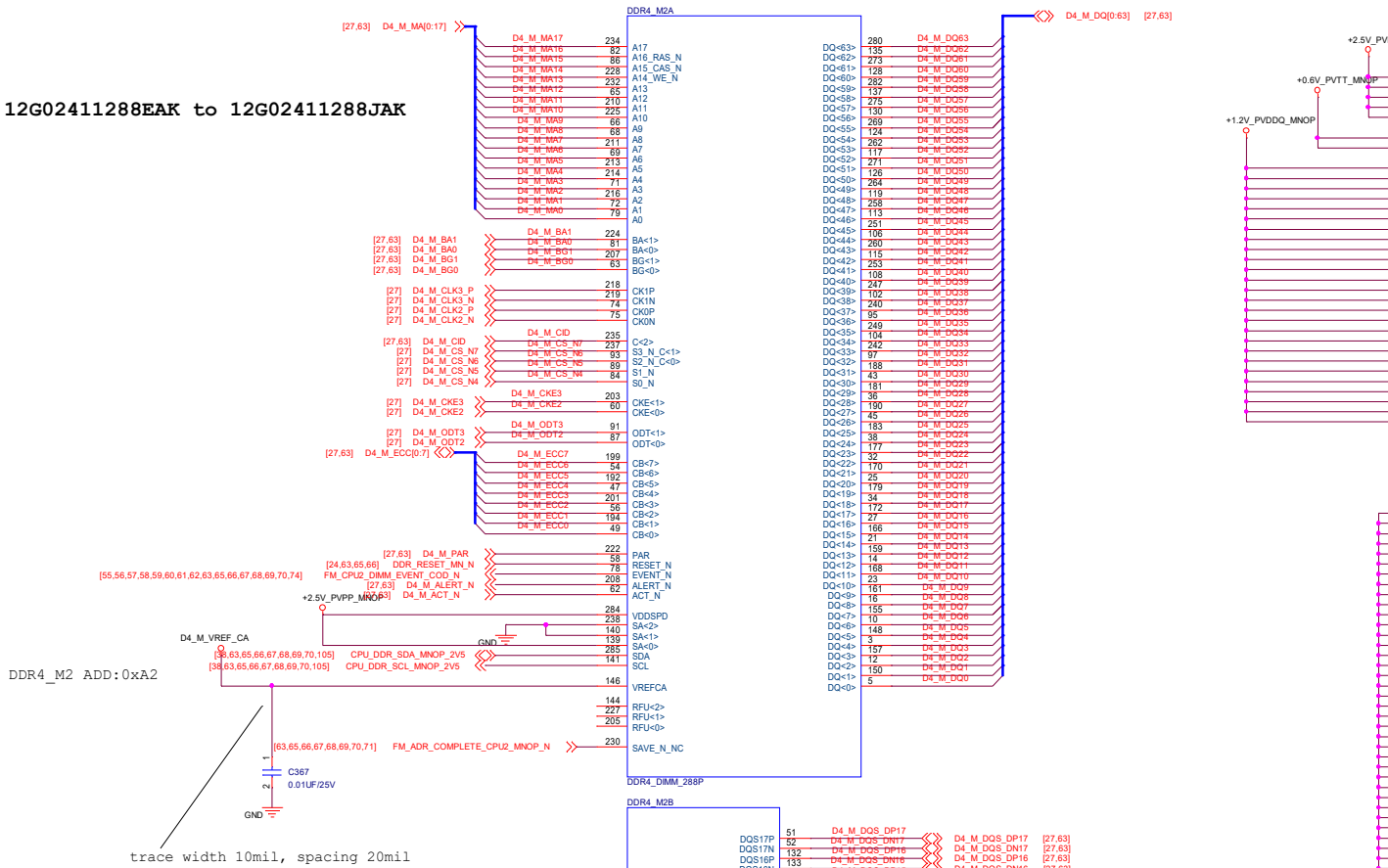
```
DDR4_M2 ADD:0xA2
DDR4_M1 ADD:0xA0
DDR4_N2 ADD:0xA6
DDR4_N1 ADD:0xA4
DDR4_O2 ADD:0xAA
DDR4_O1 ADD:0xA8
DDR4_P2 ADD:0xAA
DDR4_P1 ADD:0xA8
```

Channel	DIMM Slot	SA [2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



Size	Document Number	Rev
C	063.CPU2_DDR4_CH_M1	R1
Date:	Tuesday, March 14, 2023	Sheet 63 of 253

R1.01  
BOM:Change 12G02411288EAK to 12G02411288JAK



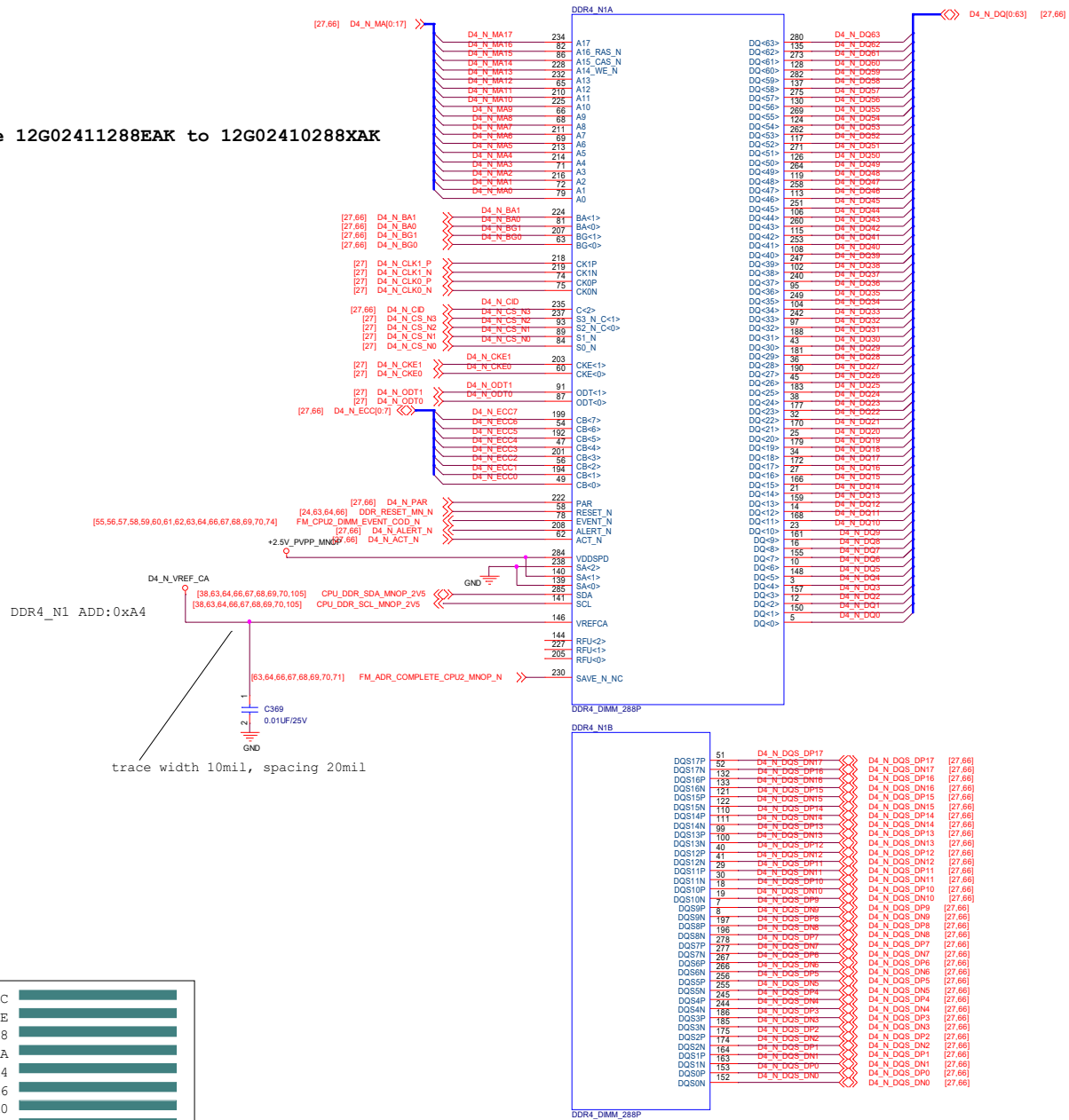
DDR4_L1	ADD:0xA6
DDR4_L2	ADD:0xA6
DDR4_K1	ADD:0xA8
DDR4_K2	ADD:0xA8
DDR4_J1	ADD:0xA4
DDR4_J2	ADD:0xA6
DDR4_I1	ADD:0xA0
DDR4_I2	ADD:0xA2

CPU2

DDR4_M2	ADD:0xA2
DDR4_M1	ADD:0xA0
DDR4_N2	ADD:0xA6
DDR4_N1	ADD:0xA4
DDR4_O2	ADD:0xA8
DDR4_O1	ADD:0xA8
DDR4_P2	ADD:0xA8
DDR4_P1	ADD:0xA8

DIMM Socket SPD Address Configurations					
Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD	
A/E or 0/4	DIMM0	000	A0	30	
	DIMM1	001	A2	32	
	DIMM0	010	A4	34	
B/F or 1/5	DIMM1	011	A6	36	
	DIMM0	100	A8	38	
	DIMM1	101	AA	3A	
C/G or 2/6	DIMM0	110	AC	3C	
	DIMM1	111	AE	3E	
D/H or 3/7	DIMM0	111	AE	3E	
	DIMM1	111	AE	3E	
	DIMM1	111	AE	3E	

**BOM:Change 12G02411288EAK to 12G02410288XAK**



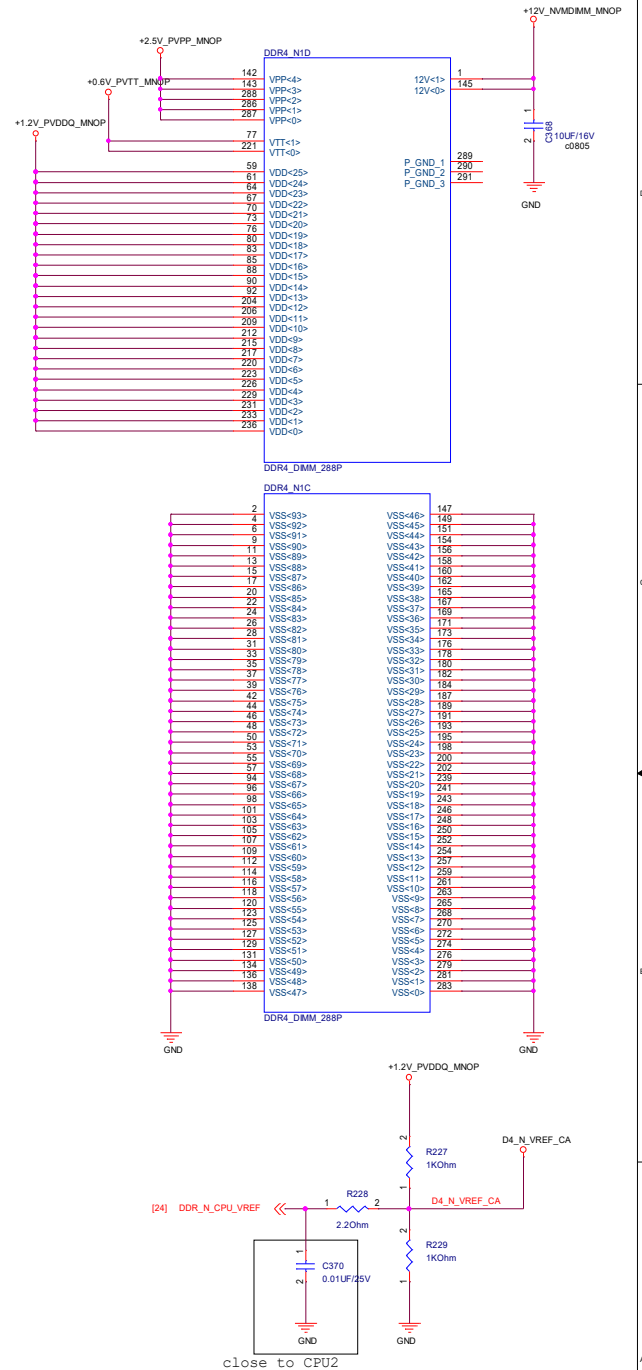
DDR4_L1	ADD: 0xA0	
DDR4_L2	ADD: 0xA0	
DDR4_K1	ADD: 0xA0	
DDR4_K2	ADD: 0xA0	
DDR4_J1	ADD: 0xA0	
DDR4_J2	ADD: 0xA0	
DDR4_I1	ADD: 0xA0	
DDR4_I2	ADD: 0xA0	

CPU2

DDR4_M2	ADD: 0xA2	
DDR4_M1	ADD: 0xA0	
DDR4_N2	ADD: 0xA6	
DDR4_N1	ADD: 0xA4	
DDR4_O2	ADD: 0xAA	
DDR4_O1	ADD: 0xA8	
DDR4_P2	ADD: 0xA4	
DDR4_P1	ADD: 0xA8	

### DIMM Socket SPD Address Configurations

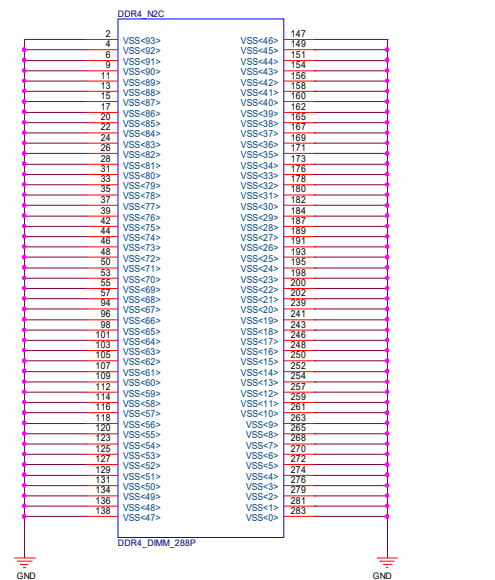
Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



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Size	Document Number	Rev
C	065.CPU2_DDR4_CH_N1	R1.00
Date:	Tuesday, March 14, 2023	Sheet 65 of 253

**BOM:Change 12G02411288EAK to 12G02411288JAK**



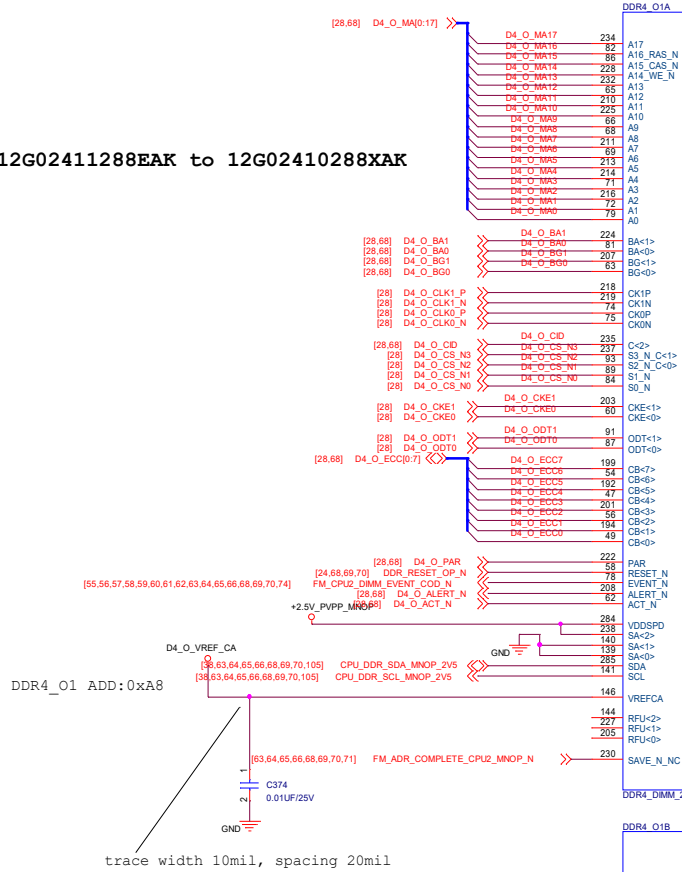
CPU2

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

DDR4_M2	ADD: 0xA2	
DDR4_M1	ADD: 0xA0	
DDR4_N2	ADD: 0xA6	
DDR4_N1	ADD: 0xA4	
DDR4_O2	ADD: 0xAA	
DDR4_O1	ADD: 0xA8	
DDR4_P2	ADD: 0xA4	
DDR4_P1	ADD: 0xA8	

R1.01

BOM:Change 12G02411288EAK to 12G02410288XAK



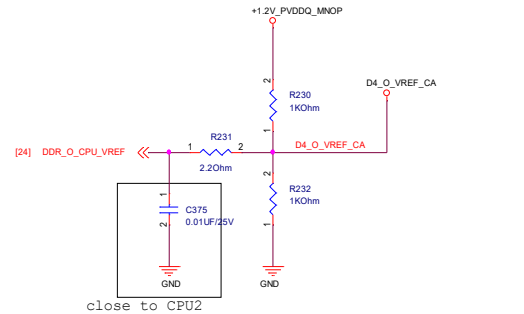
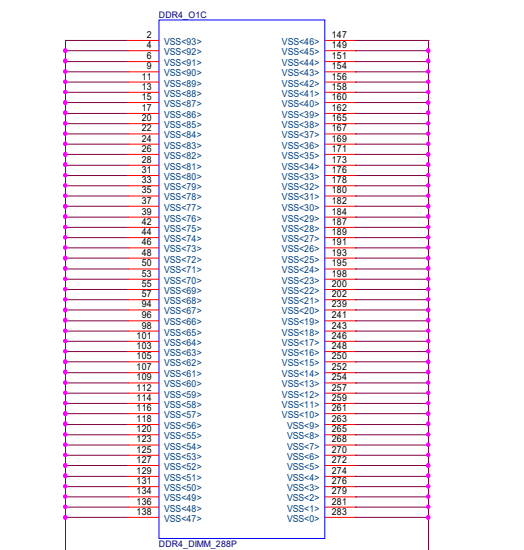
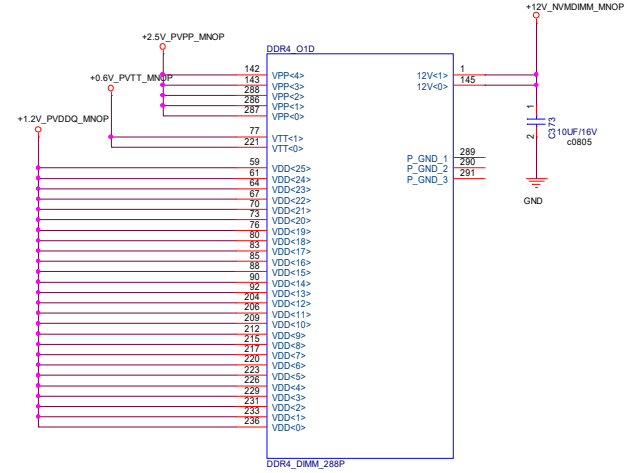
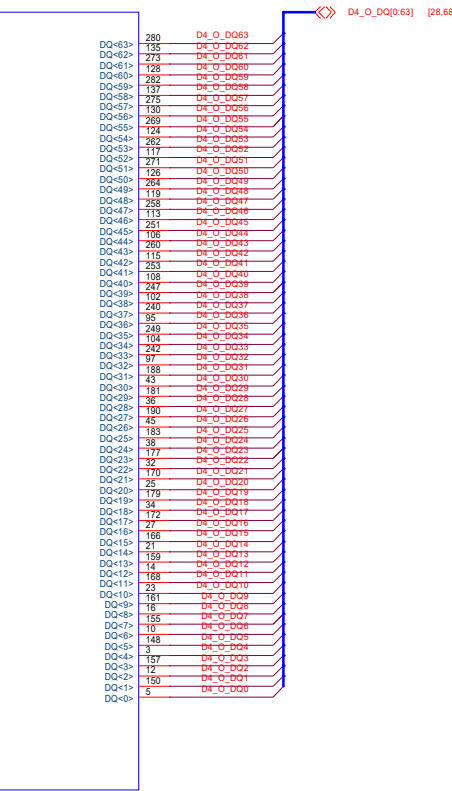
DDR4\_L1 ADD:0xA0  
DDR4\_L2 ADD:0xA0  
DDR4\_K1 ADD:0xA8  
DDR4\_K2 ADD:0xA8  
DDR4\_J1 ADD:0xA4  
DDR4\_J2 ADD:0xA6  
DDR4\_I1 ADD:0xA0  
DDR4\_I2 ADD:0xA2

CPU2

DDR4\_M2 ADD:0xA2  
DDR4\_M1 ADD:0xA0  
DDR4\_N2 ADD:0xA6  
DDR4\_N1 ADD:0xA4  
DDR4\_O2 ADD:0xAA  
DDR4\_O1 ADD:0xA8  
DDR4\_P2 ADD:0xAA  
DDR4\_P1 ADD:0xA8

DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
	DIMM0	010	A4	34
B/F or 1/5	DIMM1	011	A6	36
	DIMM0	100	A8	38
C/G or 2/6	DIMM1	101	AA	3A
	DIMM0	110	AC	3C
D/H or 3/7	DIMM1	111	AE	3E



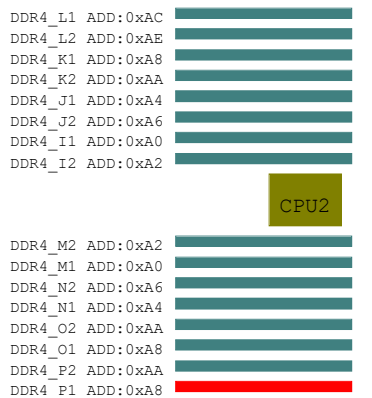
PCB231-3V





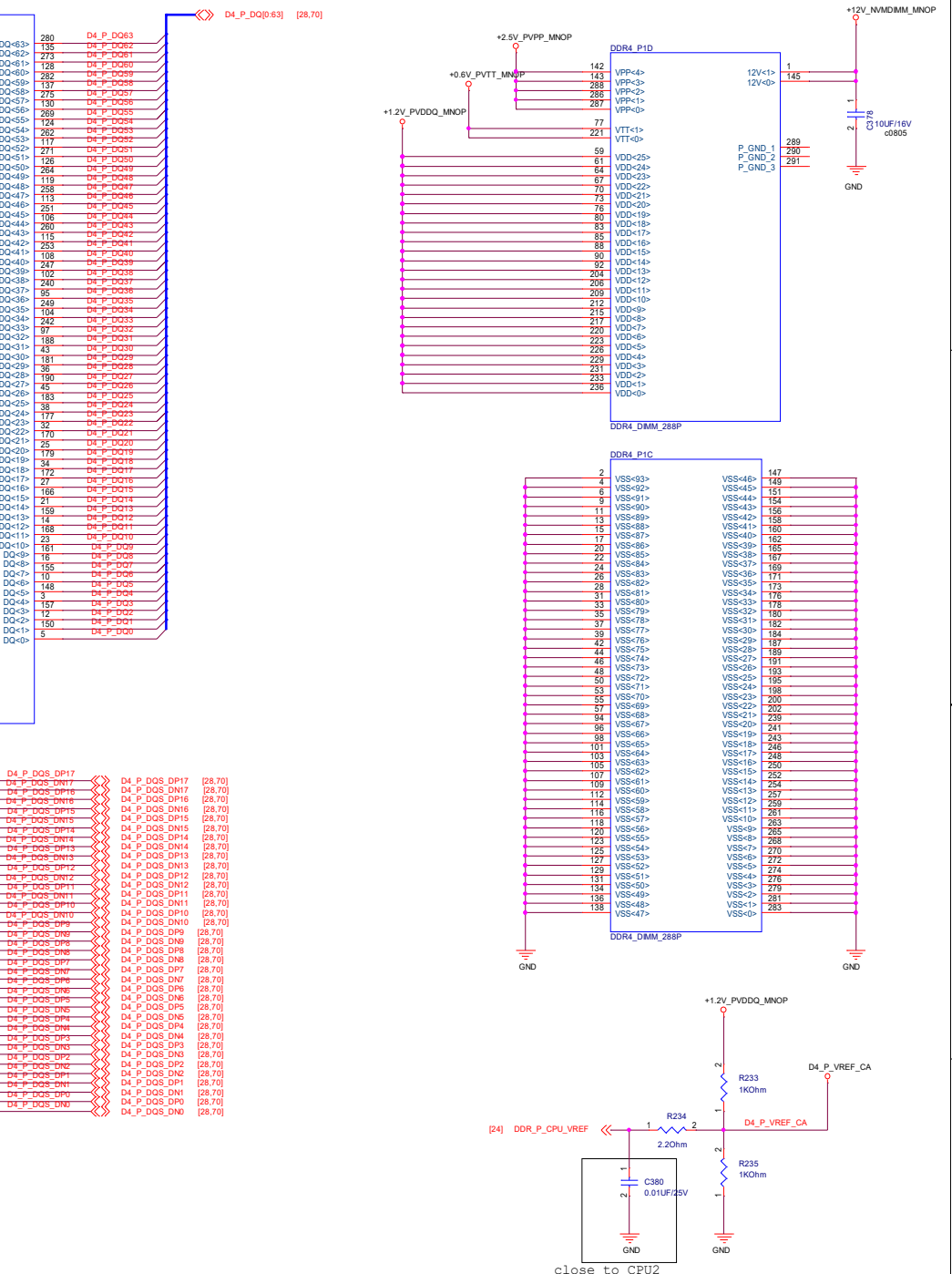


**BOM:Change 12G02411288EAK to 12G02410288XAK**



### DIMM Socket SPD Address Configurations

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E



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Size	Document Number	Rev
C	069.CPU2_DDR4_CH_P1	R1.00
Date:	Tuesday, March 14, 2023	Sheet 60 of 253

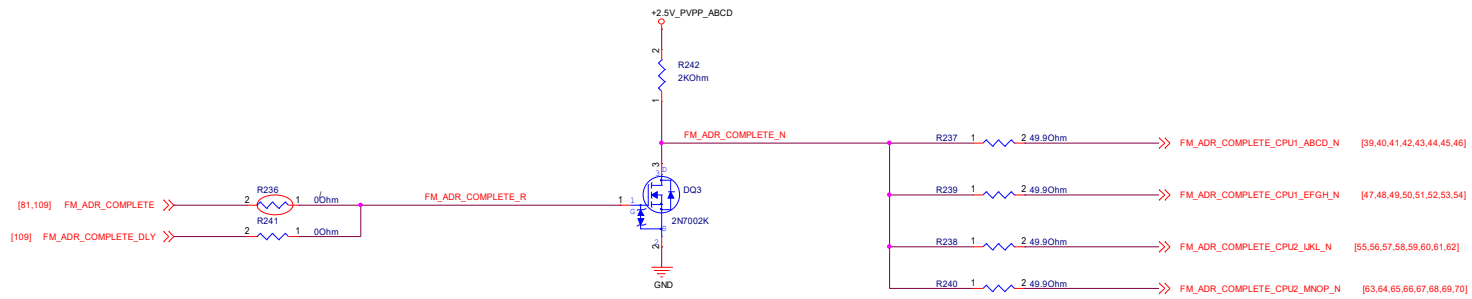
BOM:Change 12G02411288EAK to 12G02411288JAK

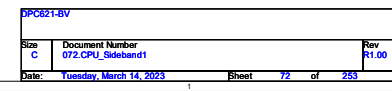


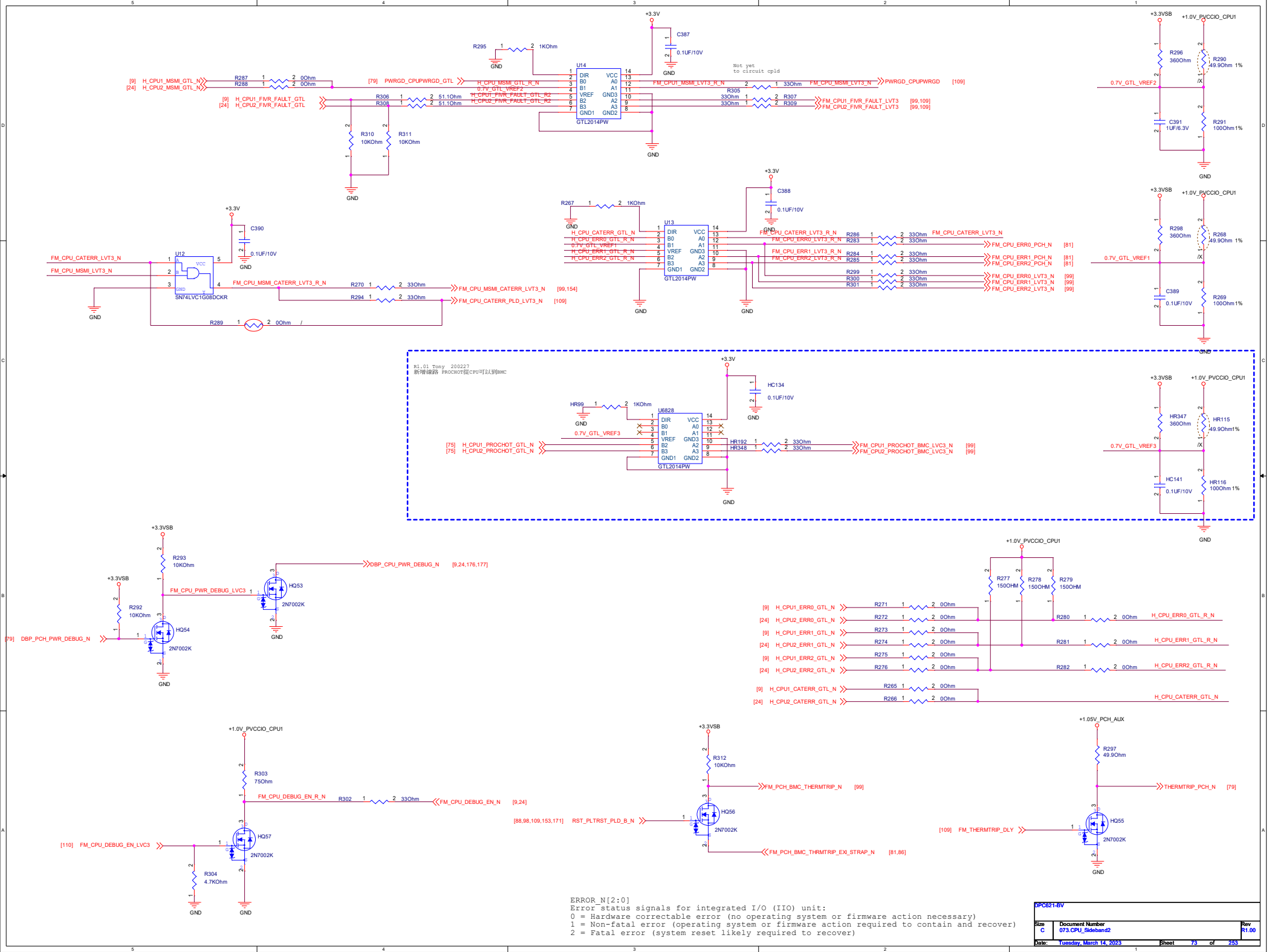
DDR4_M2	ADD: 0xA2	
DDR4_M1	ADD: 0xA0	
DDR4_N2	ADD: 0xA6	
DDR4_N1	ADD: 0xA4	
DDR4_O2	ADD: 0xAA	
DDR4_O1	ADD: 0xA8	
DDR4_P2	ADD: 0xA4	
DDR4_P1	ADD: 0xA8	

Channel	DIMM Slot	SA[2:0]	SPD Address	TSOD
A/E or 0/4	DIMM0	000	A0	30
	DIMM1	001	A2	32
B/F or 1/5	DIMM0	010	A4	34
	DIMM1	011	A6	36
C/G or 2/6	DIMM0	100	A8	38
	DIMM1	101	AA	3A
D/H or 3/7	DIMM0	110	AC	3C
	DIMM1	111	AE	3E

Size C	Document Number 070.CPU2_DDR4_CH_P2	Rev R1.00
Date: Tuesday, March 14, 2023	Sheet 70 of 253	

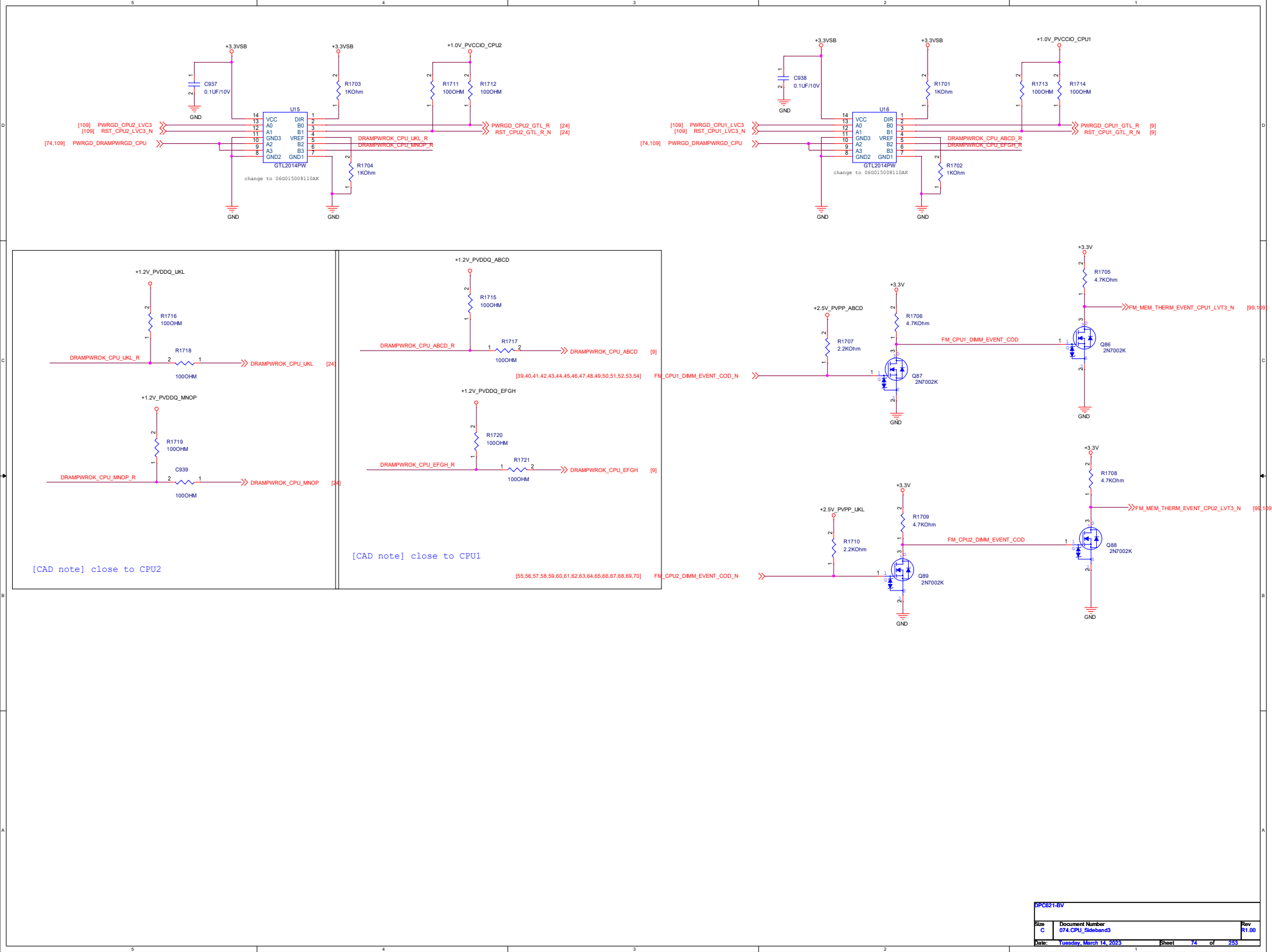




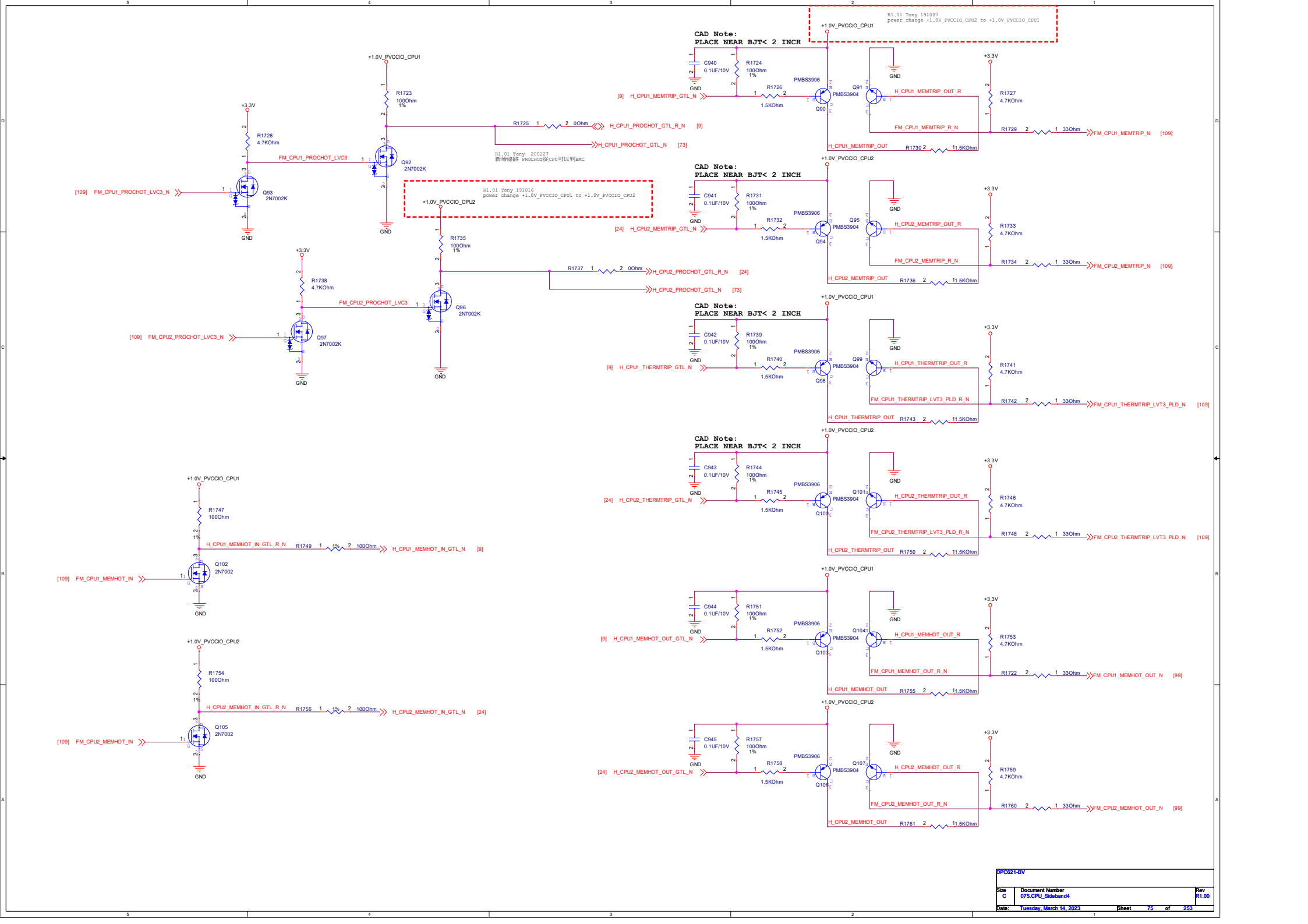


JP0821-BV

Size	Document Number	Rev
C	073.CPU_Sideband2	R1.00
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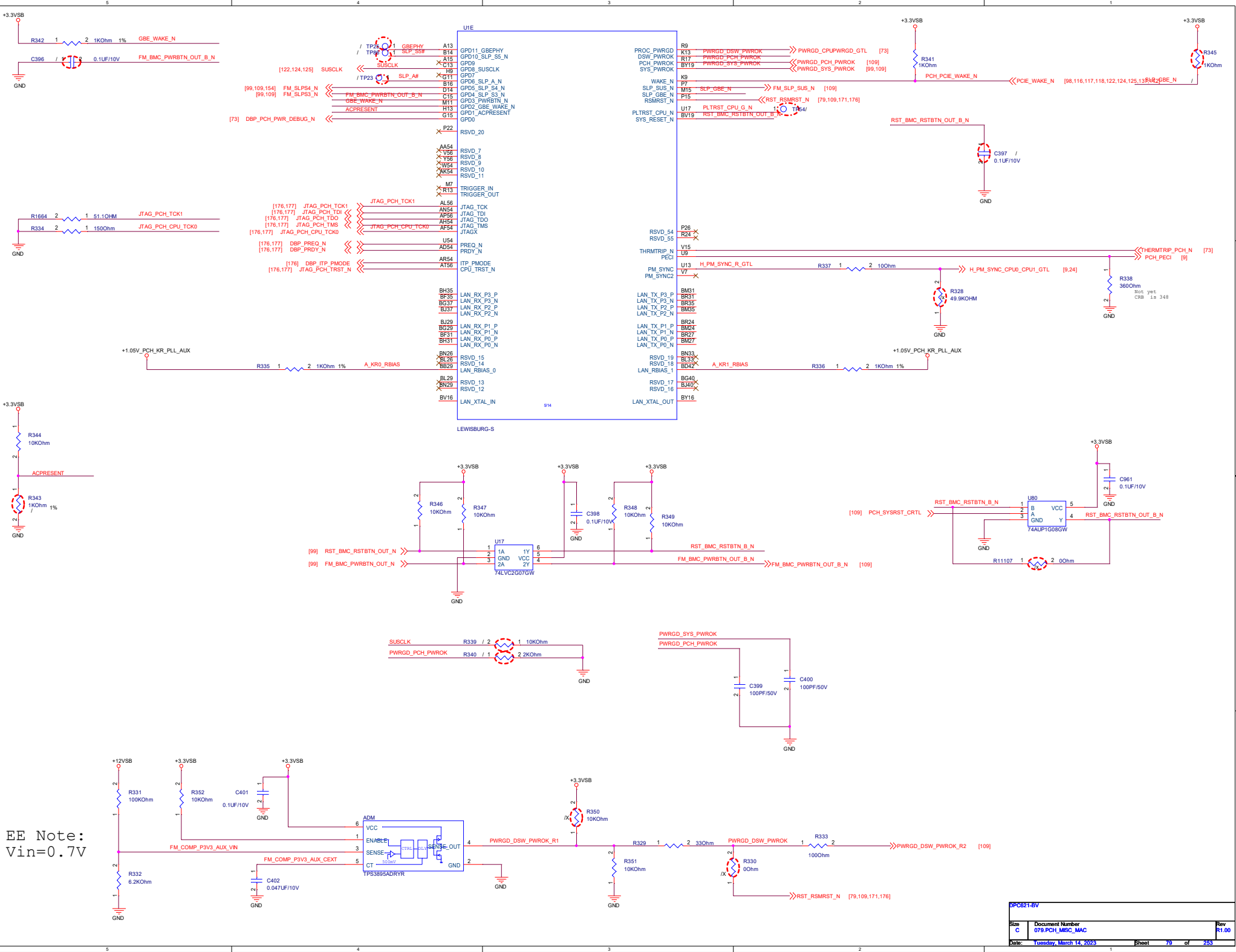


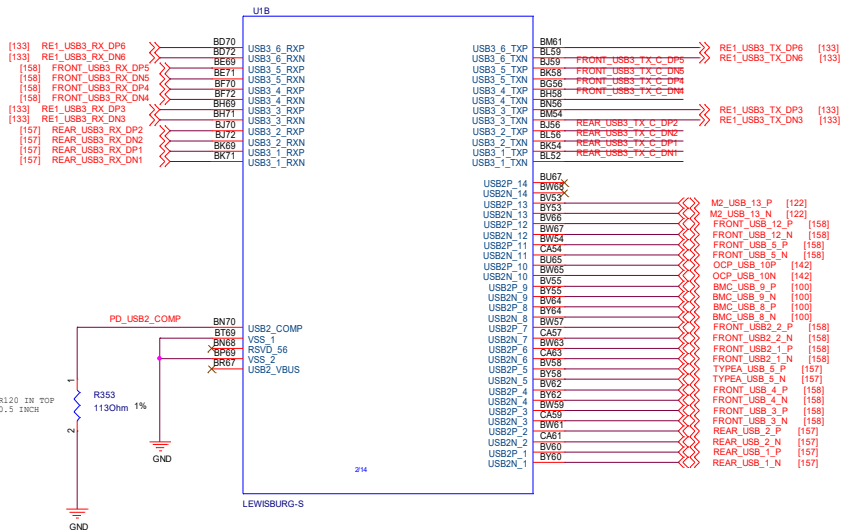
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==== PCH =====

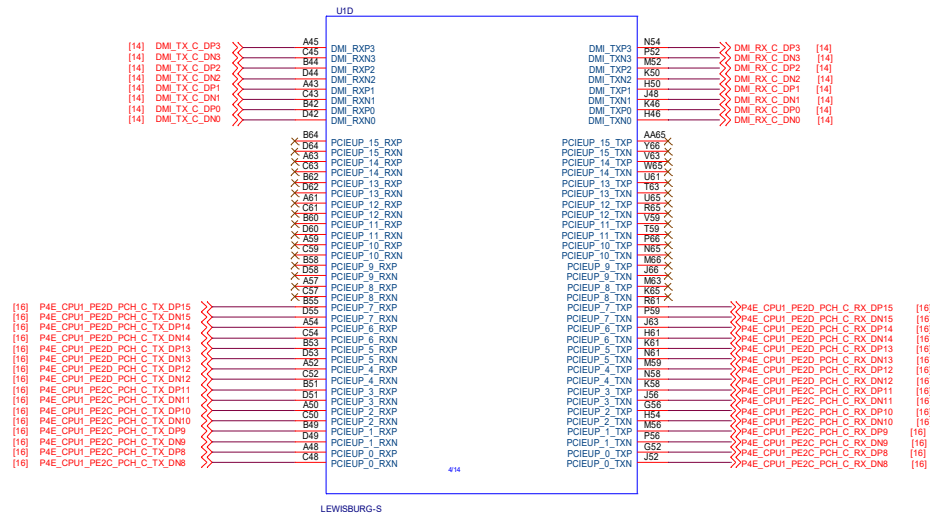
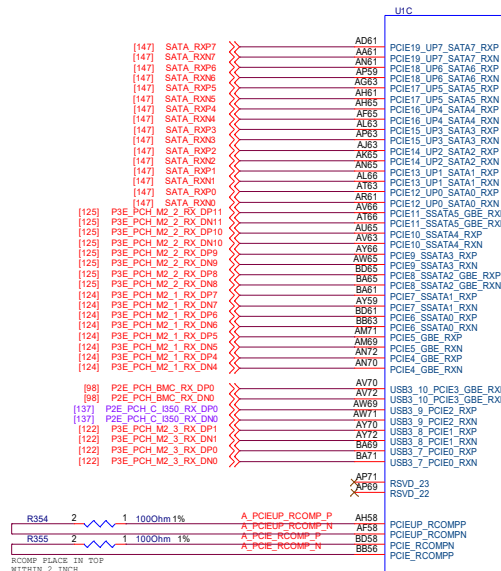


EE Note:  
Vin=0.7V



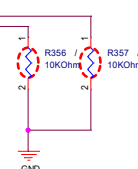


FRONT_USB3_TX_C_DP4	C405	1	2	0.1uF/16V	FRONT_USB3_TX_DP4	[158]
FRONT_USB3_TX_C_DN4	C406	1	2	0.1uF/16V	FRONT_USB3_TX_DN4	[158]
REAR_USB3_TX_C_DP2	C409	1	2	0.1uF/16V	REAR_USB3_TX_DP2	[157]
REAR_USB3_TX_C_DN2	C410	1	2	0.1uF/16V	REAR_USB3_TX_DN2	[157]
REAR_USB3_TX_C_DP1	C411	1	2	0.1uF/16V	REAR_USB3_TX_DP1	[157]
REAR_USB3_TX_C_DN1	C412	1	2	0.1uF/16V	REAR_USB3_TX_DN1	[157]
FRONT_USB3_TX_C_DP5	C13105	1	2	0.1uF/16V	FRONT_USB3_TX_DP5	[158]
FRONT_USB3_TX_C_DN5	C13104	1	2	0.1uF/16V	FRONT_USB3_TX_DN5	[158]



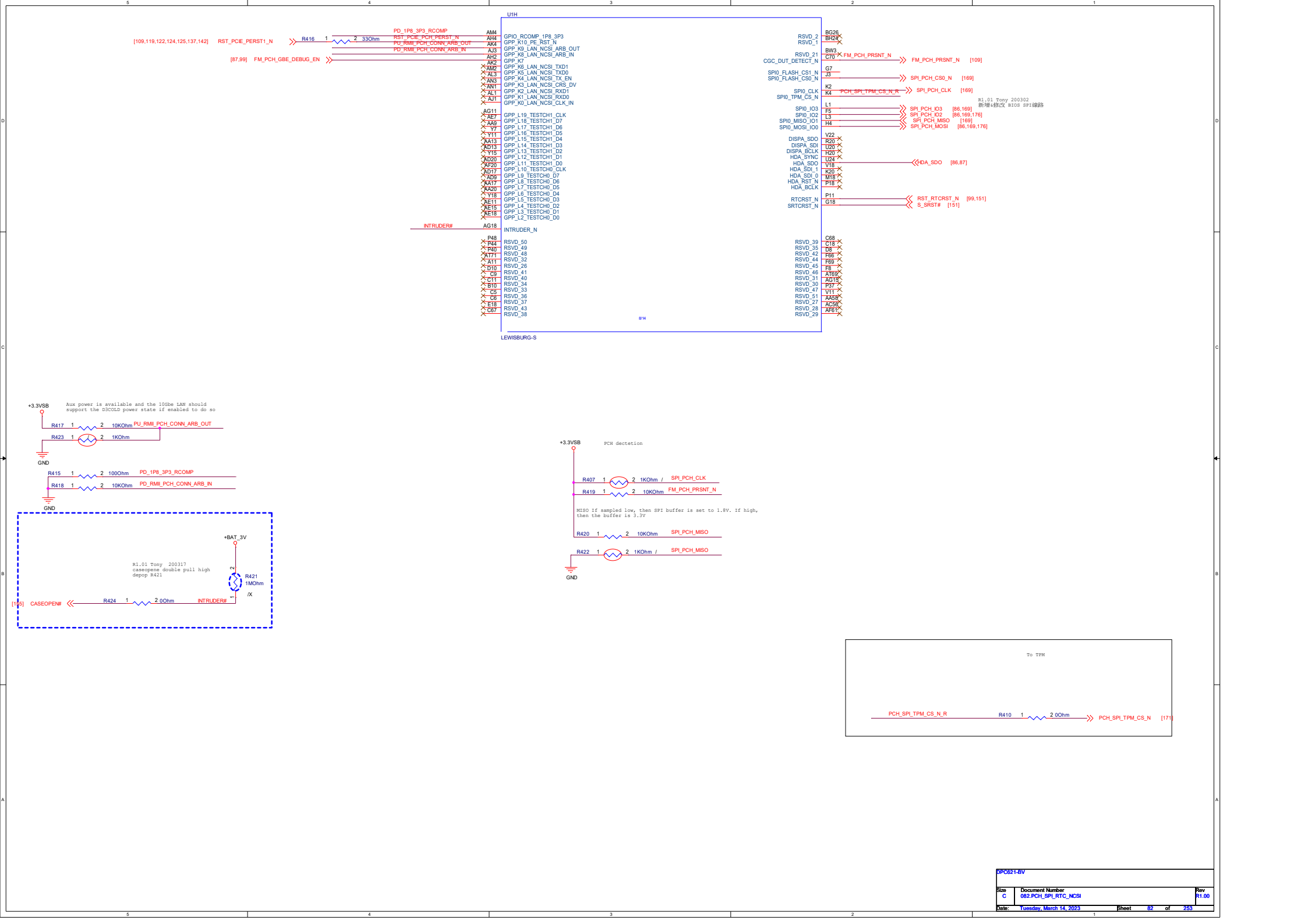
PCIE19_UP7_SATA7_RXP	L72	1	2	0.1uF/16V	PCIE19_UP7_SATA7_RXP	[147]
PCIE19_UP7_SATA7_RXN	L73	1	2	0.1uF/16V	PCIE19_UP7_SATA7_RXN	[147]
PCIE18_UP6_SATA6_RXP	M71	1	2	0.1uF/16V	PCIE18_UP6_SATA6_RXP	[147]
PCIE18_UP6_SATA6_RXN	M72	1	2	0.1uF/16V	PCIE18_UP6_SATA6_RXN	[147]
PCIE17_UP5_SATA5_RXP	N70	1	2	0.1uF/16V	PCIE17_UP5_SATA5_RXP	[147]
PCIE17_UP5_SATA5_RXN	P71	1	2	0.1uF/16V	PCIE17_UP5_SATA5_RXN	[147]
PCIE16_UP4_SATA4_RXP	R72	1	2	0.1uF/16V	PCIE16_UP4_SATA4_RXP	[147]
PCIE16_UP4_SATA4_RXN	R73	1	2	0.1uF/16V	PCIE16_UP4_SATA4_RXN	[147]
PCIE15_UP3_SATA3_RXP	T71	1	2	0.1uF/16V	PCIE15_UP3_SATA3_RXP	[147]
PCIE15_UP3_SATA3_RXN	T72	1	2	0.1uF/16V	PCIE15_UP3_SATA3_RXN	[147]
PCIE14_UP2_SATA2_RXP	V70	1	2	0.1uF/16V	PCIE14_UP2_SATA2_RXP	[147]
PCIE14_UP2_SATA2_RXN	V71	1	2	0.1uF/16V	PCIE14_UP2_SATA2_RXN	[147]
PCIE13_UP1_SATA1_RXP	W70	1	2	0.1uF/16V	PCIE13_UP1_SATA1_RXP	[147]
PCIE13_UP1_SATA1_RXN	W71	1	2	0.1uF/16V	PCIE13_UP1_SATA1_RXN	[147]
PCIE12_UP0_SATA0_RXP	X70	1	2	0.1uF/16V	PCIE12_UP0_SATA0_RXP	[147]
PCIE12_UP0_SATA0_RXN	X71	1	2	0.1uF/16V	PCIE12_UP0_SATA0_RXN	[147]
PCIE11_SSATA5_GBE_RXP	AC71	1	2	0.1uF/16V	PCIE11_SSATA5_GBE_RXP	[147]
PCIE11_SSATA5_GBE_RXN	AC72	1	2	0.1uF/16V	PCIE11_SSATA5_GBE_RXN	[147]
PCIE10_SSATA4_RXP	AD70	1	2	0.1uF/16V	PCIE10_SSATA4_RXP	[147]
PCIE10_SSATA4_RXN	AD71	1	2	0.1uF/16V	PCIE10_SSATA4_RXN	[147]
PCIE9_SSATA3_RXP	AE71	1	2	0.1uF/16V	PCIE9_SSATA3_RXP	[147]
PCIE9_SSATA3_RXN	AE72	1	2	0.1uF/16V	PCIE9_SSATA3_RXN	[147]
PCIE8_SSATA2_GBE_RXP	AF70	1	2	0.1uF/16V	PCIE8_SSATA2_GBE_RXP	[147]
PCIE8_SSATA2_GBE_RXN	AF71	1	2	0.1uF/16V	PCIE8_SSATA2_GBE_RXN	[147]
PCIE7_SSATA1_RXP	AH69	1	2	0.1uF/16V	PCIE7_SSATA1_RXP	[147]
PCIE7_SSATA1_RXN	AJ72	1	2	0.1uF/16V	PCIE7_SSATA1_RXN	[147]
PCIE6_SSATA0_RXP	B363	1	2	0.1uF/16V	PCIE6_SSATA0_RXP	[147]
PCIE6_SSATA0_RXN	BH65	1	2	0.1uF/16V	PCIE6_SSATA0_RXN	[147]
PCIE5_GBE_RXP	BM65	1	2	0.1uF/16V	PCIE5_GBE_RXP	[147]
PCIE5_GBE_RXN	BM66	1	2	0.1uF/16V	PCIE5_GBE_RXN	[147]
PCIE4_GBE_RXP	CG66	1	2	0.1uF/16V	PCIE4_GBE_RXP	[147]
PCIE4_GBE_RXN	CG67	1	2	0.1uF/16V	PCIE4_GBE_RXN	[147]
USB3_10_PCIE3_GBE_RXP	BK61	1	2	0.1uF/16V	USB3_10_PCIE3_GBE_RXP	[147]
USB3_10_PCIE3_GBE_RXN	BH61	1	2	0.1uF/16V	USB3_10_PCIE3_GBE_RXN	[147]
USB3_9_PCIE2_RXP	BL66	1	2	0.1uF/16V	USB3_9_PCIE2_RXP	[147]
USB3_9_PCIE2_RXN	BM65	1	2	0.1uF/16V	USB3_9_PCIE2_RXN	[147]
USB3_8_PCIE1_RXP	BM65	1	2	0.1uF/16V	USB3_8_PCIE1_RXP	[147]
USB3_8_PCIE1_RXN	BM66	1	2	0.1uF/16V	USB3_8_PCIE1_RXN	[147]
USB3_7_PCIE0_RXP	CG66	1	2	0.1uF/16V	USB3_7_PCIE0_RXP	[147]
USB3_7_PCIE0_RXN	CG67	1	2	0.1uF/16V	USB3_7_PCIE0_RXN	[147]

EE NOTE :  
For M.2 Gen 3, PDG suggest to change from 0.1uF to 0.22uF



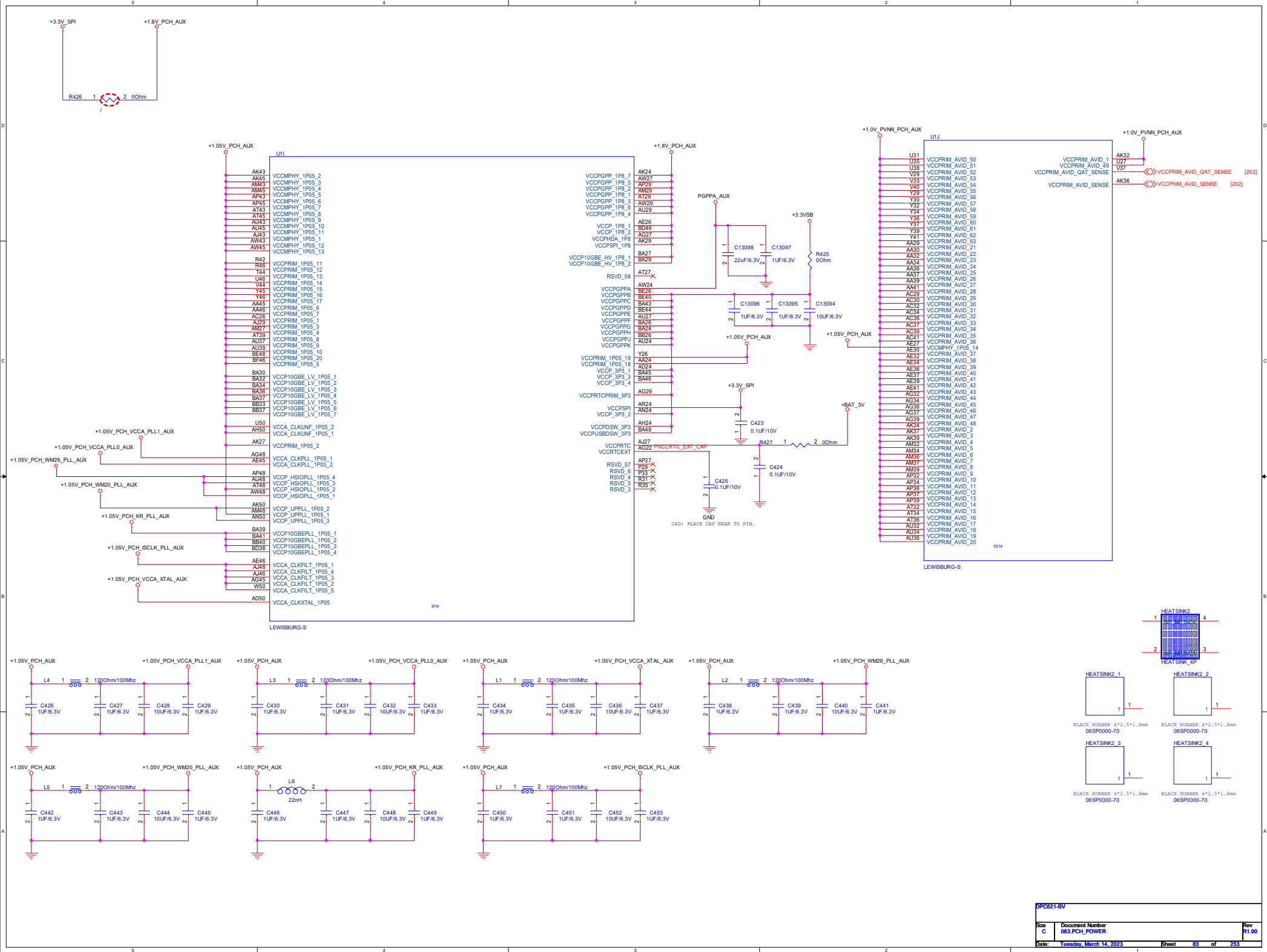




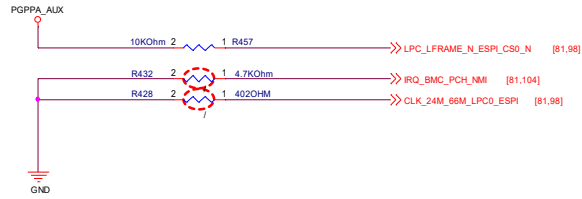
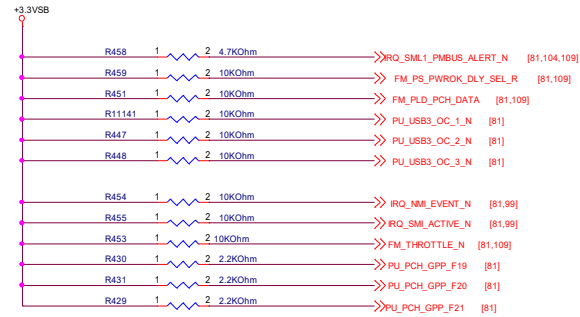
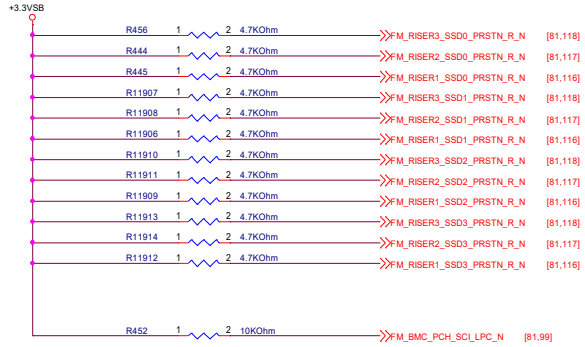
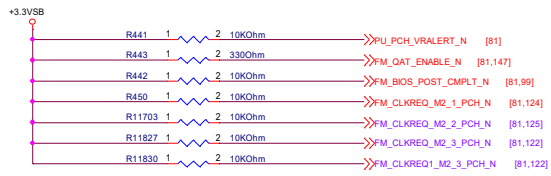


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Size	Document Number	Rev
C	082.PCH_SPI_RTC_NCSI	R1.00
Date:	Tuesday, March 14, 2023	Sheet 82 of 253

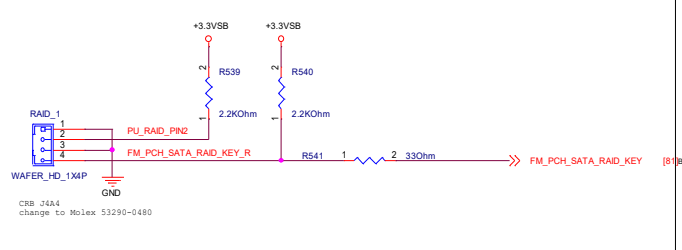
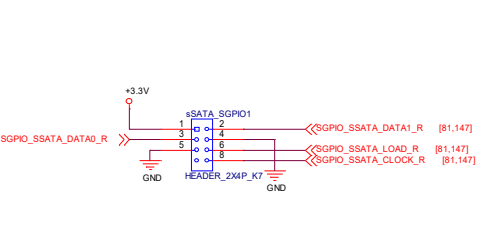
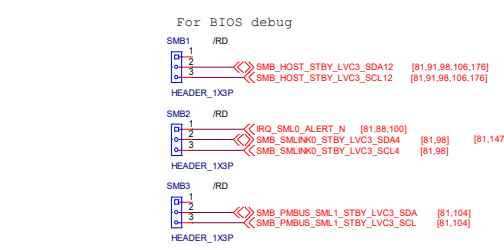
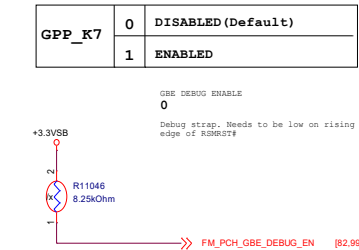
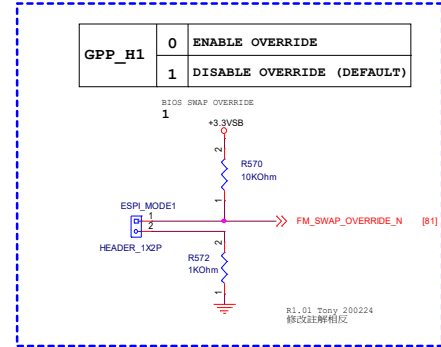
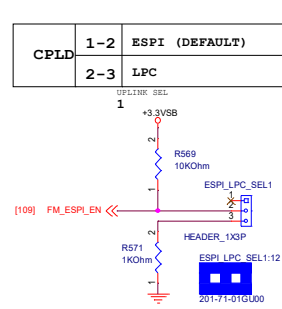
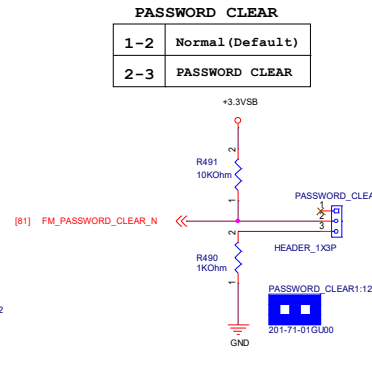
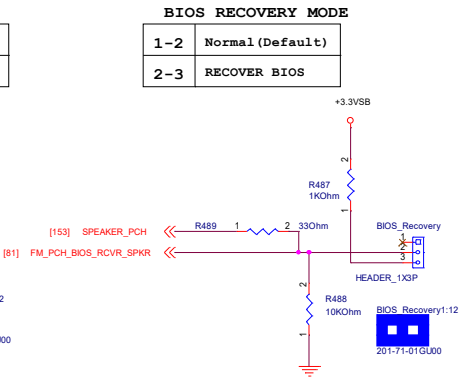
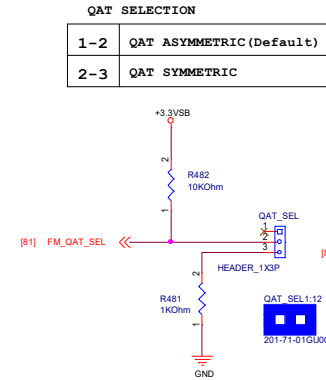
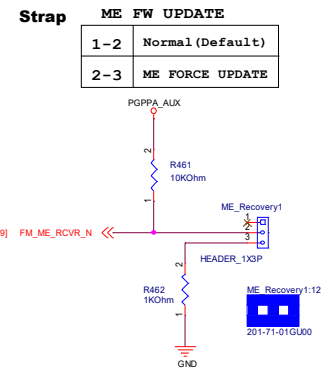
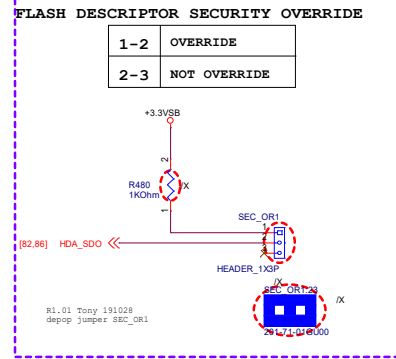
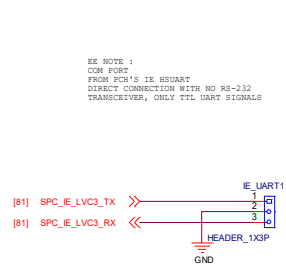
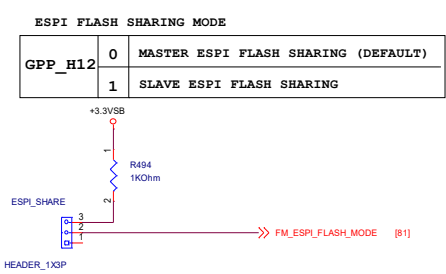
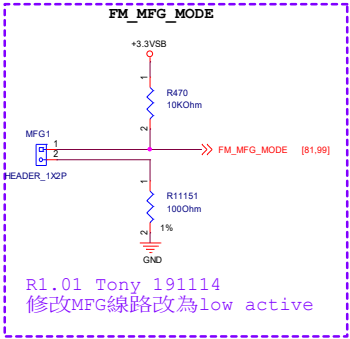


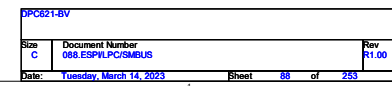




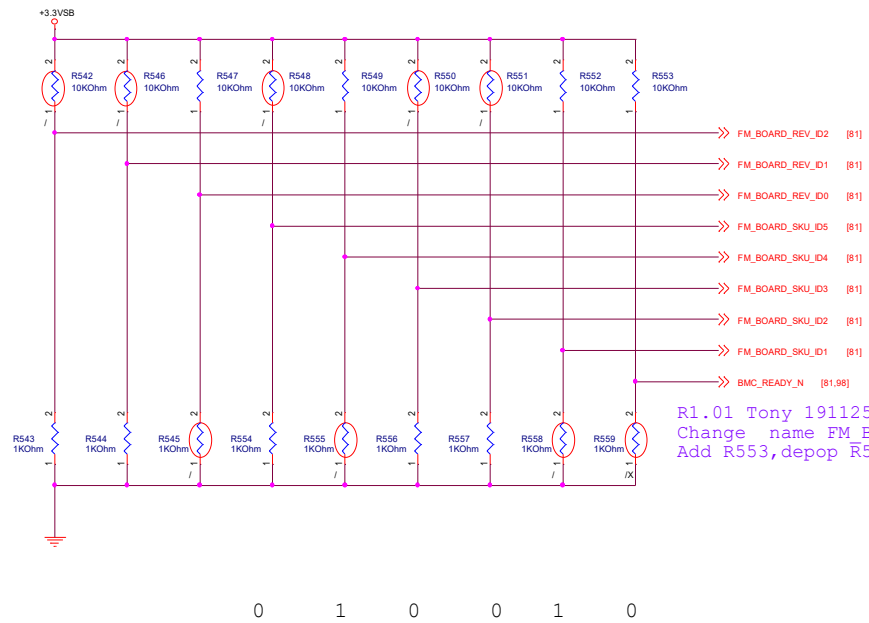




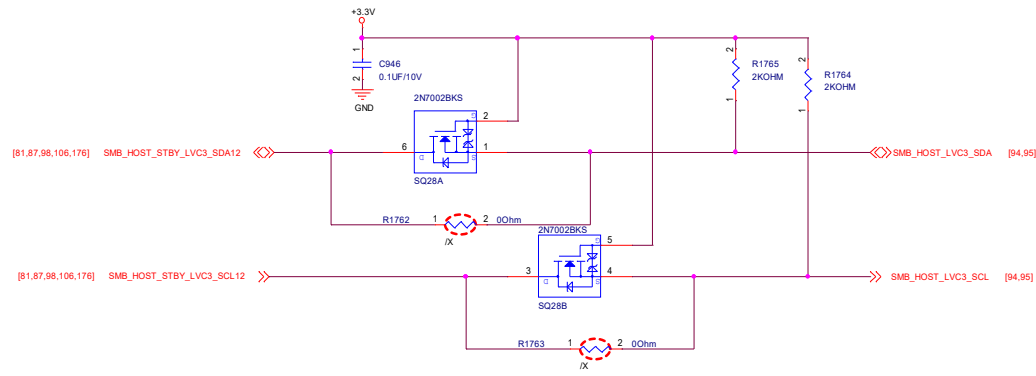








R1.01 Tony 191125  
 Change name FM\_BOARD\_SKU\_ID0 to BMC\_READY and connect to BMC  
 Add R553, depop R559



D

1

C

1

B

1

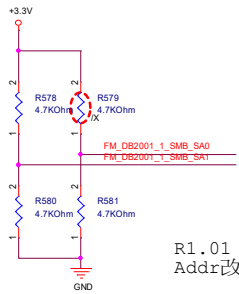
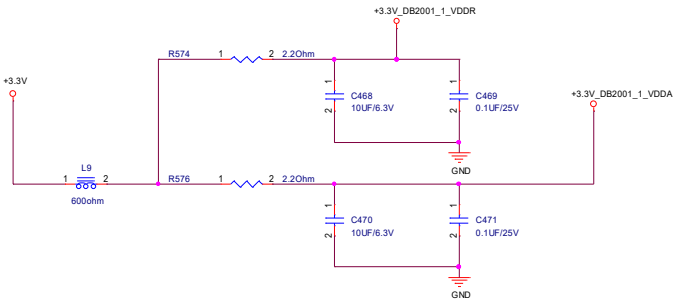
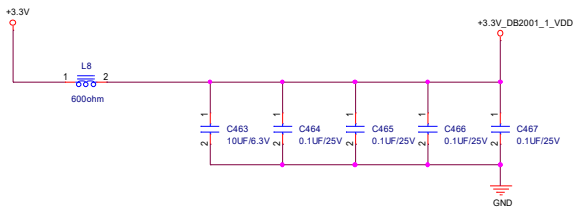
A

1

DPC821-BV			
Size C	Document Number 092 Blank		Rev R1.0
Date: Tuesday, March 14, 2023	Sheet	92 of	253

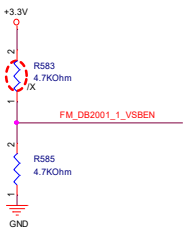


===CLK\_Buffer===

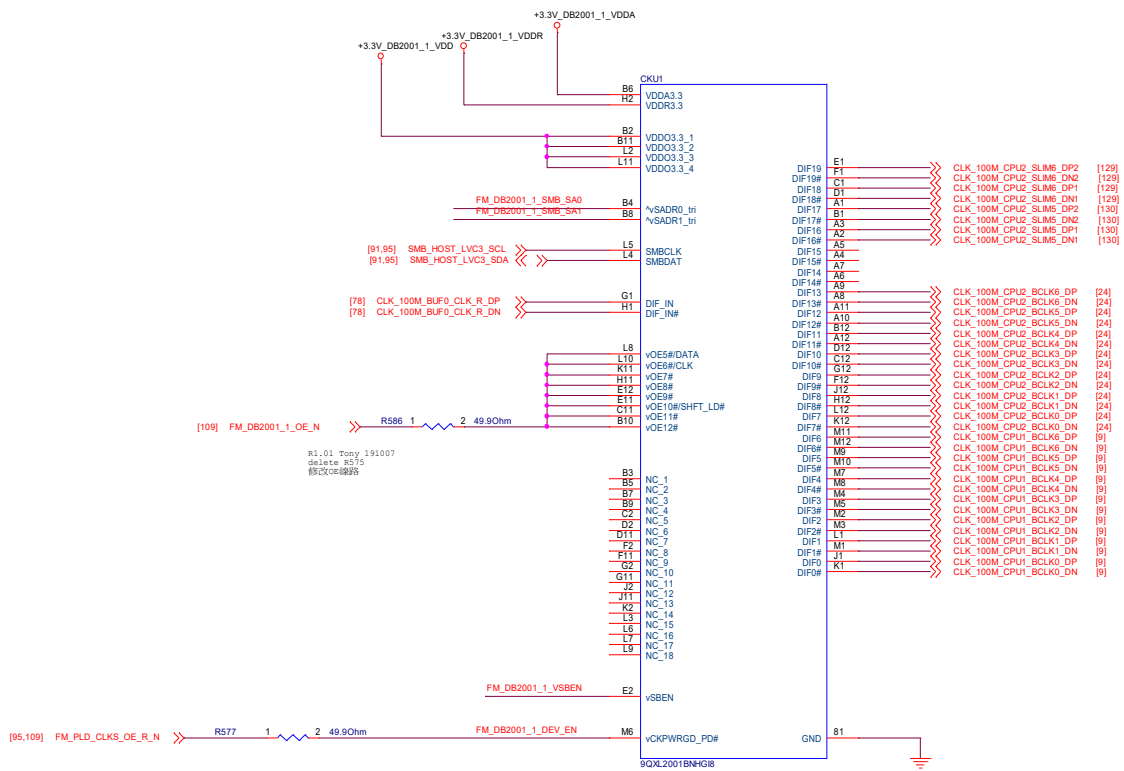


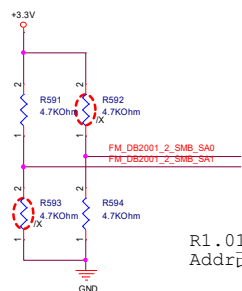
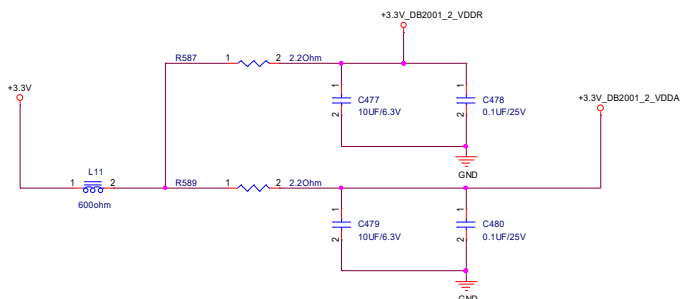
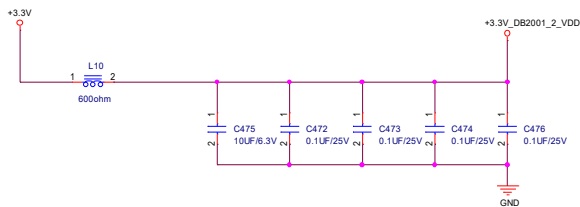
R1.01 Tony 191120  
Addr改為正確

**SMBUS ADDRESS: 0 X C2**



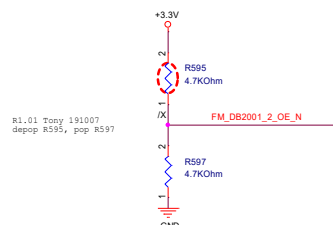
**VSбен MODE**  
**0: OE PINS AND SMBUS (DEFAULT)**  
**1:SIDE-BAND INTERFACE**



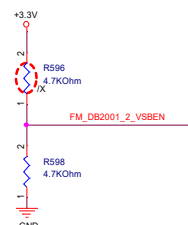


R1.01 Tony 191120  
Addr改為正確

SMBUS ADDRESS: 0 X CA



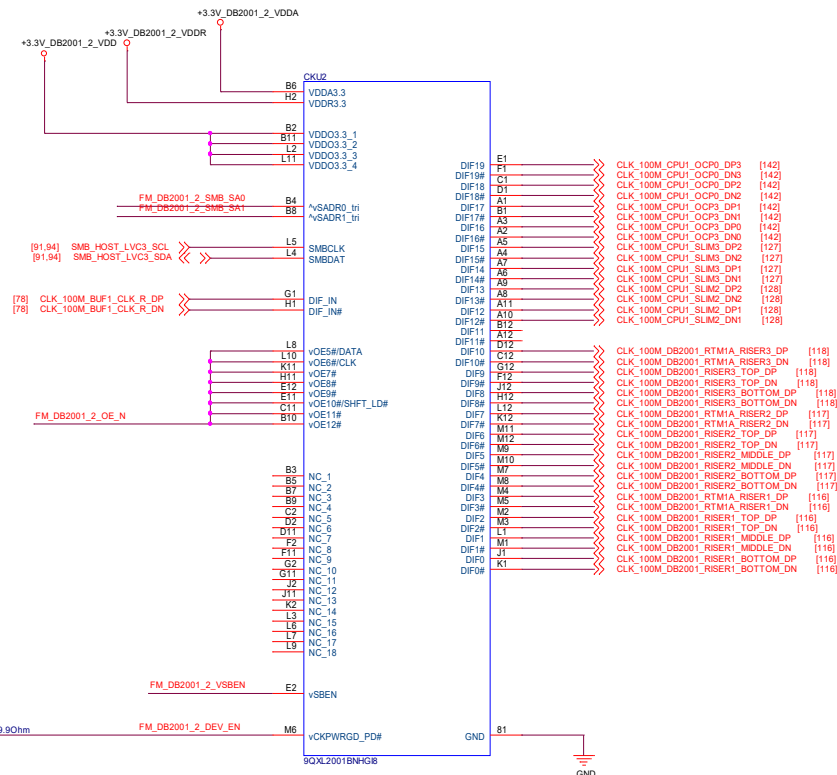
R1.01 Tony 191007  
depop R595, pop R597



```

VSBEN MODE
0: OE PINS AND SMBUS (DEFAULT)
1: SIDE-BAND INTERFACE

```



DF10	E1	CLK_100M_CPU1_OCPO, DP3	[142]
DF19F	A1	CLK_100M_CPU1_OCPO, DN3	[142]
DF18	A1	CLK_100M_CPU1_OCPO, DP2	[142]
DF19	A1	CLK_100M_CPU1_OCPO, DN2	[142]
DF17	A1	CLK_100M_CPU1_OCPO, DP1	[142]
DF17F	A3	CLK_100M_CPU1_OCPO, DN1	[142]
DF16F	A3	CLK_100M_CPU1_OCPO, DN0	[142]
DF16F	M5	CLK_100M_CPU1_SLMG, DN0	[127]
DF15	A4	CLK_100M_CPU1_SLMG, DP2	[127]
DF15F	A4	CLK_100M_CPU1_SLMG, DN2	[127]
DF14	A6	CLK_100M_CPU1_SLMG, DP1	[127]
DF14F	A8	CLK_100M_CPU1_SLMG, DN1	[127]
DF13	A8	CLK_100M_CPU1_SLMG, DN0	[127]
DF13F	A11	CLK_100M_CPU1_SLMG, DN2	[128]
DF12	B12	CLK_100M_CPU1_SLMG, DN1	[128]
DF12F	A10	CLK_100M_CPU1_SLMG, DN0	[128]
DF11	D12		
DF11F	D12		
DF10	D12	CLK_100M_DB2001_RTHMA, RSER, DP	[118]
DF10F	G12	CLK_100M_DB2001_RTHMA, RSER, DP	[118]
DF9	H12	CLK_100M_DB2001_RSER, TOP, DN	[118]
DF9F	J12	CLK_100M_DB2001_RSER, TOP, DP	[118]
DF8	H12	CLK_100M_DB2001_RSER, BOTTOM, DN	[118]
DF7	K12	CLK_100M_DB2001_RTHMA, RSER, DP	[117]
DF7F	M11	CLK_100M_DB2001_RTHMA, RSER, DP	[117]
DF6	M11	CLK_100M_DB2001_RSER, TOP, DP	[117]
DF5F	M5	CLK_100M_DB2001_RSER, TOP, DP	[117]
DF5	M7	CLK_100M_DB2001_RSER, MIDDLE, DN	[117]
DF4	M5	CLK_100M_DB2001_RSER, BOTTOM, DP	[117]
DF3	M5	CLK_100M_DB2001_RTHMA, RSER, DP	[118]
DF2	M5	CLK_100M_DB2001_RTHMA, RSER, DP	[118]
DF2F	M1	CLK_100M_DB2001_RSER, TOP, DP	[116]
DF1F	M1	CLK_100M_DB2001_RSER, MIDDLE, DN	[116]
DF1	M1	CLK_100M_DB2001_RSER, BOTTOM, DP	[116]
DF1F	K1	CLK_100M_DB2001_RSER, BOTTOM, DP	[116]

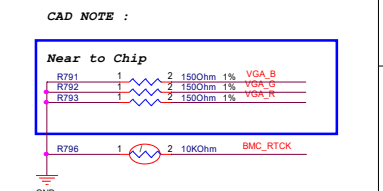
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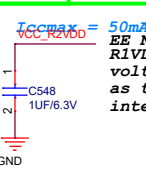
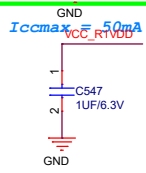
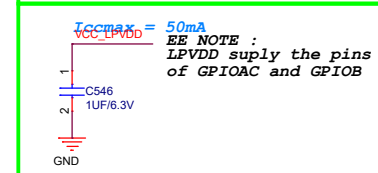
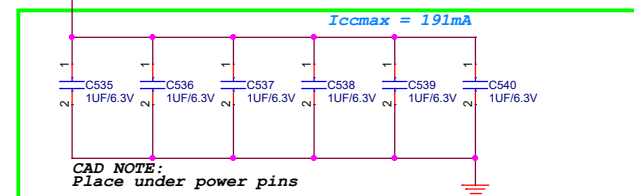
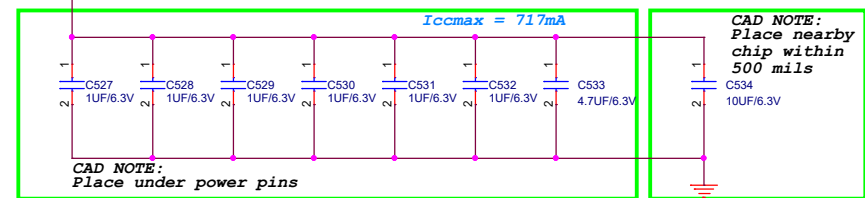
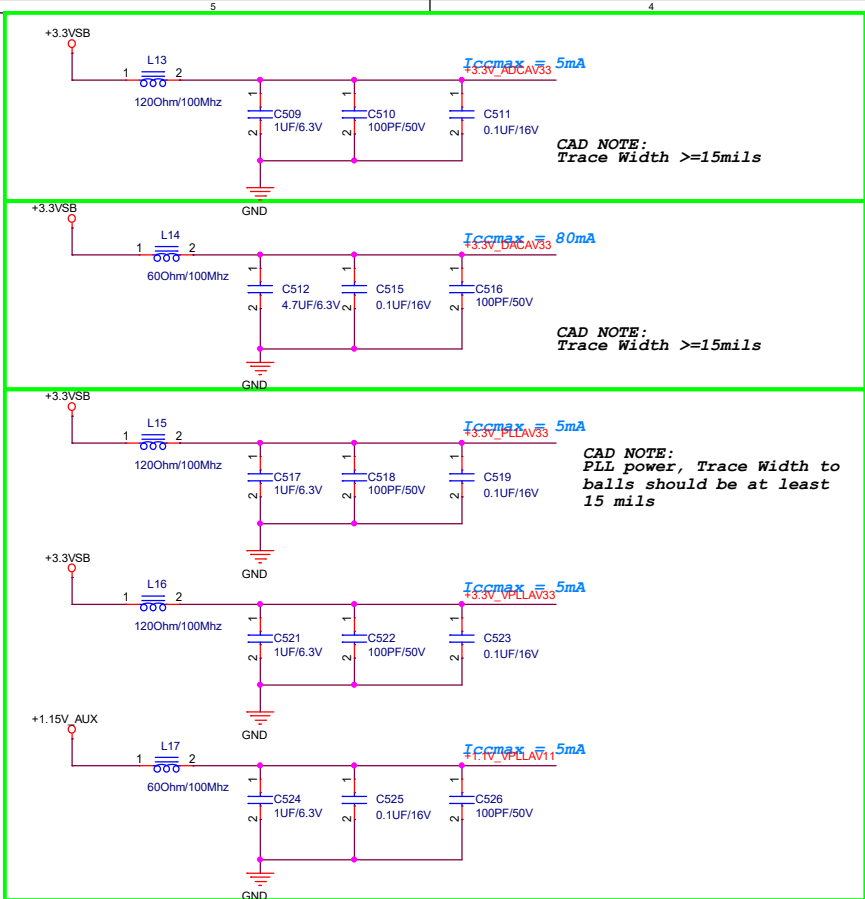
===BMC===



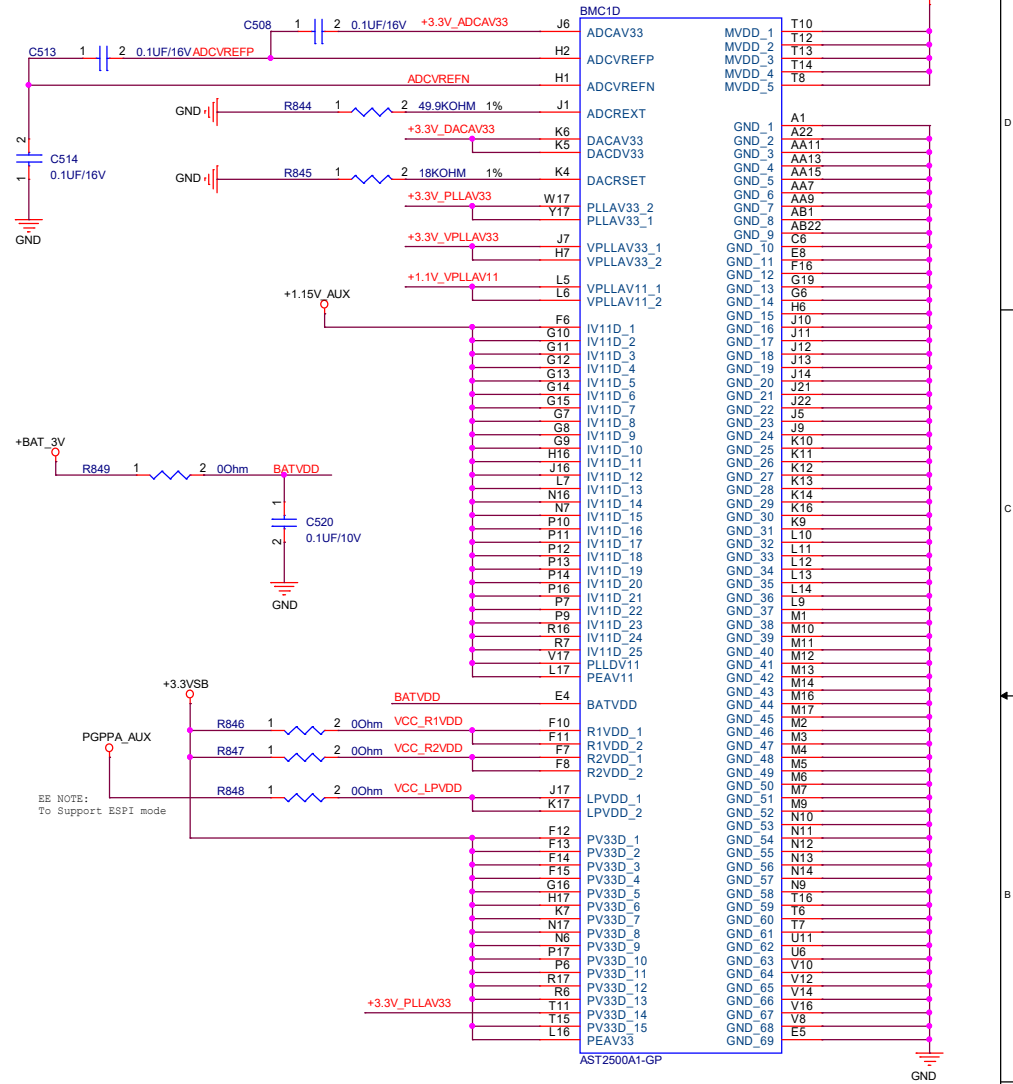
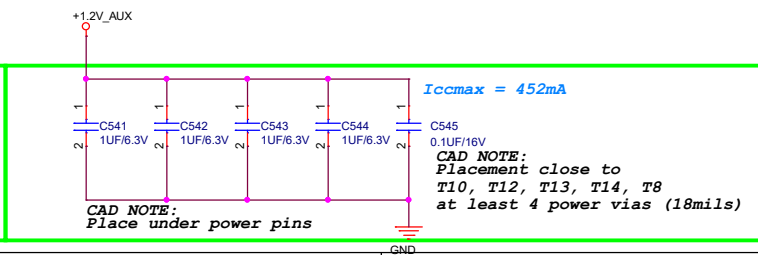








EE NOTE: R1VDD and R2VDD voltage must be the same as the PHY RMII/RGMII interface power



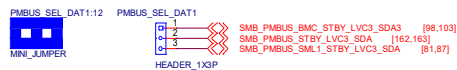
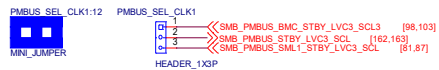




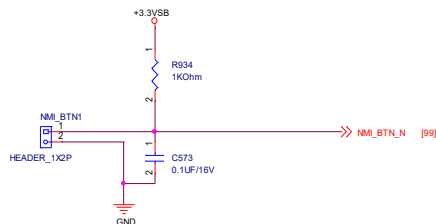
The schematic diagram illustrates the LED driver circuit for the BMC module. A +3VSB input is connected to a 220 Ohm resistor (R912) and the anode of a yellow/green LED (BLED1). The cathode of BLED1 is connected to a node that branches to two 00hm resistors (R913 and R914), which are then connected to BMC\_HB\_LED\_N and BMC\_HB\_LED\_N respectively.

[illegible]

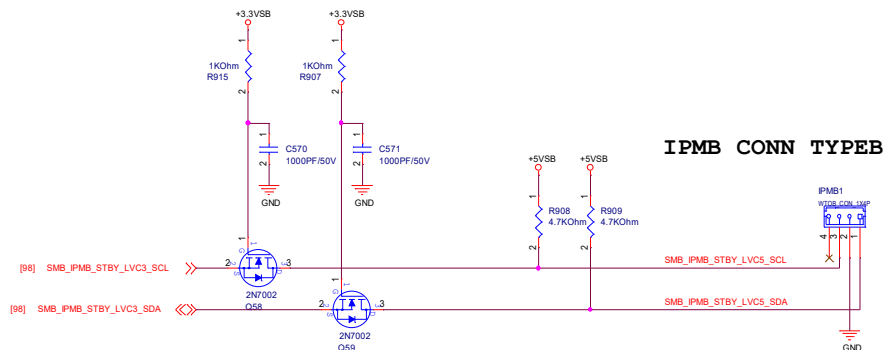
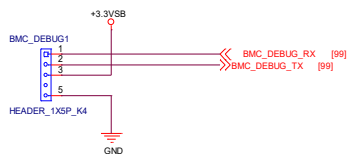
## PMBUS SELECT JUMPER



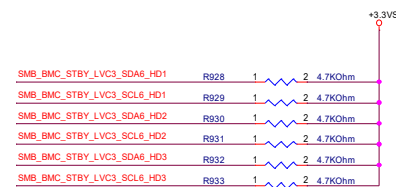
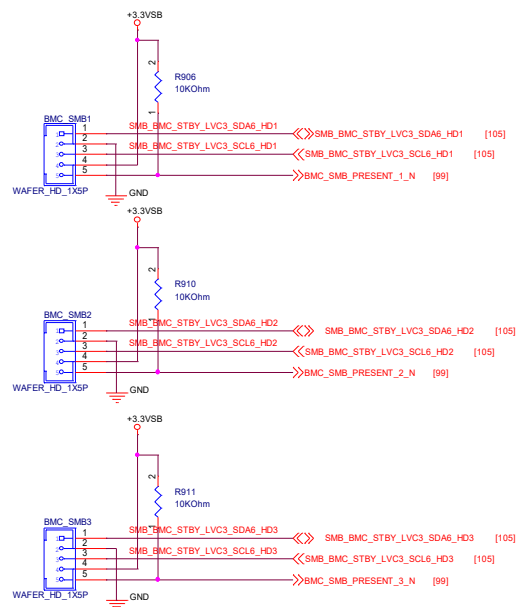
## NMI Button

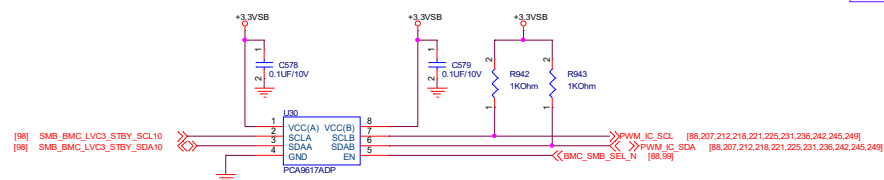
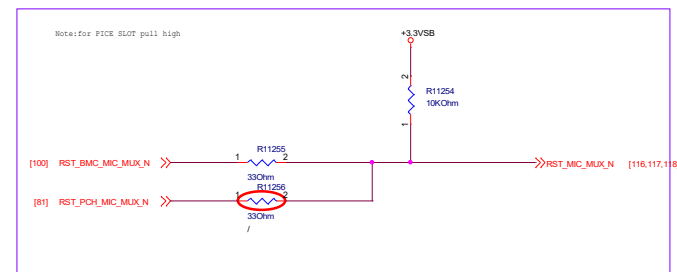
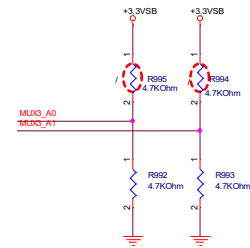
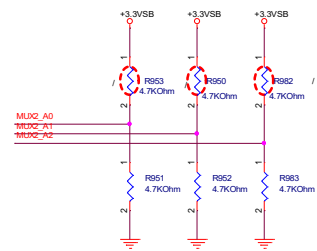
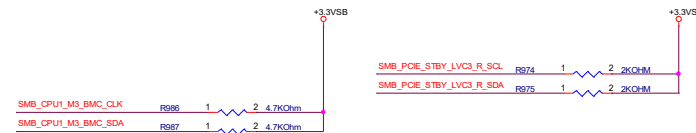
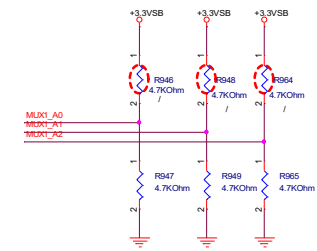
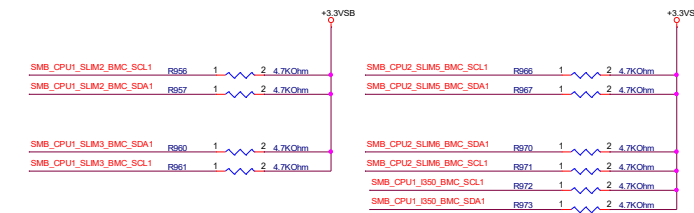


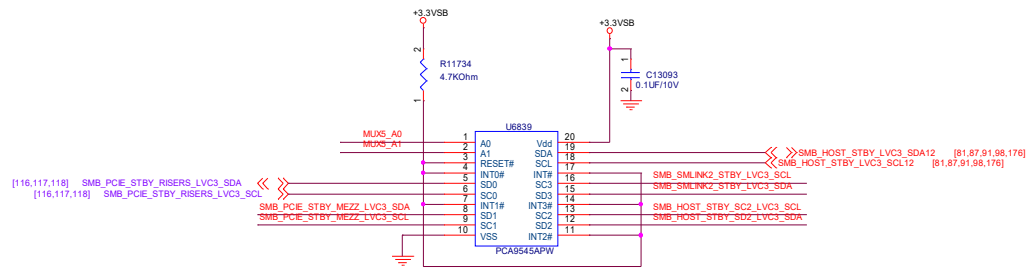
EE NOTE :  
BMC Debug port



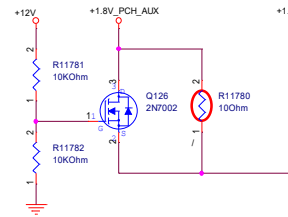
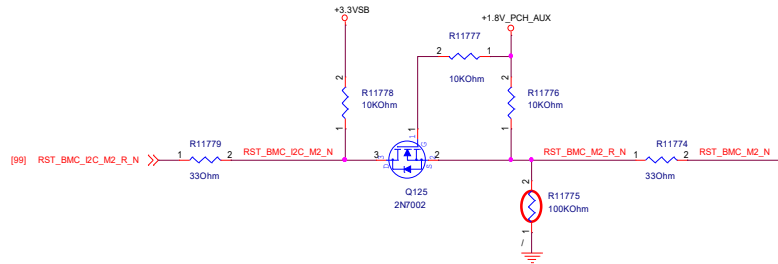
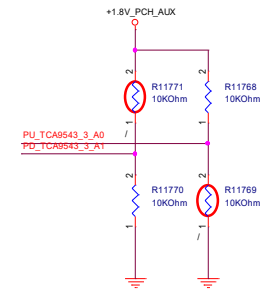
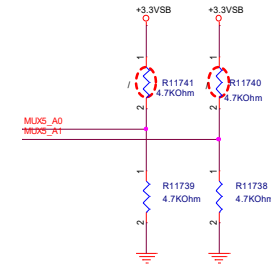
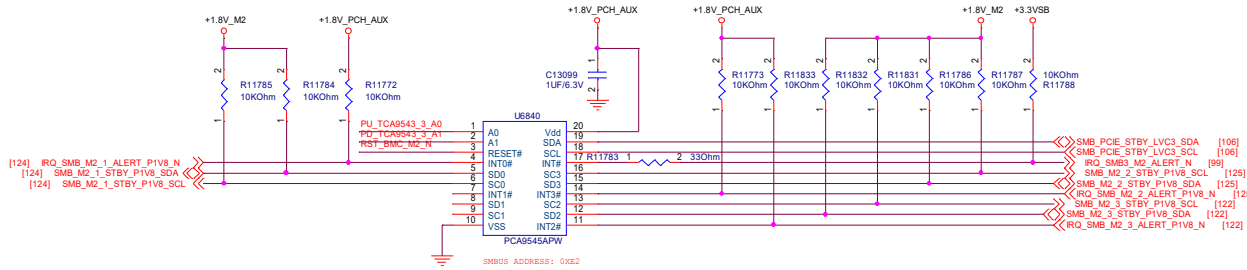
## IPMB CONN TYPEB







SMB_PCIE_STBY_RISERS_LVC3_SDA	R11735	1	2	4.7KOhm
SMB_PCIE_STBY_RISERS_LVC3_SCL	R11737	1	2	4.7KOhm
SMB_PCIE_STBY_MEZZ_LVC3_SDA	R11743	1	2	4.7KOhm
SMB_PCIE_STBY_MEZZ_LVC3_SCL	R11744	1	2	4.7KOhm
SMB_HOST_STBY_SC2_LVC3_SDA	R11745	1	2	4.7KOhm
SMB_HOST_STBY_SC2_LVC3_SCL	R11746	1	2	4.7KOhm
SMB_SMLINK2_STBY_LVC3_SDA	R11747	1	2	4.7KOhm
SMB_SMLINK2_STBY_LVC3_SCL	R11748	1	2	4.7KOhm



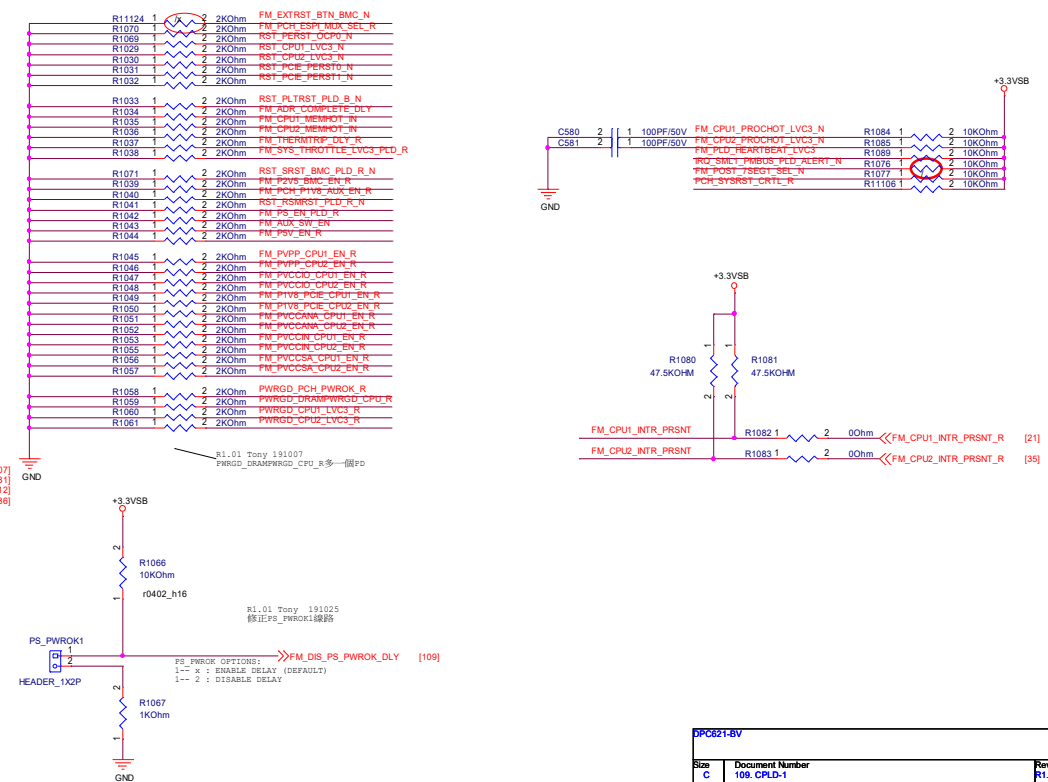
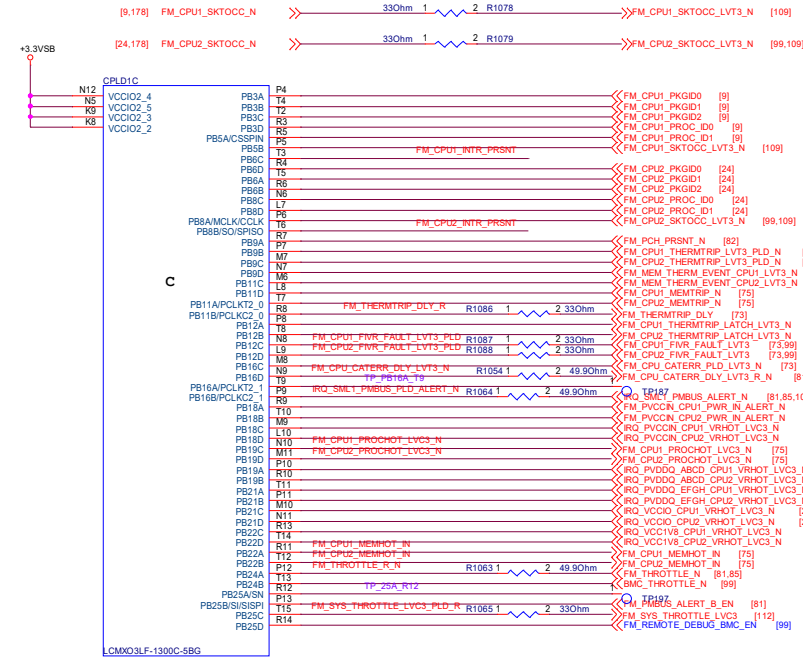
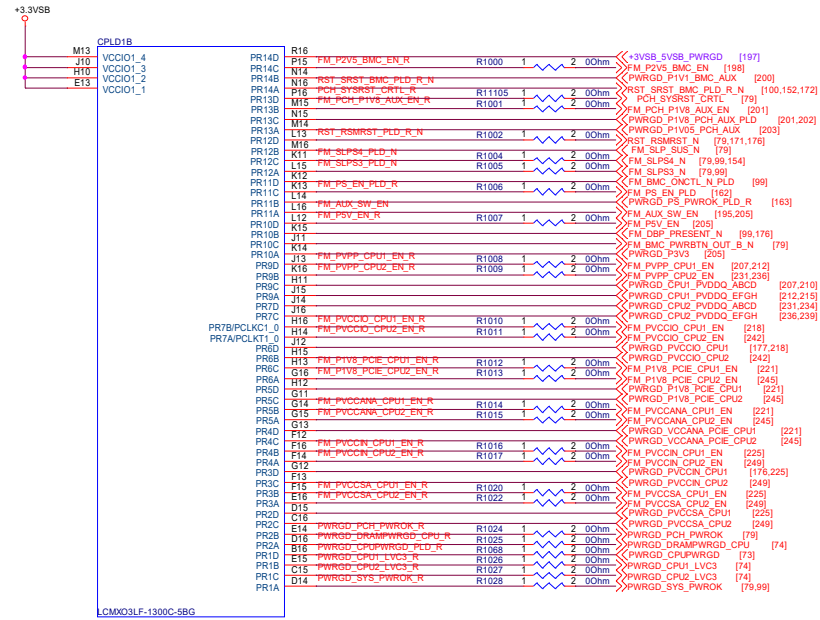
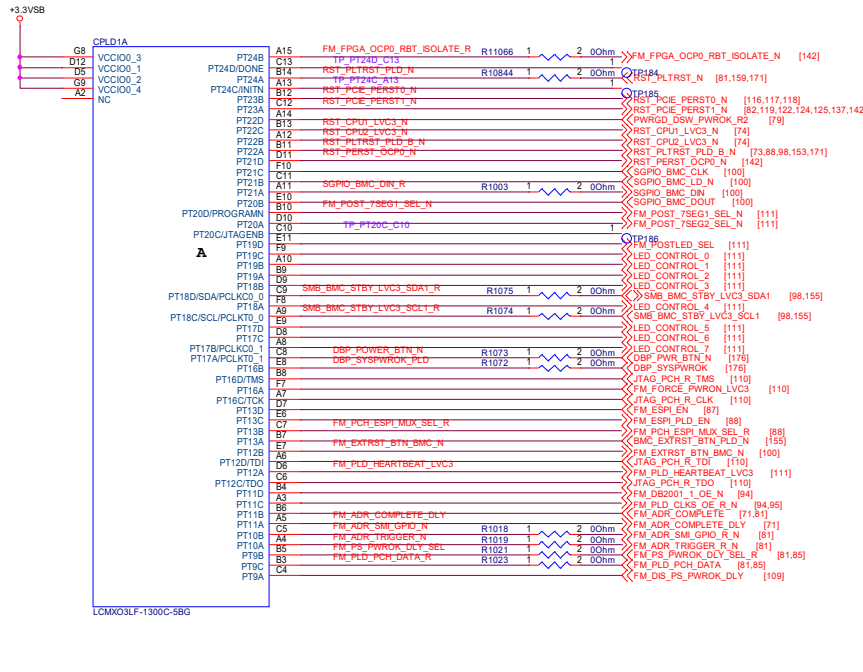
[105] SMB_PCIE_STBY_LVC3_R_SCL	R11794	1	2	330Ohm	SMB_PCIE_STBY_LVC3_SCL	[106]
[105] SMB_PCIE_STBY_LVC3_R_SDA	R11795	1	2	330Ohm	SMB_PCIE_STBY_LVC3_SDA	[106]

JPC021-0V

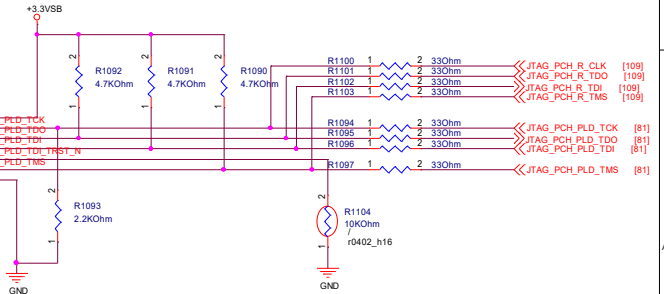
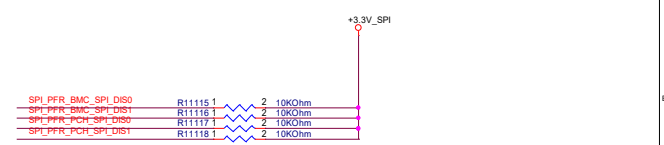
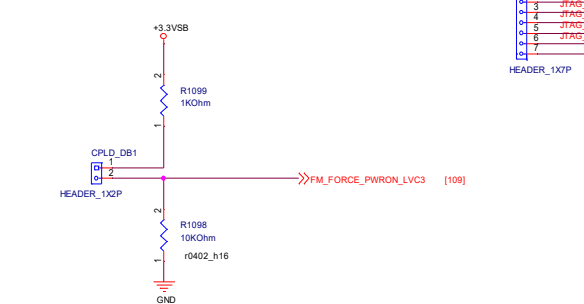
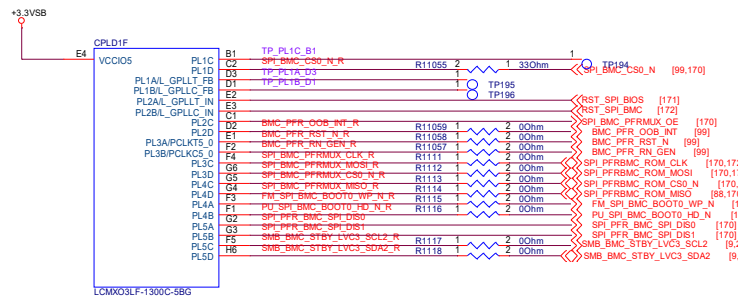
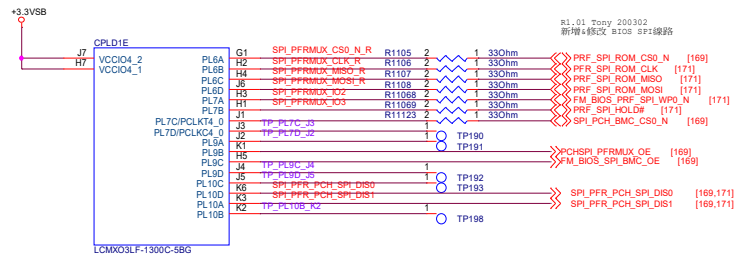
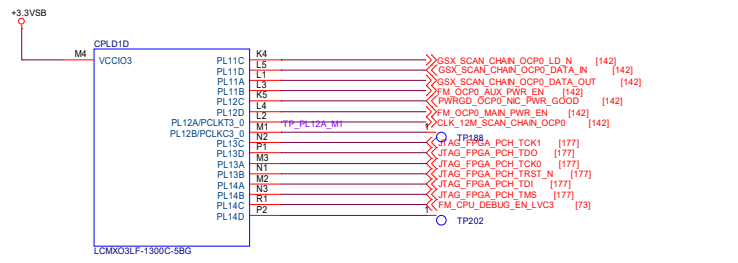
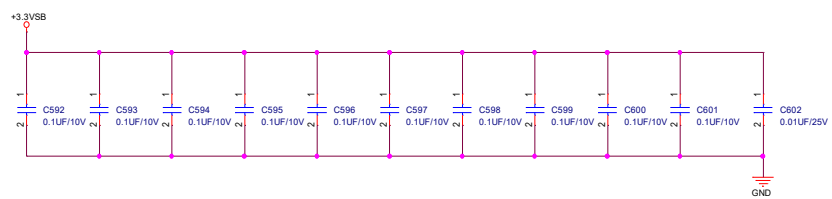
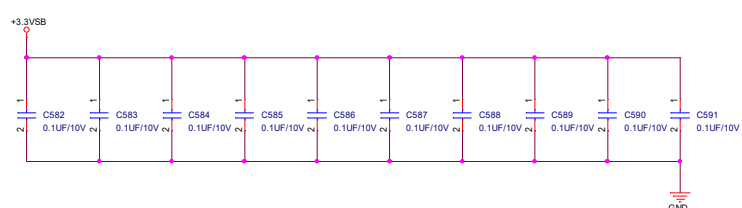
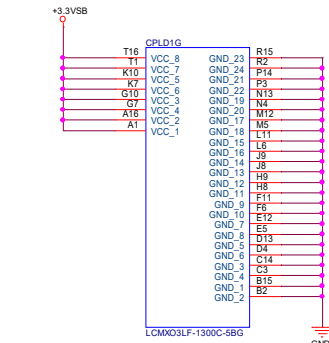


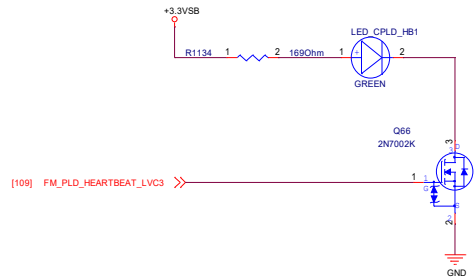
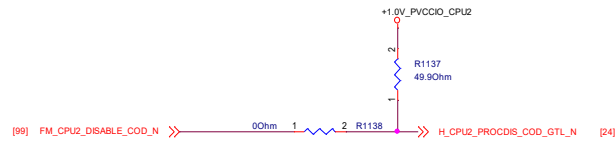
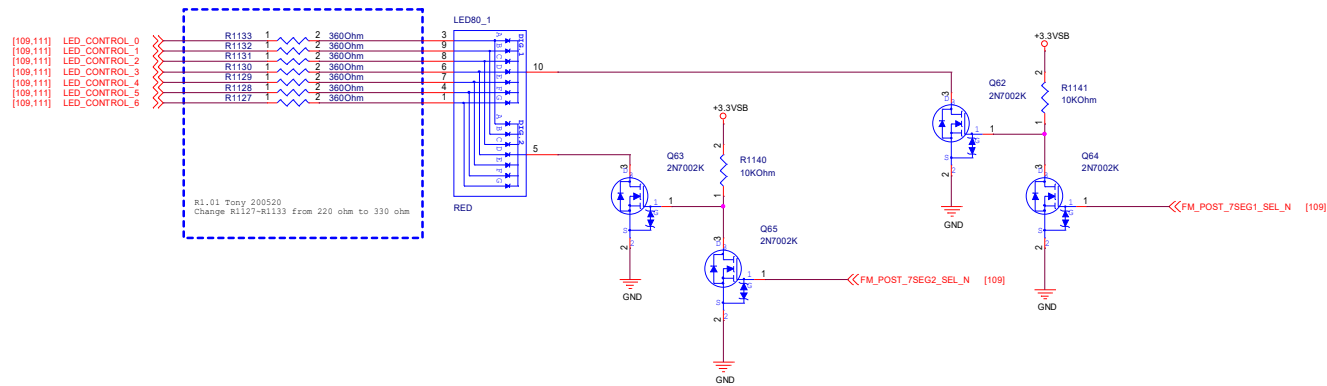
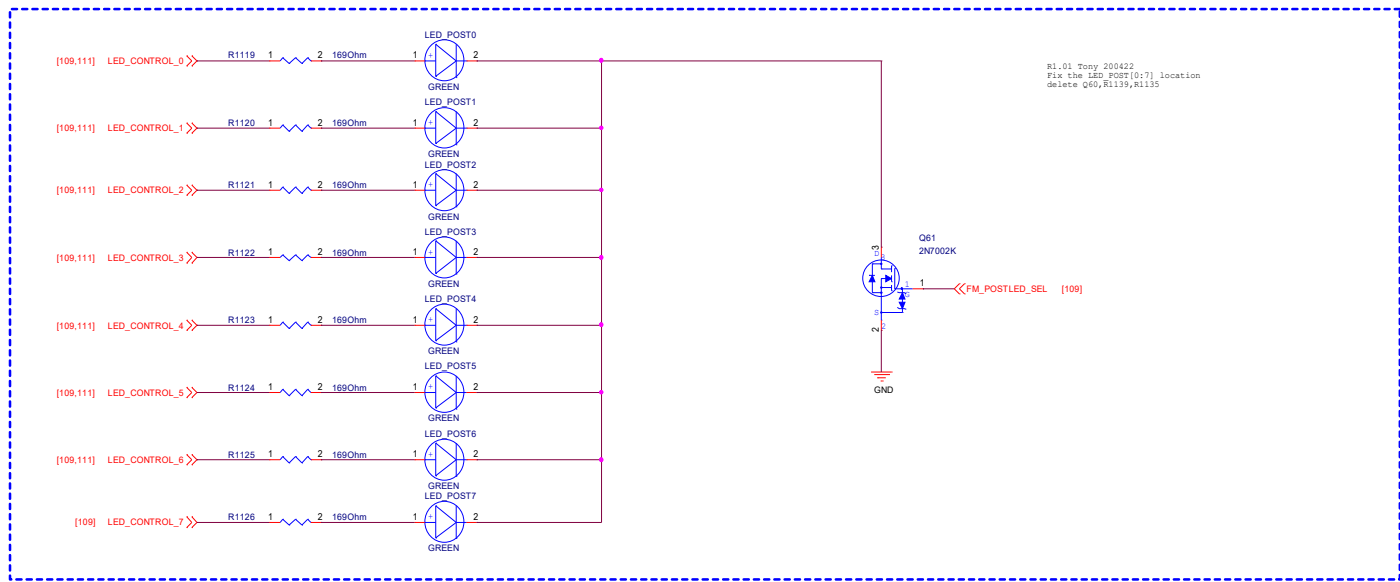
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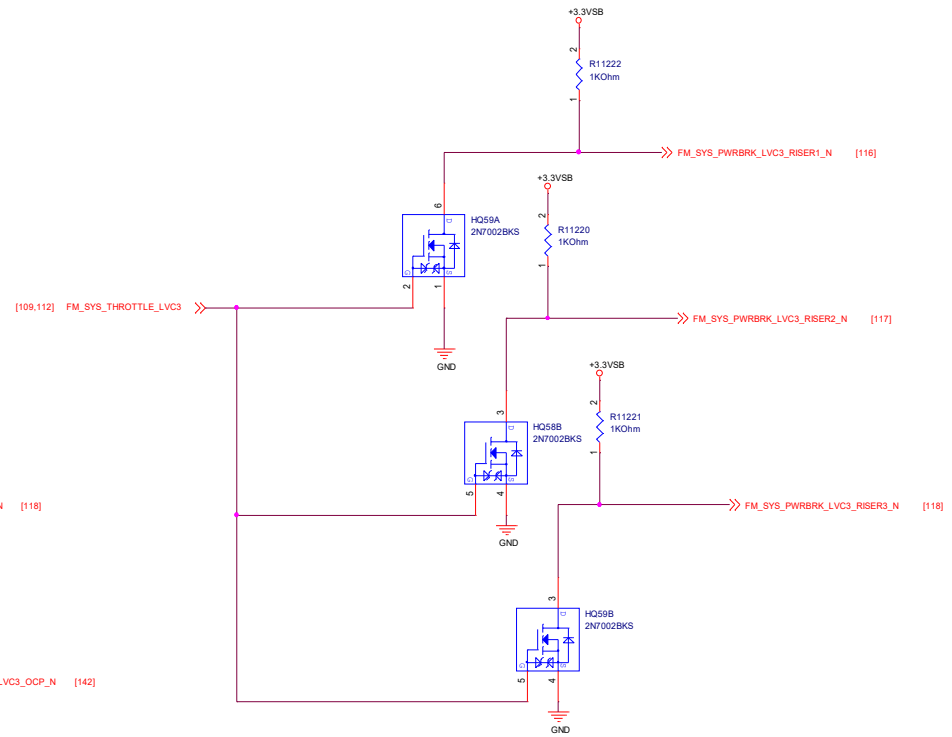
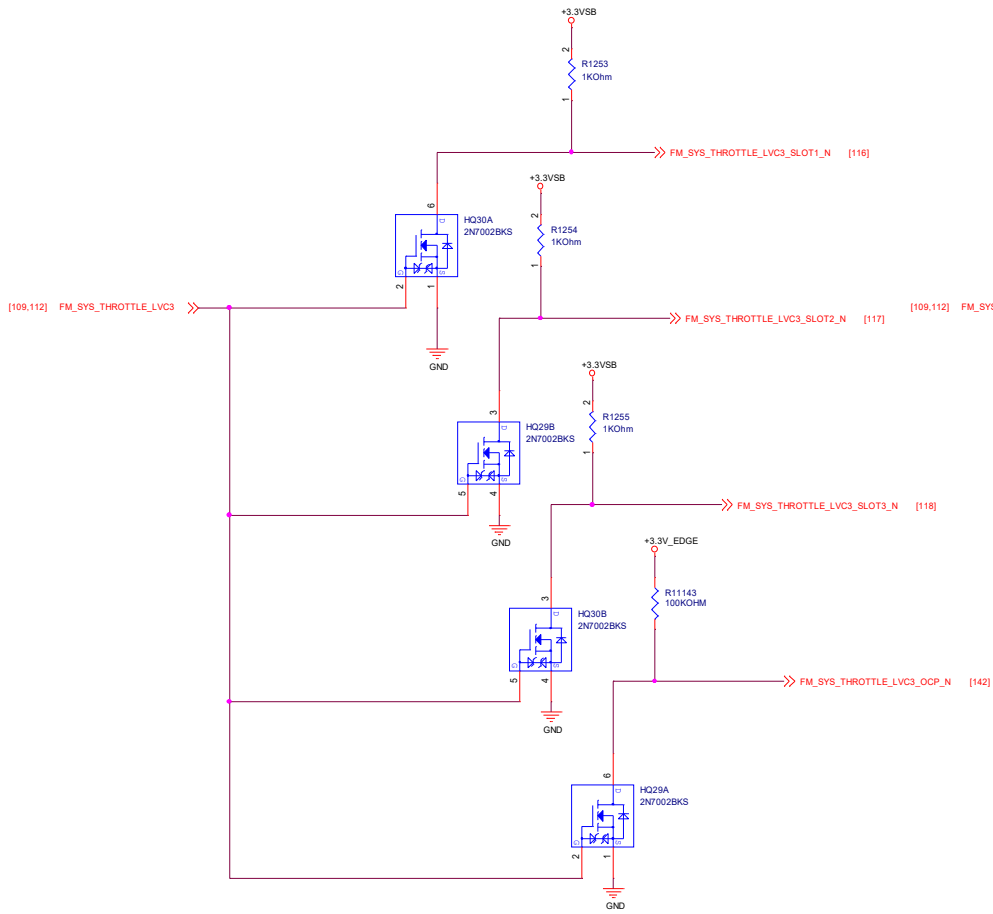
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BOM :CPLD change to 02G019001100AK





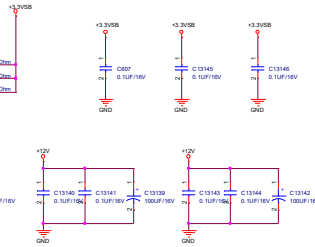


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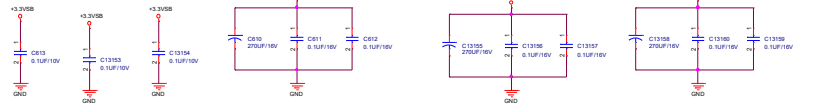
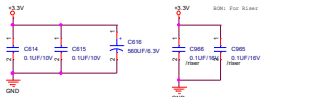
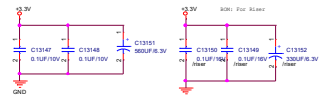
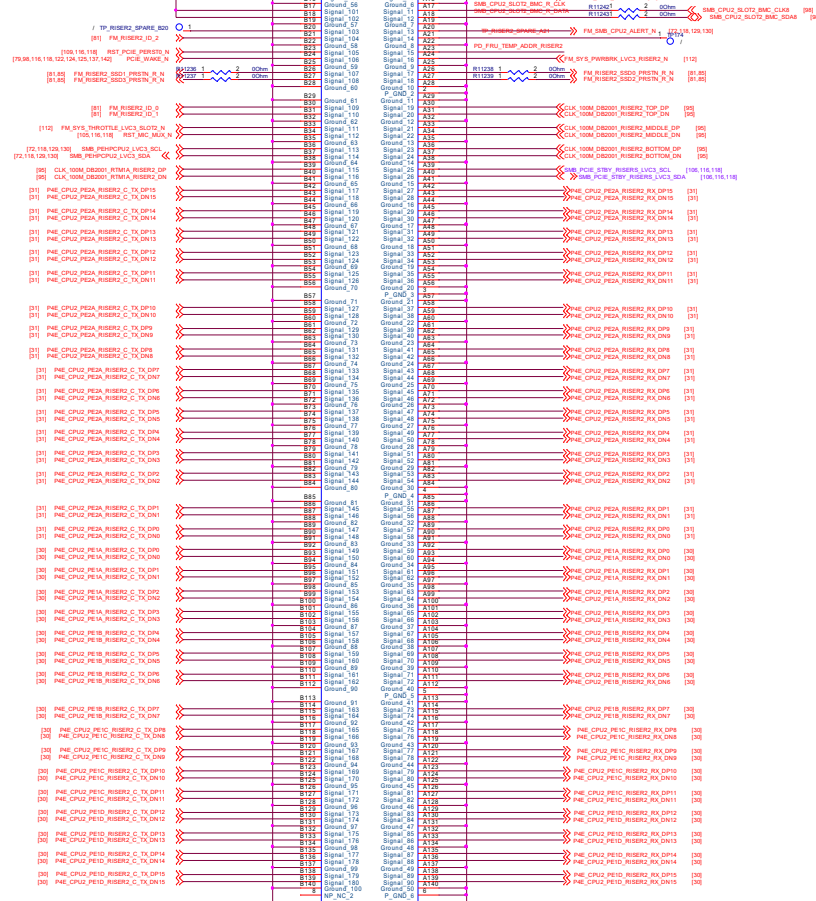
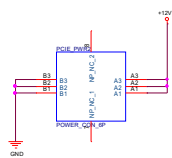


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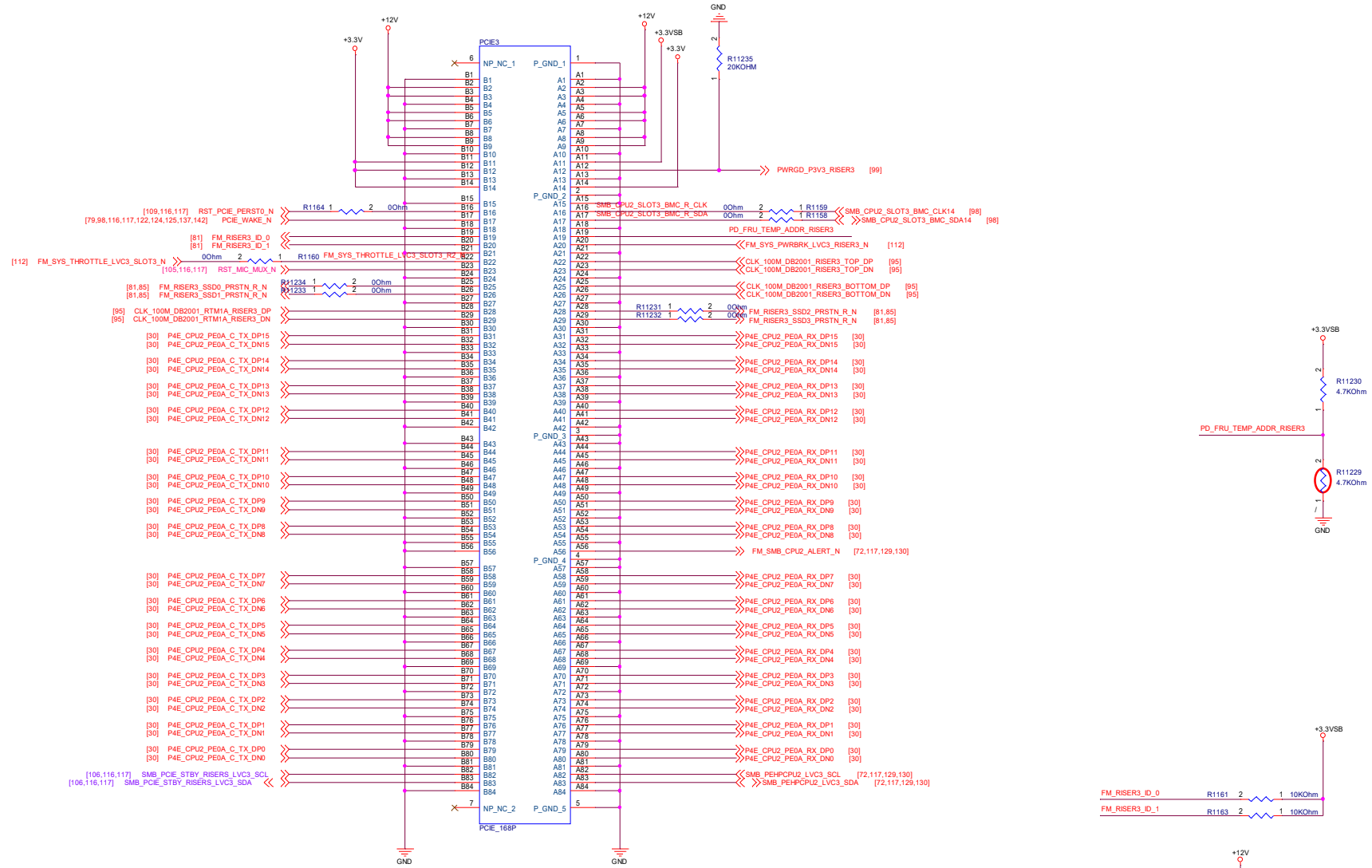
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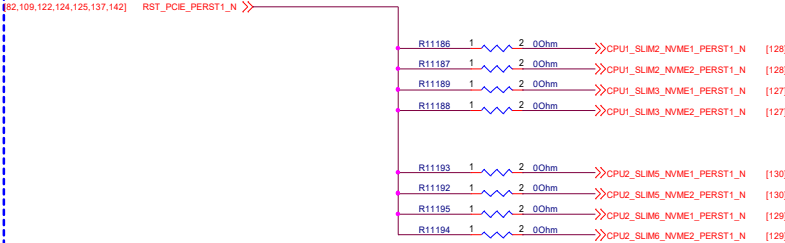
DPC621-BV			
Size	Document Number		Rev
D	116.PCIE_SLOT1(P04)		R1.00
Date:	Thursday, March 24, 2011	Sheet	116 of 203



BOM: PCIe3 change to 12G030021680AK



R1.01 Tony 200311  
修改Slimline reset線路



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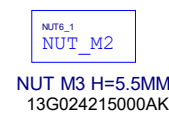
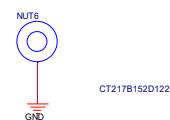
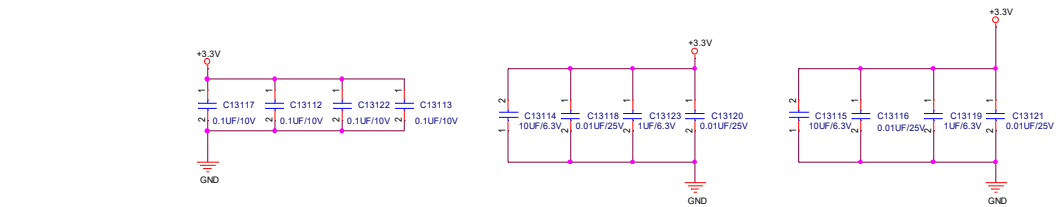
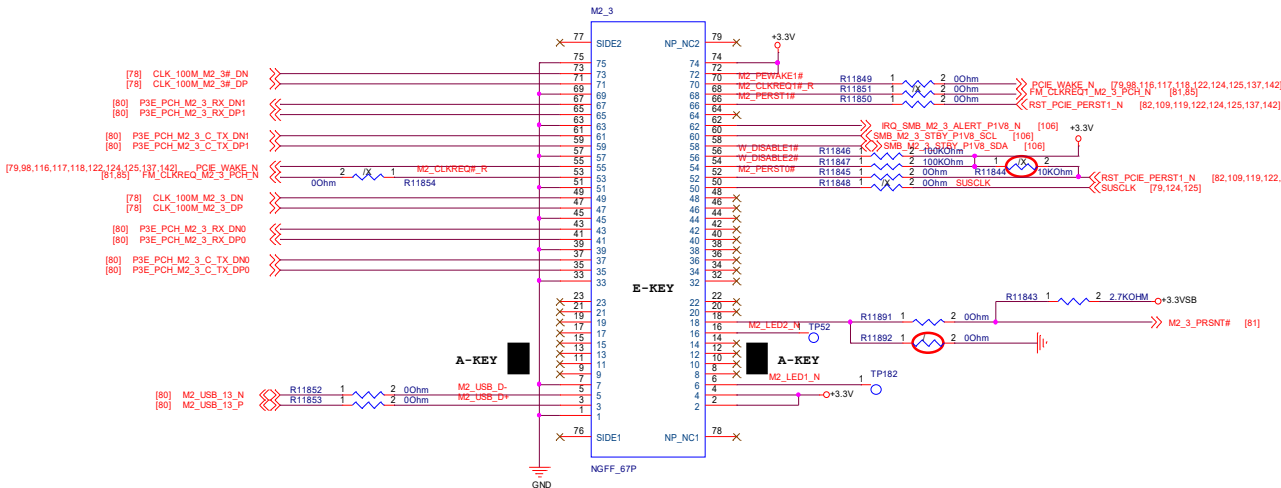


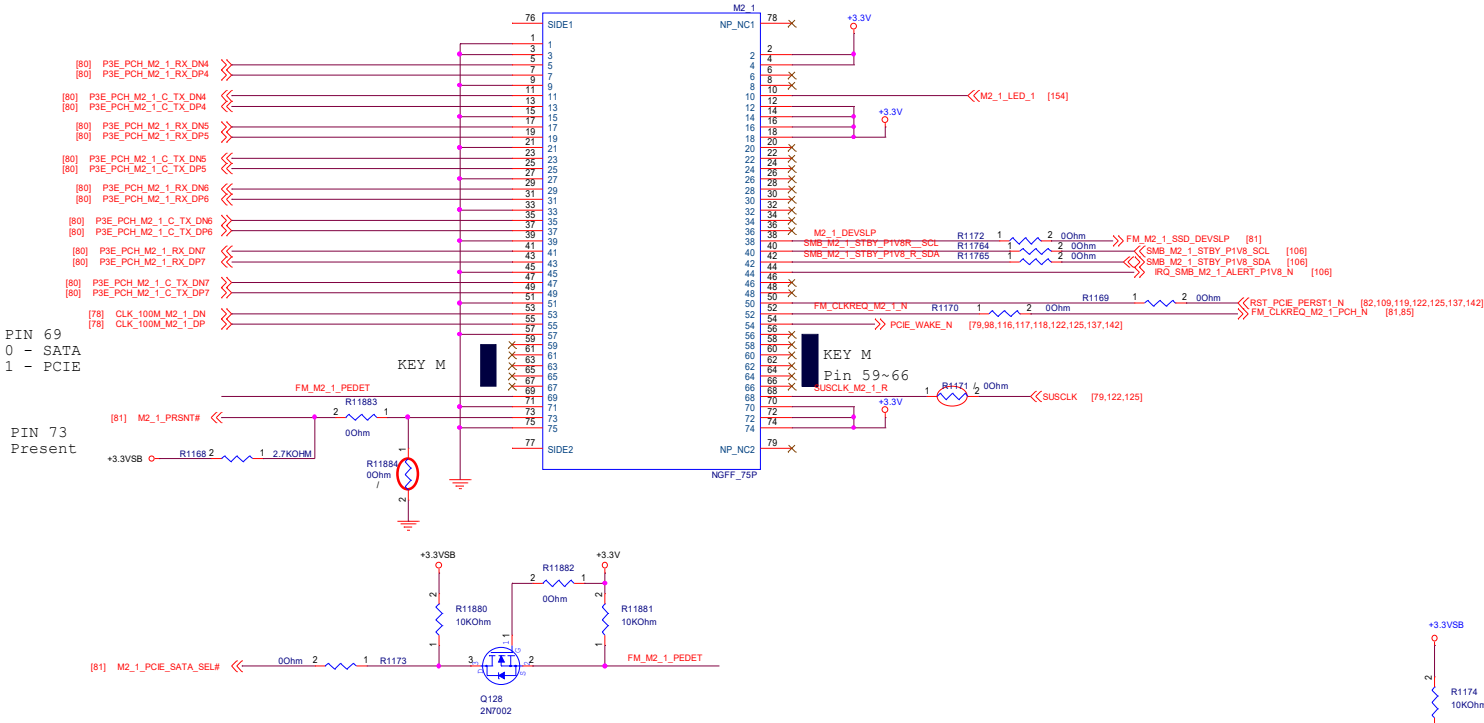
Table 45. Socket 1-SD Pin-Out Diagram (Mechanical Key E) On Platform

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKp1	73
70	UIM_POWER_SRC/GPIO1/PEWAKE1#	RESERVED/REFCLKp1	71
68	UIM_POWER_SINK/CLKREQ1#	RESERVED/PERn1	69
66	UIM_SWP/PERST1#	RESERVED/PERp1	67
64	RESERVED	RESERVED/PERp1	65
62	ALERT# (I/O)(3.3V)	GND	63
60	DC_CLK (O)(0/3.3V)	RESERVED/PETn1	61
58	DC_DATA (I/O)(0/3.3V)	RESERVED/PETp1	59
56	W_DISABLE1# (O)(0/3.3V)	GND	57
54	W_DISABLE2# (O)(0/3.3V)	PEWAKE1# (I/O)(0/3.3V)	55
52	PERST0# (O)(0/3.3V)	CLKREQ0# (I/O)(0/3.3V)	53
50	SUSCLK (32MHz) (O)(0/3.3V)	GND	51
48	COEX1 (I/O)(0/1.8V)	REFCLKn0	49
46	COEX2 (I/O)(0/1.8V)	REFCLKp0	47
44	COEX3 (I/O)(0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (O)(0/1.8V)	PETn0	37
34	UART CTS (I)(0/1.8V)	PETp0	35
32	UART TXD (O)(0/1.8V)	GND	33
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
22	UART RXD (I)(0/1.8V)	SDIO RESET# (O)(0/1.8V)	23
20	UART WAKE# (I)(0/3.3V)	SDIO WAKE# (I)(0/1.8V)	21
18	GND	SDIO DATA# (I/O)(0/3.3V)	19
16	LED2# (I)(GND)	SDIO DATA2 (I/O)(0/1.8V)	17
14	PCM_OUT/25 SD_OUT (O)(0/1.8V)	SDIO DATA3 (I/O)(0/1.8V)	15
12	PCM_IN/25 SD_IN (I)(0/1.8V)	SDIO DATA4 (I/O)(0/1.8V)	13
10	PCM_SYNC/25 WS (O)(0/1.8V)	SDIO CMD0 (I/O)(0/1.8V)	11
8	PCM_CLK/25 SCK (O)(0/1.8V)	SDIO CLK (O)(0/1.8V)	9
6	LED1# (I)(GND)	GND	7
4	3.3V	USB_D-	5
2	3.3V	USB_D+	3
		GND	1

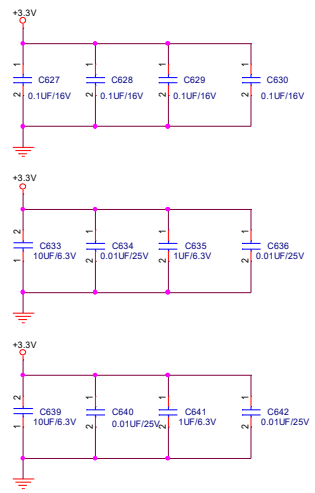
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- 1.SIO GP73 ( PIN90 ) for M.2 config ( 偵測插入M.2卡的類型 , low為SATA , high為PCIE )  
2.PCH GPIO9 = low = SATA mode, high = PCIE mode  
3.PCH SSATA3 share with M.2 SATA  
4.SIO GP72 ( PIN91 ) for M.2 present detect ( low=present )

R1.01  
BOM:Change 12G030100672AK to 12G030100678AK

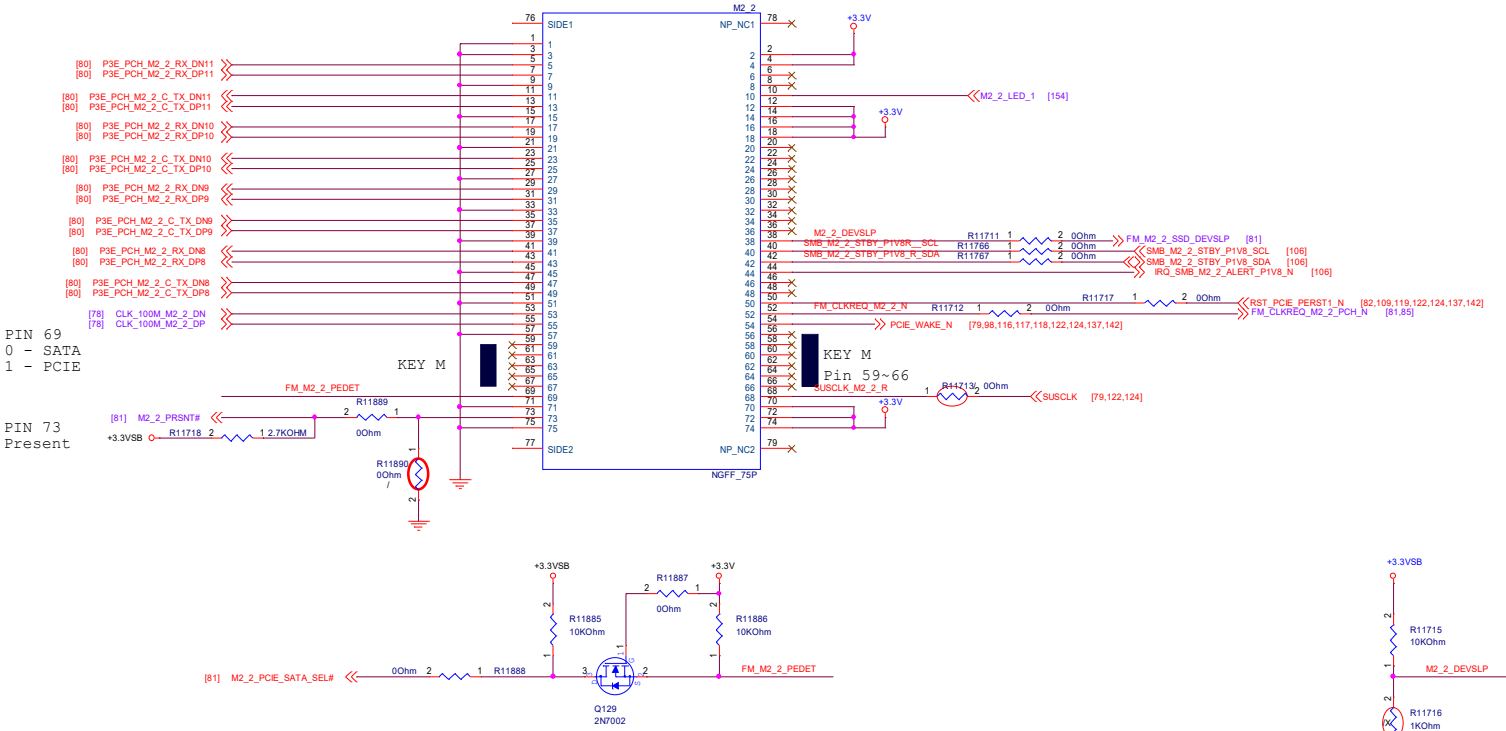


74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(30MHz) (0)(0/3.3V)	PEDET (NC-PCh/GND-SATA)	69
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PERMANENT(0)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQM(1)(0)(0/3.3V) or N/C	GND	51
50	PERSTW(0)(0/3.3V) or N/C	PETH0/SATA-A	49
48	N/C	PETH0/SATA-A	47
46	N/C	GND	45
44	N/C	PERIO/SATA-B	43
42	N/C	PERHO/SATA-B	41
40	N/C	GND	39
38	DEVSLP (0)	PETH1	37
36	N/C	PETH1	35
34	N/C	GND	33
32	N/C	PERD1	31
30	N/C	PERD1	29
28	N/C	GND	27
26	N/C	PETH2	25
24	N/C	PETH2	23
22	N/C	GND	21
20	N/C	PERD2	19
18	3.3V	PERD2	17
16	3.3V	GND	15
14	3.3V	PETH3	13
12	3.3V	PETH3	11
10	DAS/DSSM(1)(0/1/3.3V)	GND	9
8	N/C	PERD3	7
6	N/C	PERD3	5
4	3.3V	GND	3
2	3.3V	GND	1

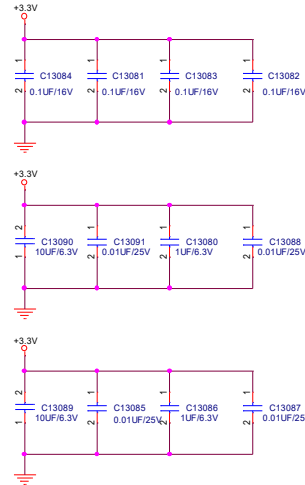
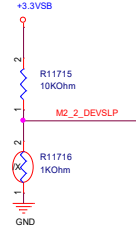


- 1.SIO GP73 ( PIN90 ) for M.2 config ( 偵測插入M.2卡的類型 , low為SATA , high為PCIE )  
2.PCH GPIO9 = low = SATA mode, high = PCIE mode  
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4.SIO GP72 ( PIN91 ) for M.2 present detect ( low=present )

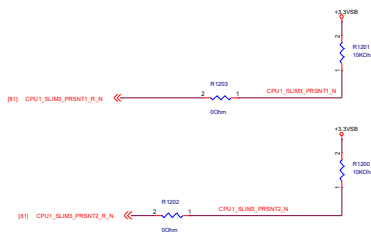
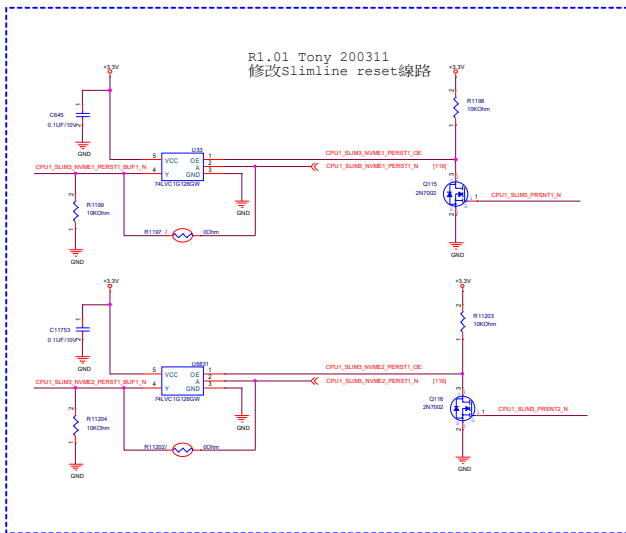
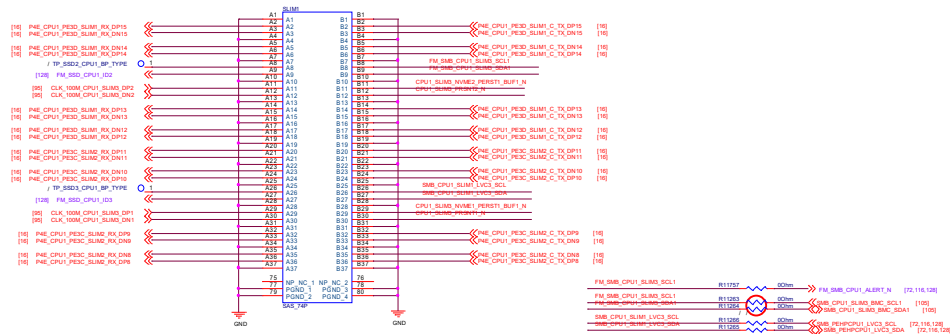
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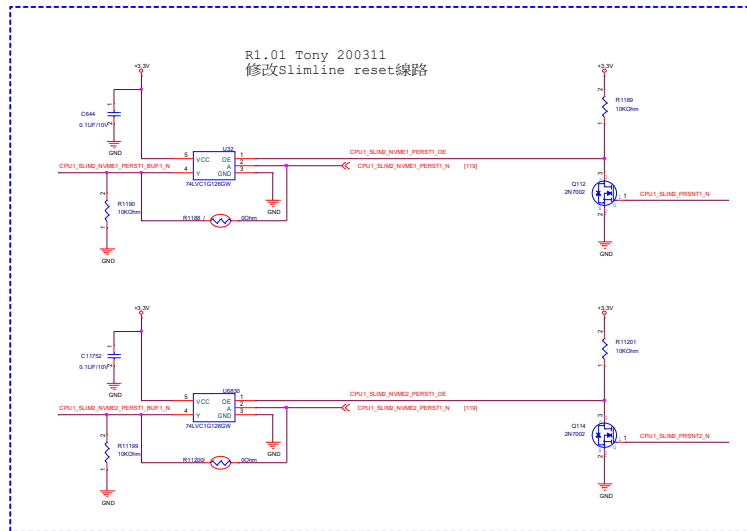
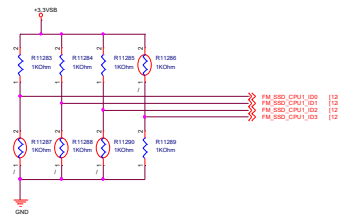


74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32KHz) (O)(V3.3V)	PEDET (NC, PCH/GND-SATA)	69
	Connector Key	Connector Key	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKER (I/O)(V3.3V) or N/C	REFCLKN	53
52	CLKREQ (I/O)(V3.3V) or N/C	GND	51
50	PERST# (O)(V3.3V) or N/C	PETH0/SATA-A+	49
48	N/C	PETH0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERH0/SATA-B+	43
42	N/C	PERH0/SATA-B-	41
40	N/C	GND	39
38	DEVSLP (O)	PETH1	37
36	N/C	PETH1	35
34	N/C	SHD	33
32	N/C	PERD1	31
30	N/C	PETH2	29
28	N/C	GND	27
26	N/C	PETH2	25
24	N/C	PETH2	23
22	N/C	GND	21
20	N/C	PERD2	19
18	3.3V	PERH2	17
16	3.3V	SHD	15
14	3.3V	PETH3	13
12	3.3V	PERD3	11
10	DAS/DSH (I/O)(LED1#) (V3.3V)	GND	9
8	N/C	PERD3	7
6	N/C	PERD3	5
4	3.3V	GND	3
2	3.3V	GND	1



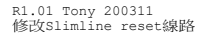
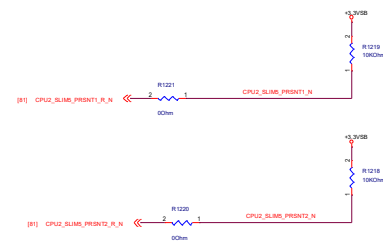
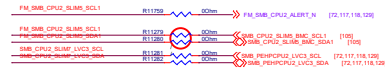
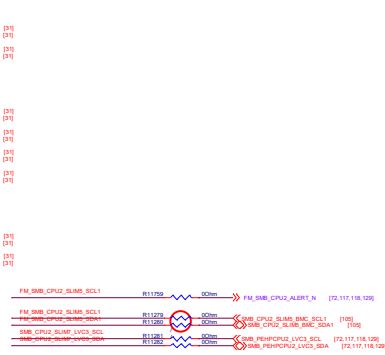












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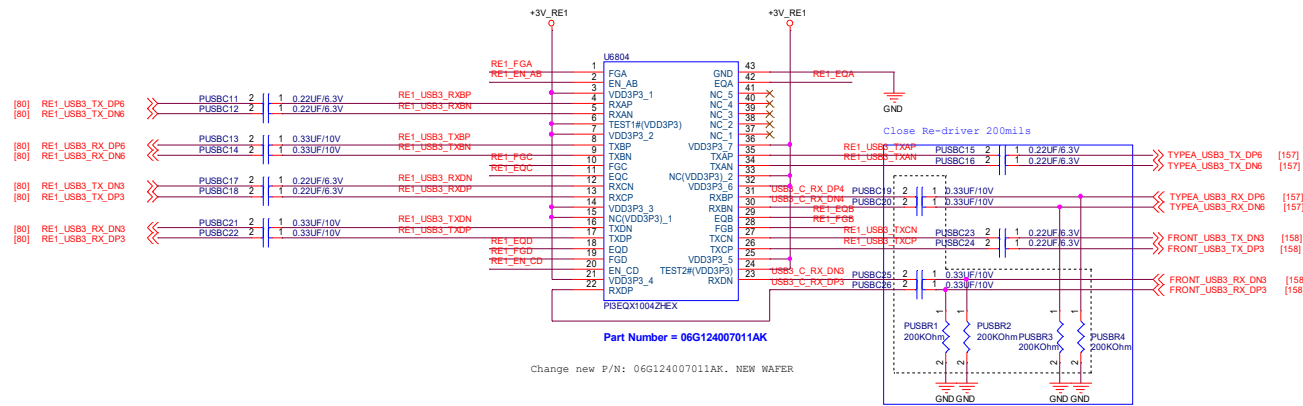
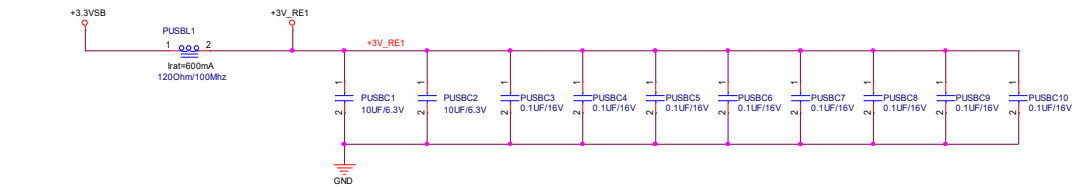
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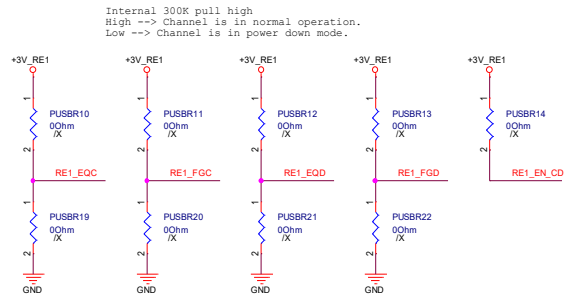
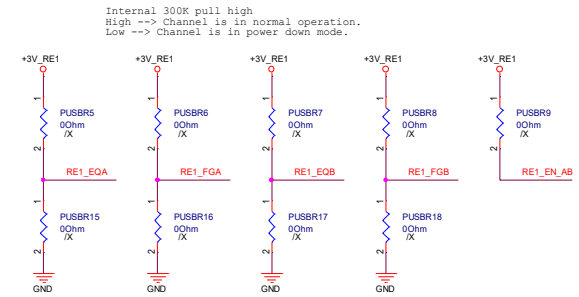
DPC821-BV

Size C	Document Number 131.Blank	Rev R1.0
Date: Tuesday, March 14, 2023	Sheet 131 of 253	

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Technmosa recommend to reserve for the device which has MUX on it.



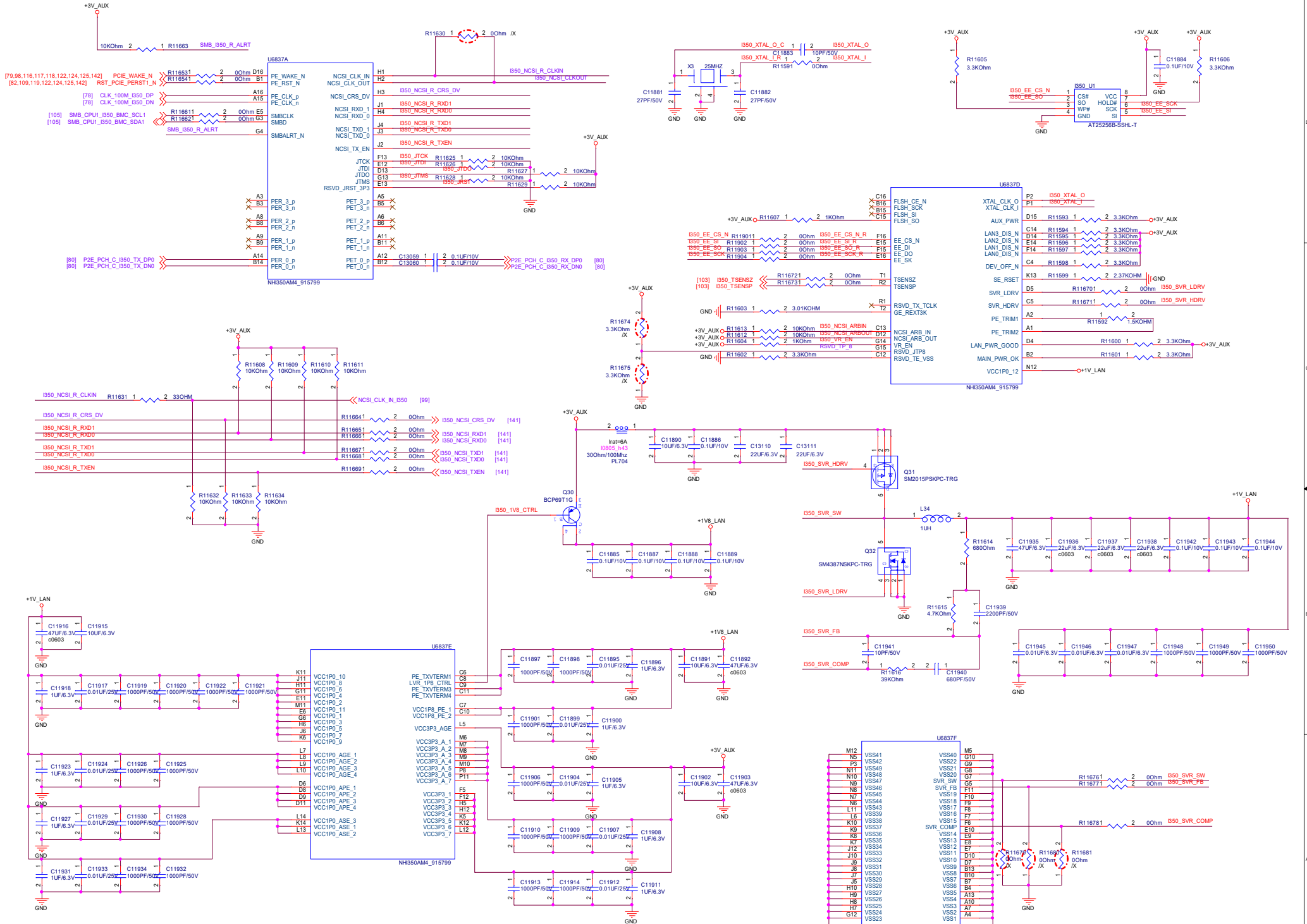
Internal 300K pull high  
High --> Channel is in normal operation.  
Low --> Channel is in power down mode.

Internal 300K pull high  
High --> Channel is in normal operation.  
Low --> Channel is in power down mode.

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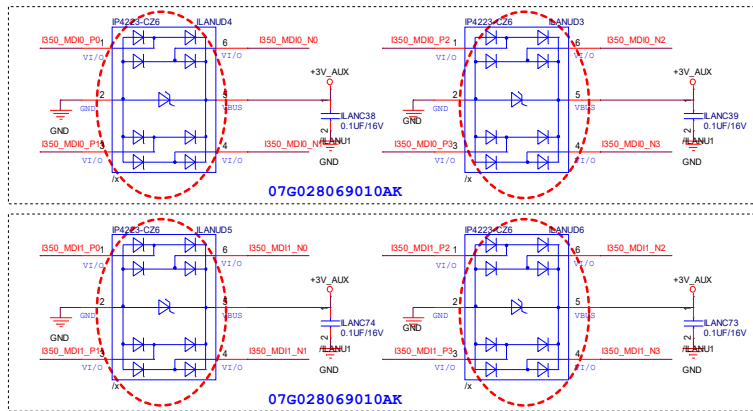
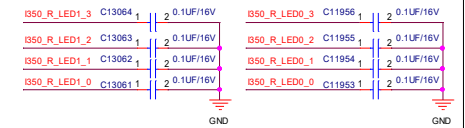
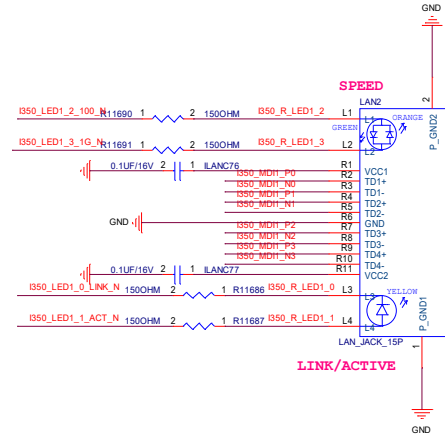
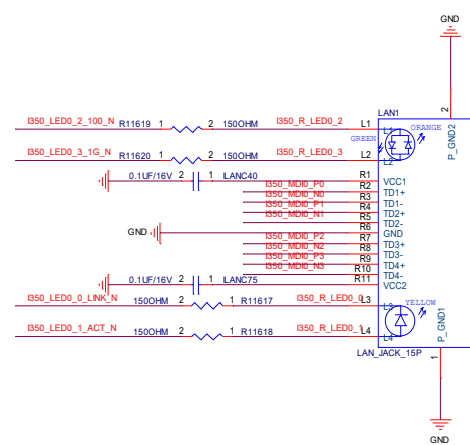
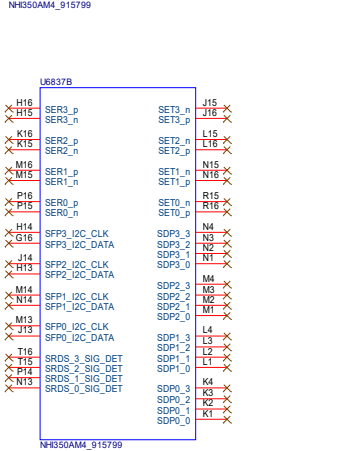
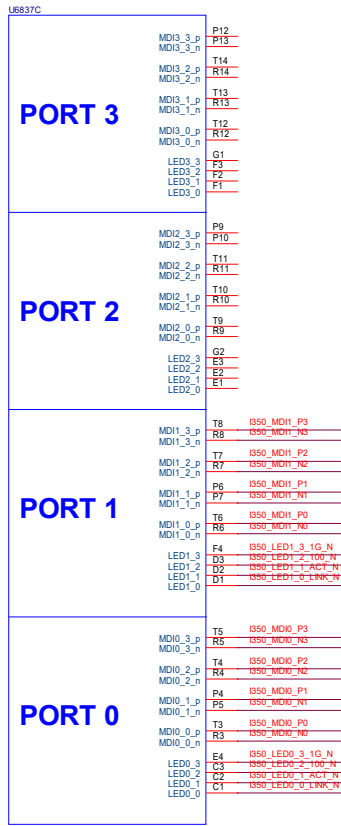


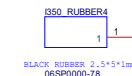
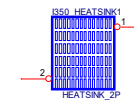
Table 5-1. Power Limits by Form-Factor

Main	LOM
Auxiliary (aux enabled)	N/A
Auxiliary (aux disabled)	375 mA @ 3.3 V
	20 mA @ 3.3 V

Left LED:  
1. Yellow : Activity

Right LED:  
1. Green : 1000Mbps  
2. Orange : 100Mbps  
3. No Light : 10Mbps

	1G	100M	
I1000#	Low	High	
I100#	High	Low	
	High	High	



LED0->LINK UP IS LOW, LINK DOWN IS HIGH.  
CONNECT LED0 TO CATHODE OF GREEN LINK/ACTIVITY LED

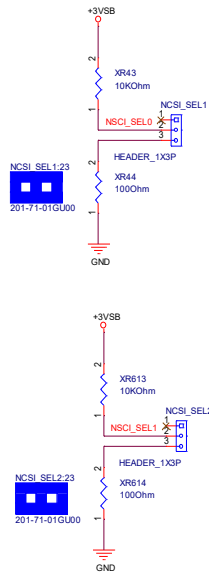
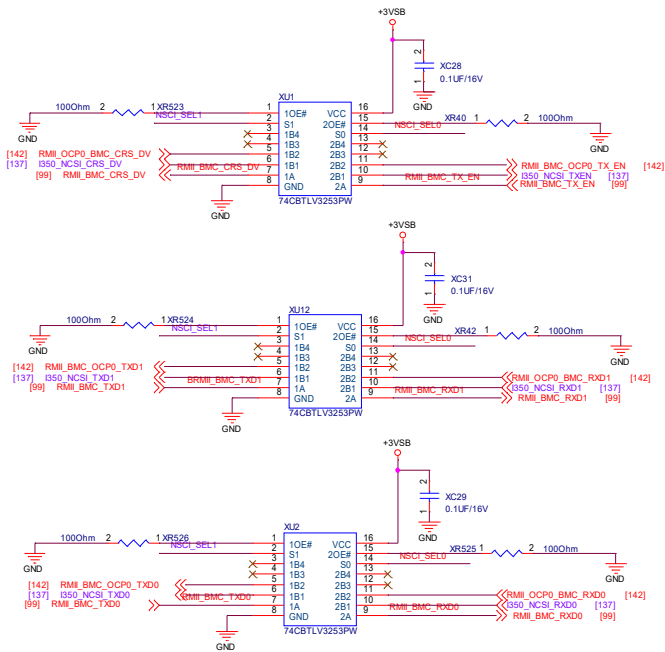
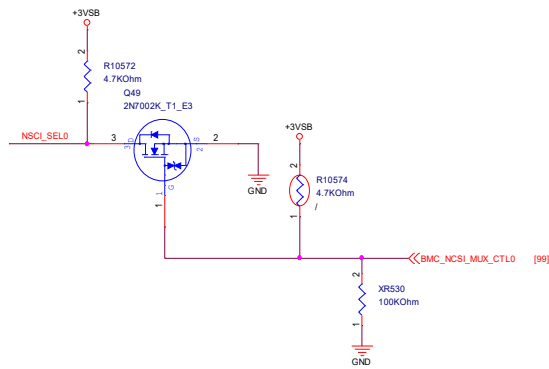
LED1->NORMALLY HIGH, BLINKS LOW FOR FILTERED ACTIVITY.  
CONNECT LED1 TO ANODE OF LINK/ACTIVITY LED

LED2->IF LINKED AT 100BASE-TX THEN LOW  
CONNECT LED2 TO CATHODE OF GREEN SPEED LED AND THE ANODE OF THE ORANGE SPEED LED.

LED3->IF LINKED AT 1000BASE-T THEN LOW  
CONNECT LED3 TO CATHODE OF ORANGE SPEED LED AND THE ANODE OF THE GREEN SPEED LED.

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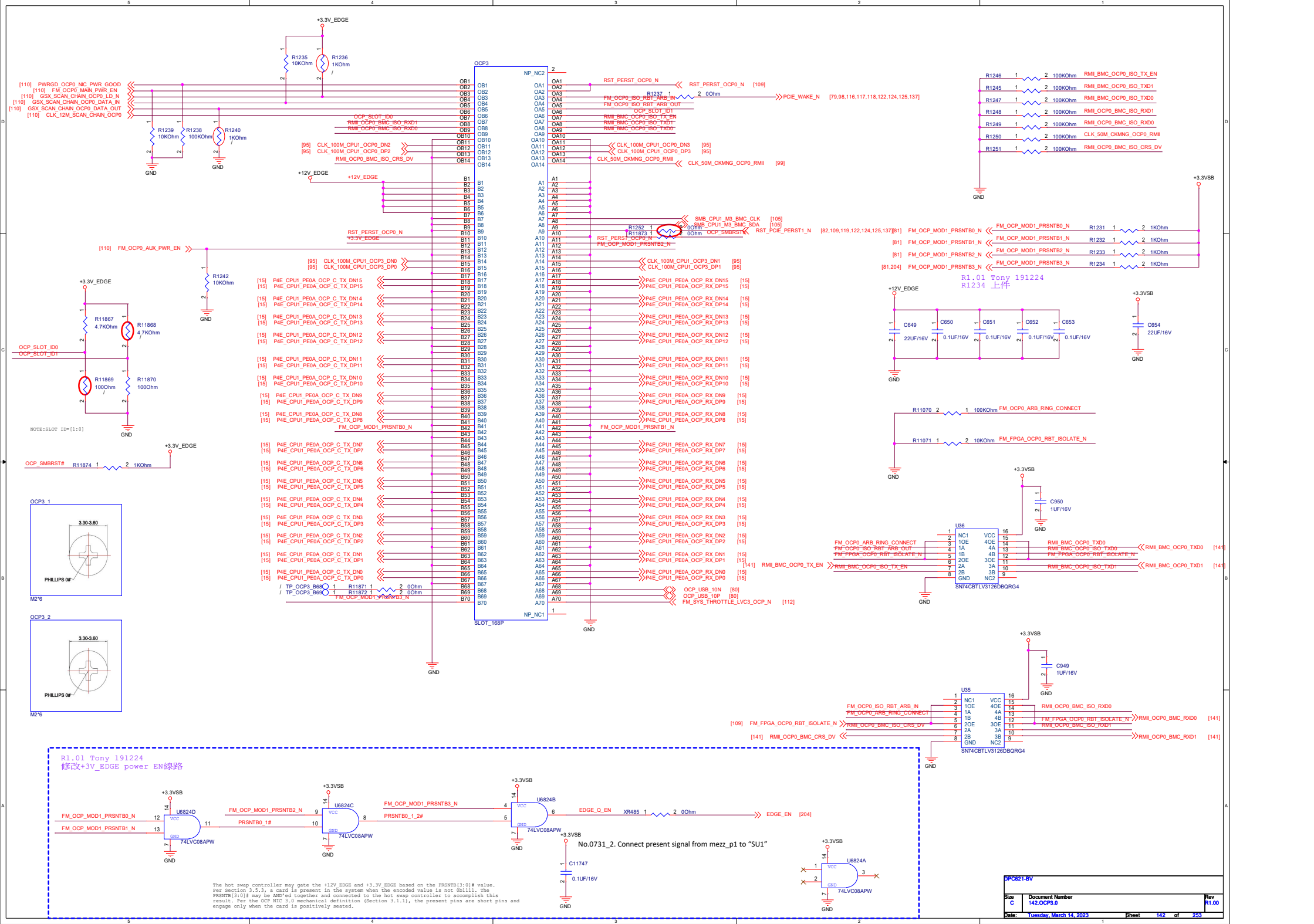


## 6. Functional description

Table 3. Function table

Inputs	1OE#	2OE	S1	S0	Function switch
X	H	X	X	X	disconnect 2A and 2Bn
H	X	X	X	X	disconnect 1A and 1Bn
L	L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	L	H	H	1A to 1B4 and 2A to 2B4

NCSI_SEL		
S1	S0	Optional
0	0	I210_0 (default)
0	1	OCF3.0
1	0	Mezzanine card
1	1	N/A





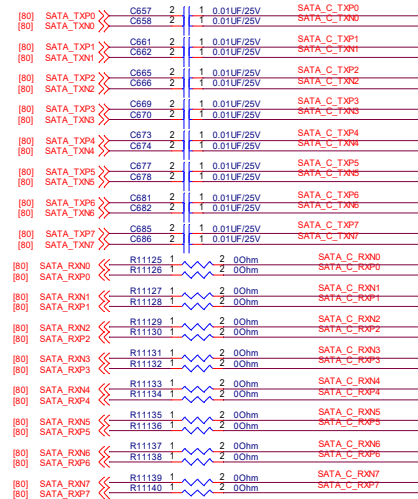
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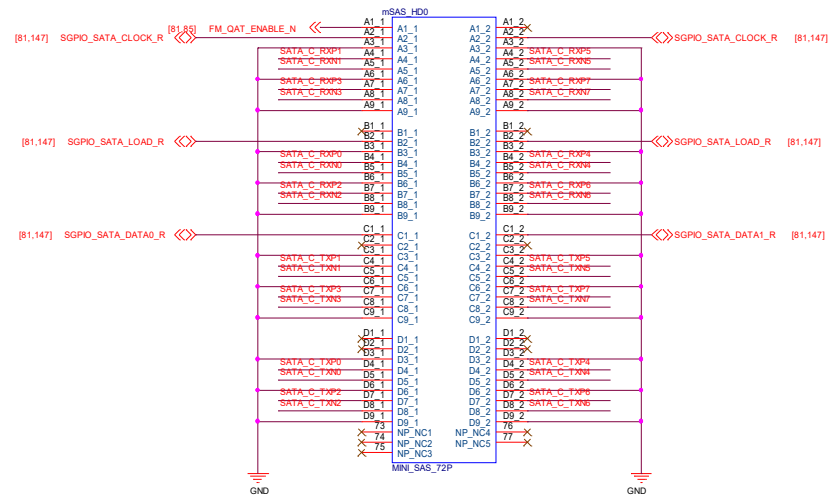
====SATA&SAS====

CAD: TX PLACE CAPS CLOSE TO LRG.

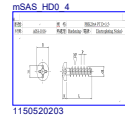
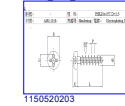


CAD: RX PLACE CAPS CLOSE TO CONNECTOR.

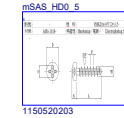
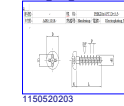
## MINI SAS HD



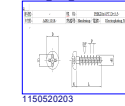
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mSAS\_HD0\_2

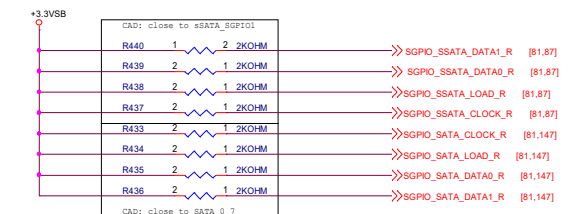
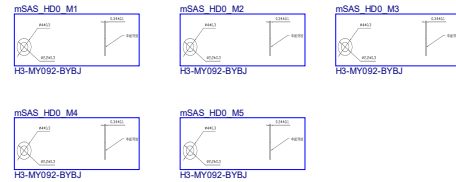


mSAS\_HD0\_3



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BOM: 螺絲改為13G024071020AK

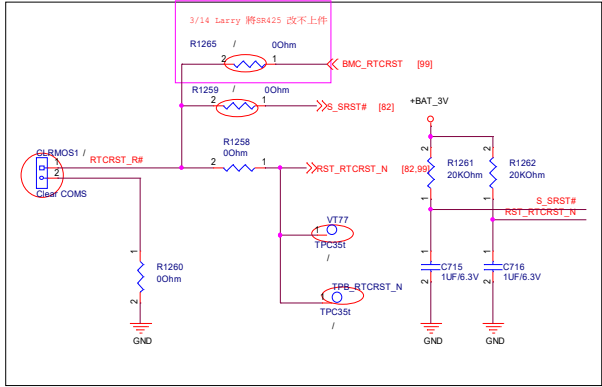
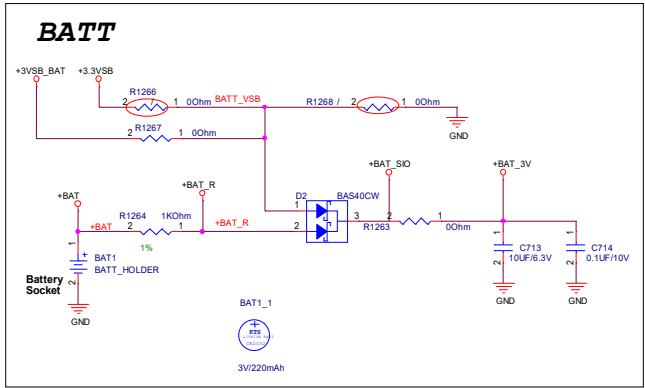


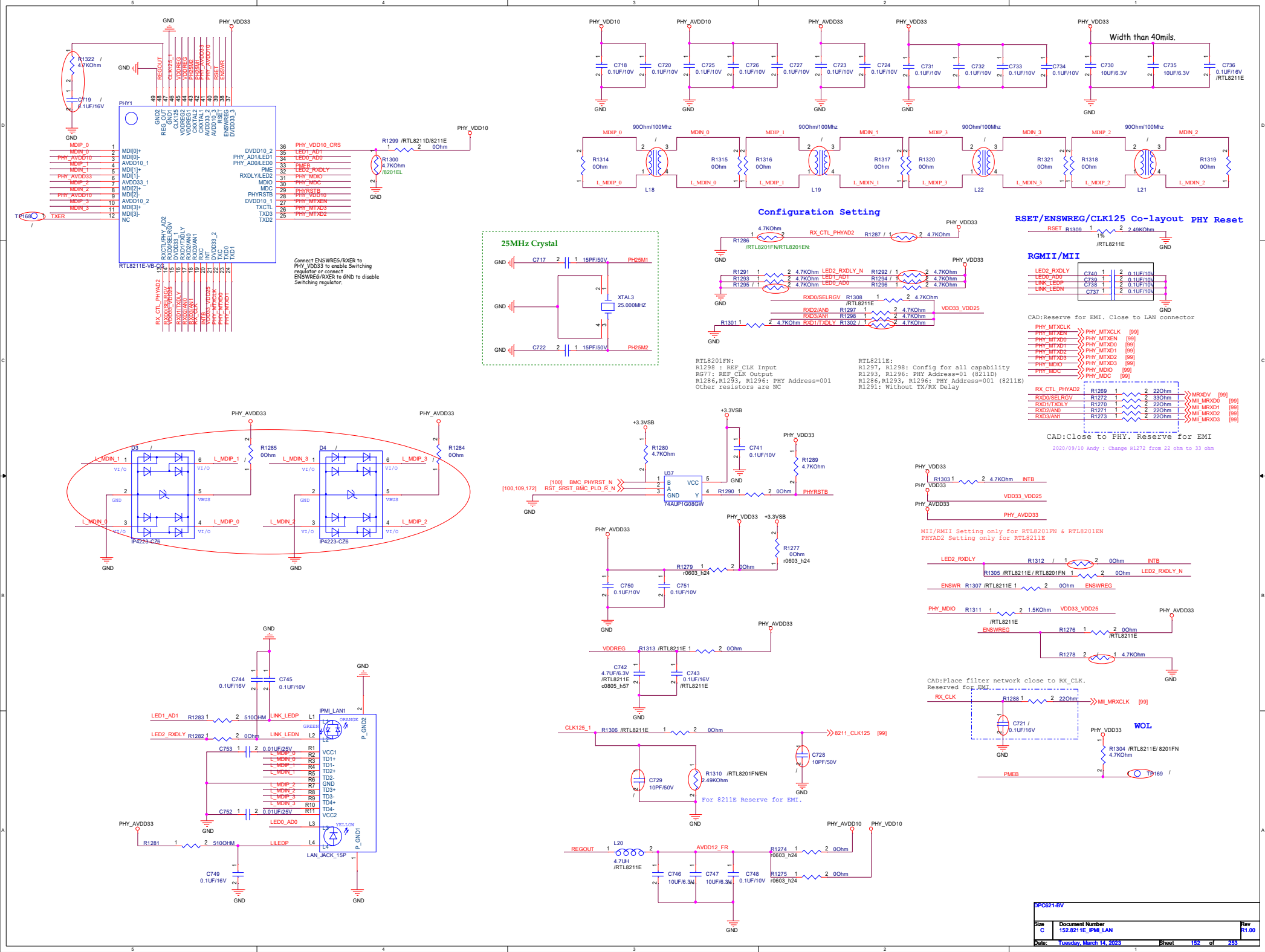
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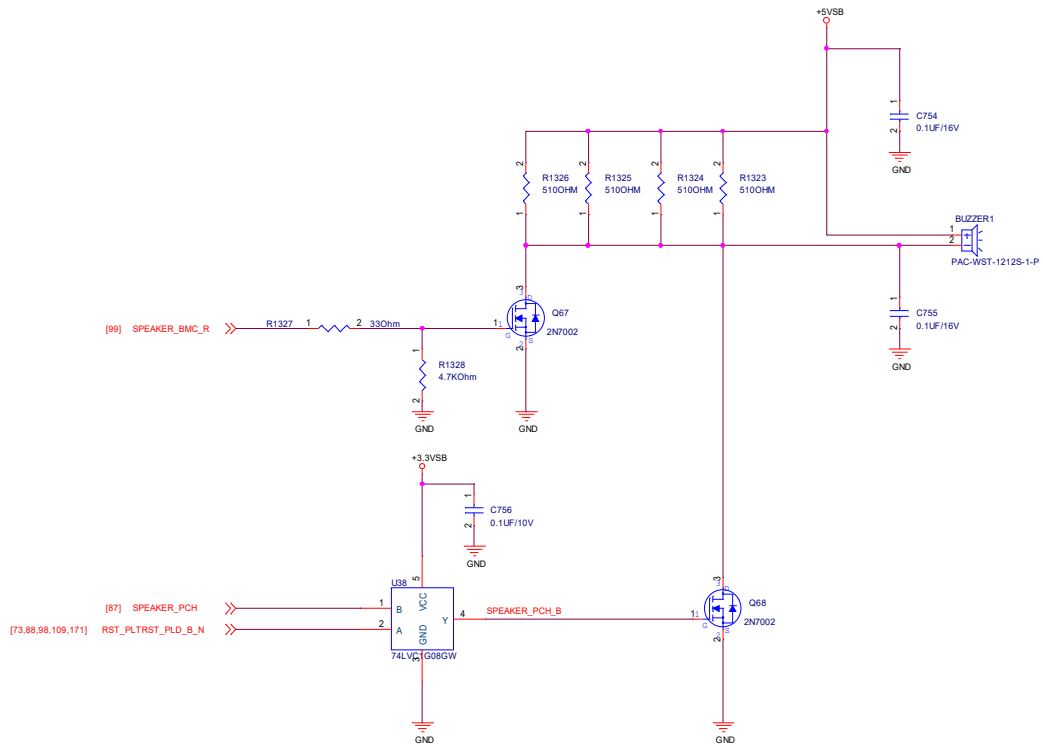
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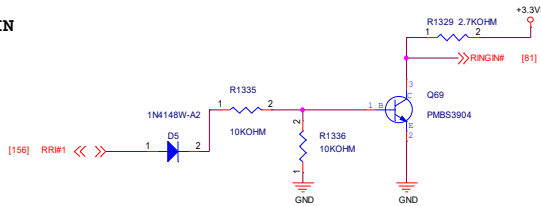
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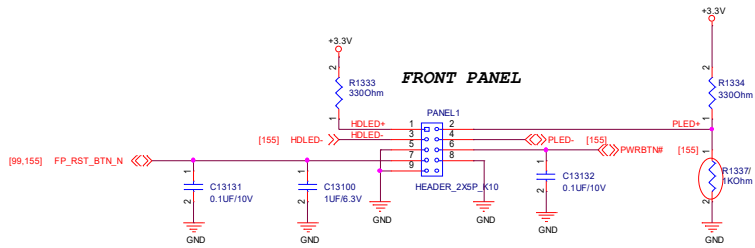




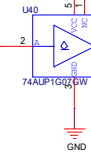
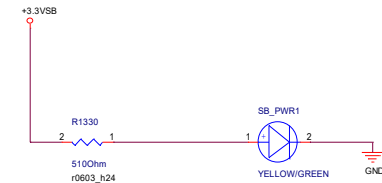
# RING\_IN



## FRONT PANEL

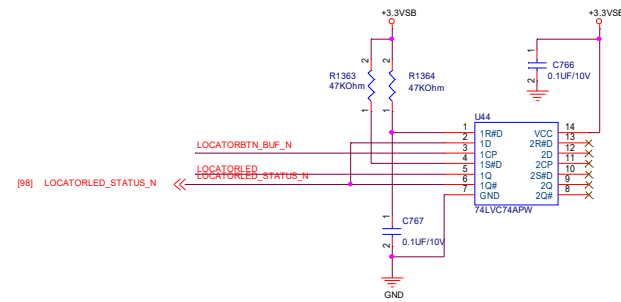
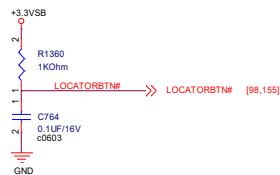
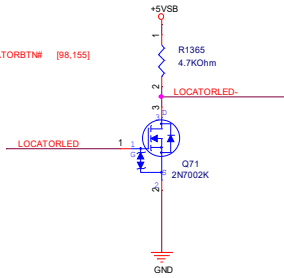
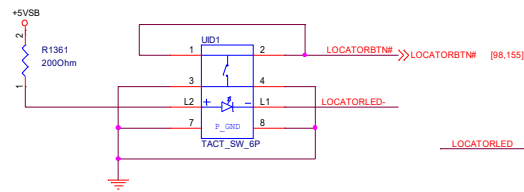
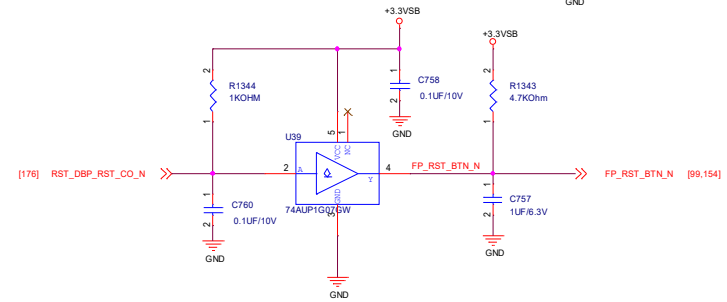
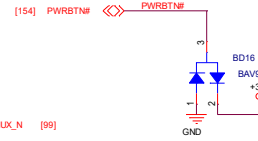
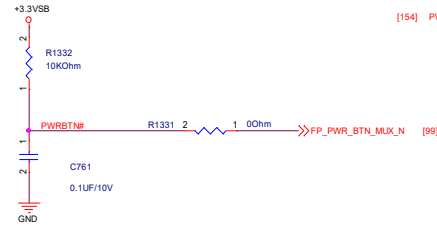
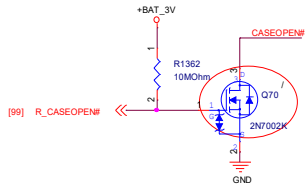
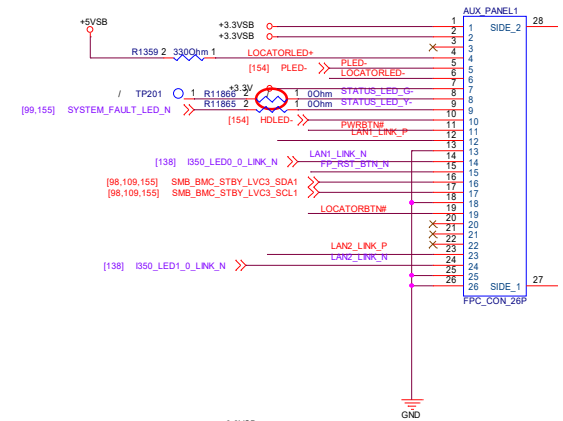
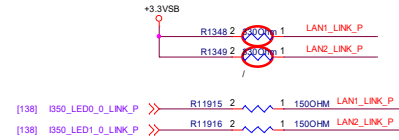
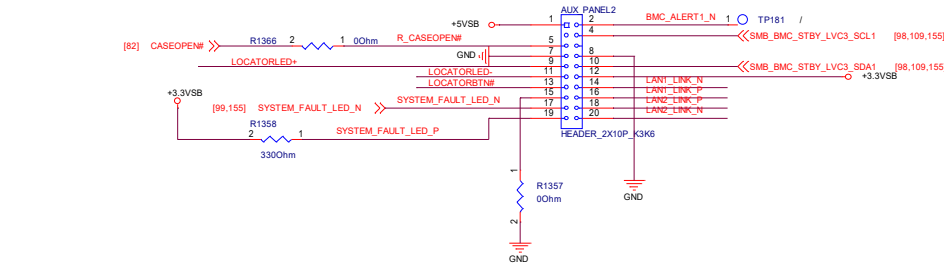


## 3V Standby Power Led

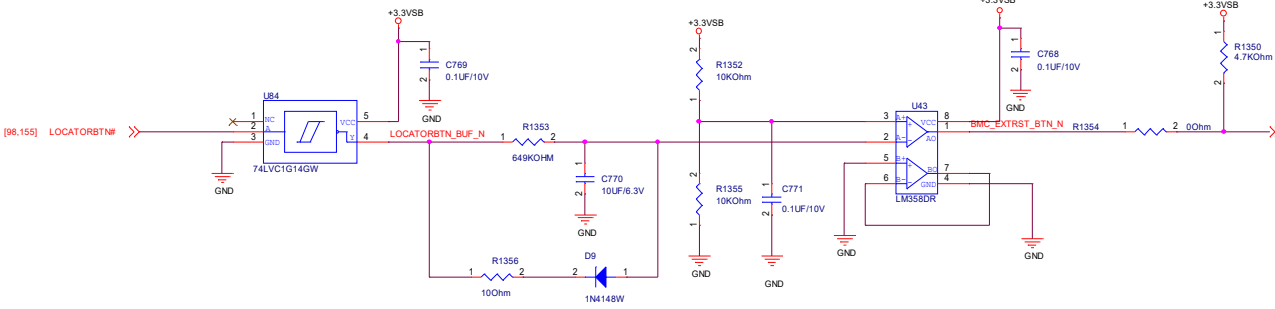


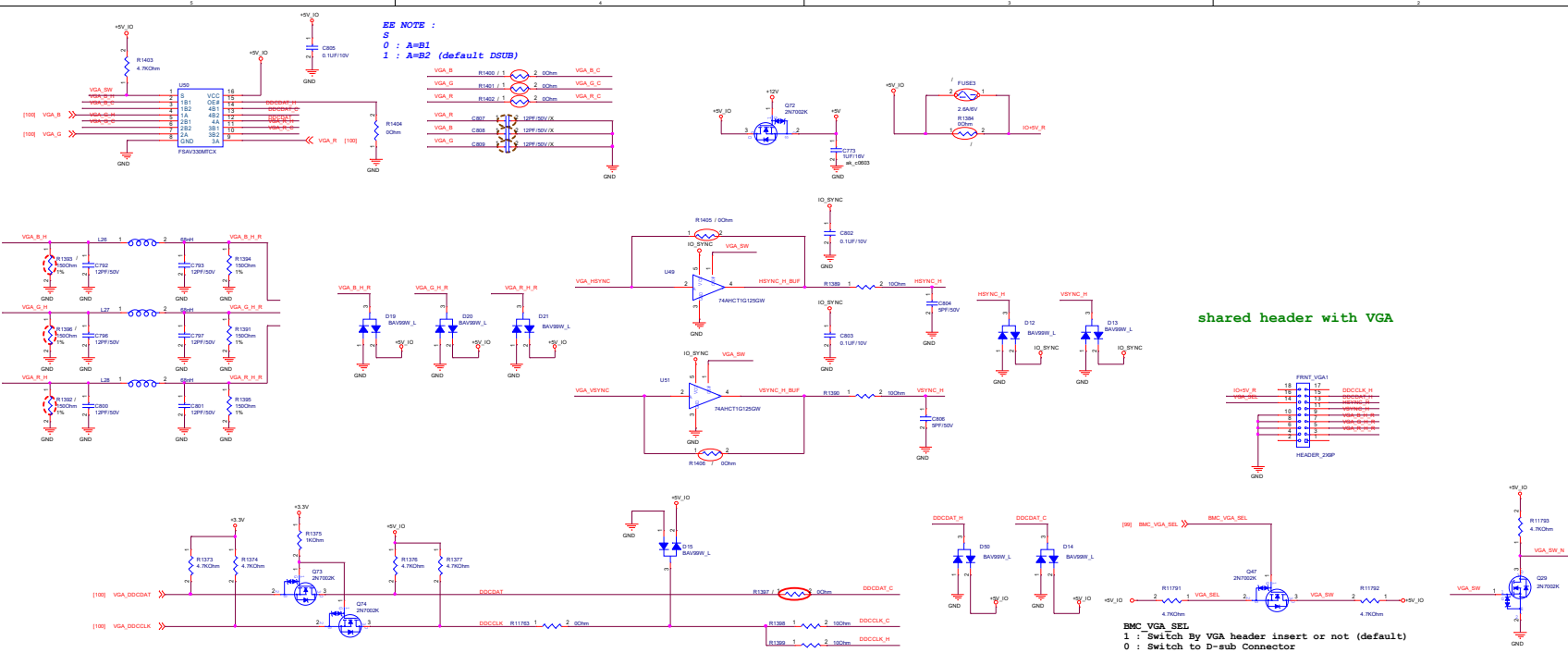
JPC0821-3V

# AUX\_PANEL



## 4s Override for BMC reset

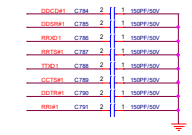
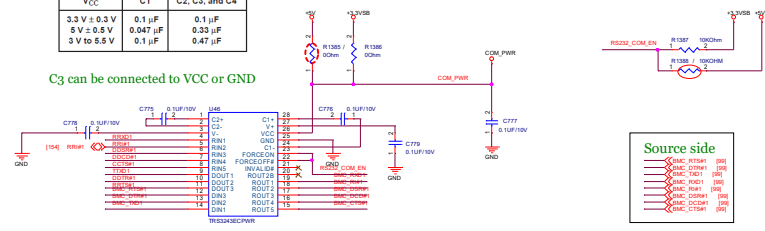




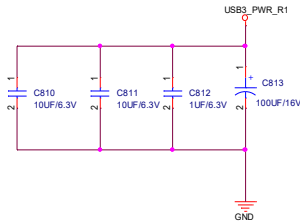
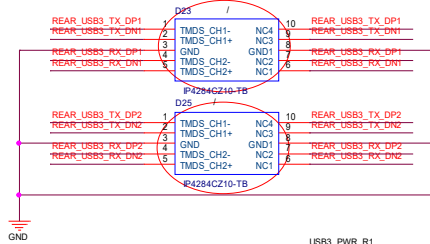
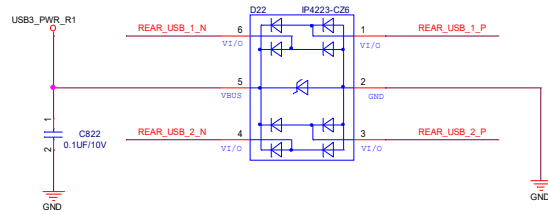
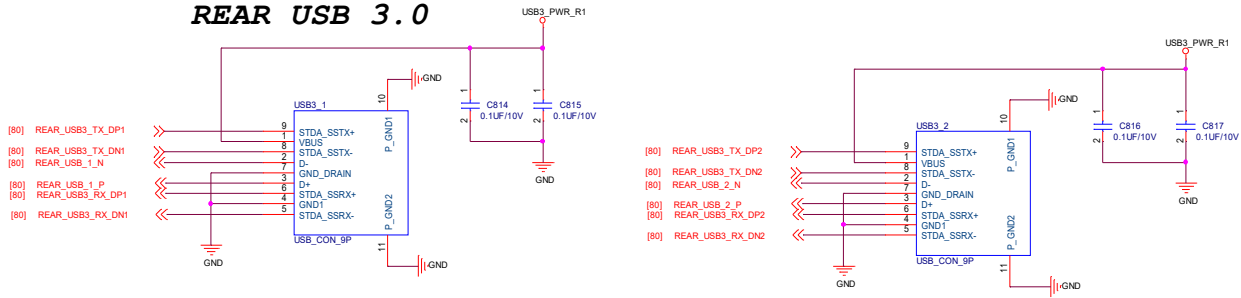
## COM Port

V <sub>CC</sub> vs CAPACITOR VALUES			
V <sub>CC</sub>	C1	C2, C3, and C4	
3.3 V ± 0.3 V	0.1 µF	0.1 µF	
5 V ± 0.5 V	0.047 µF	0.33 µF	
5 V to 5.5 V	0.1 µF	0.47 µF	

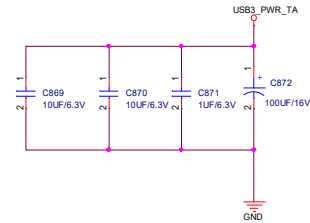
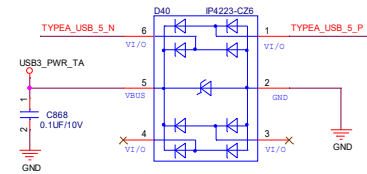
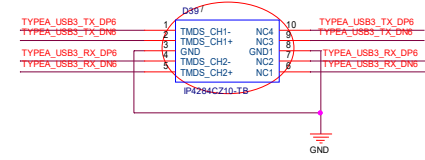
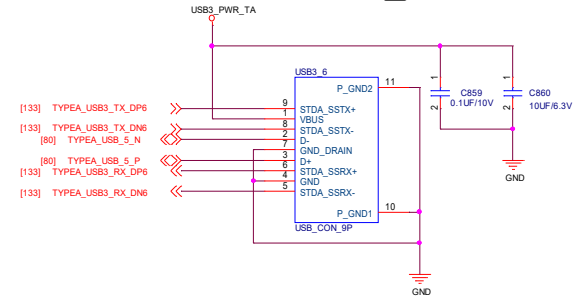
C3 can be connected to VCC or GND



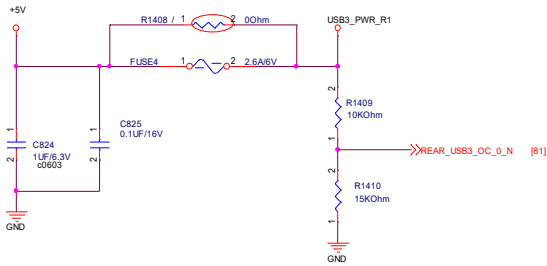
## REAR USB 3.0



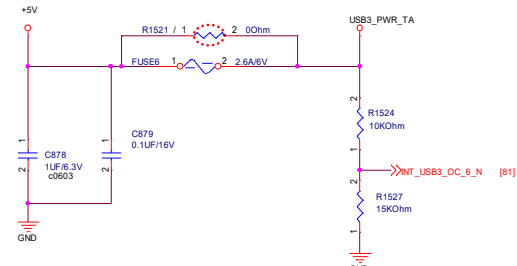
## USB 3.0 TYPE\_A



### REAR USB 3.0\*2 Power

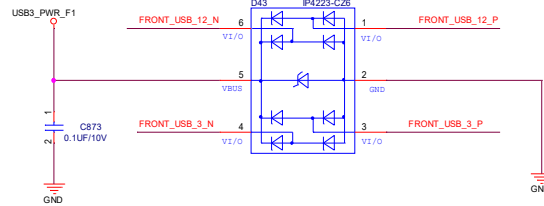
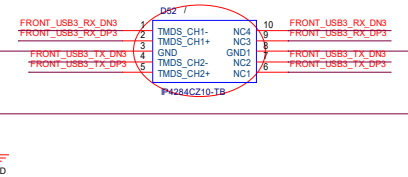
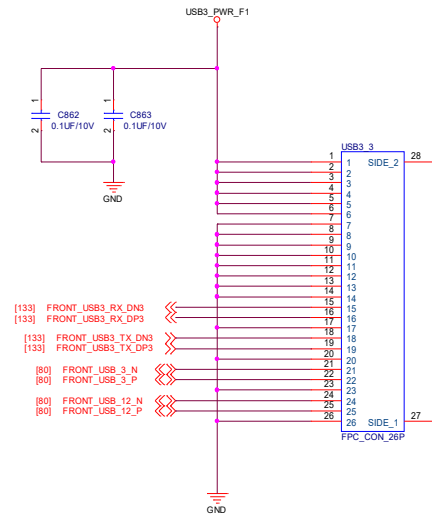


### REAR Type A USB 3.0\*1 Power

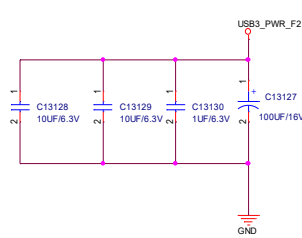
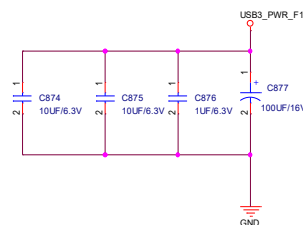
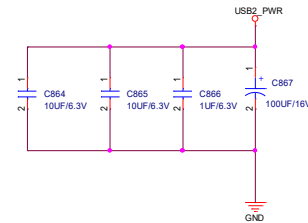
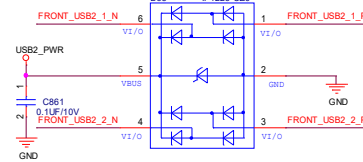
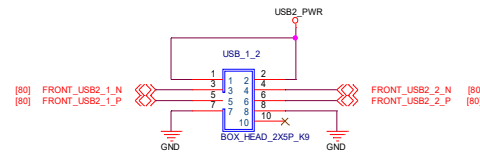


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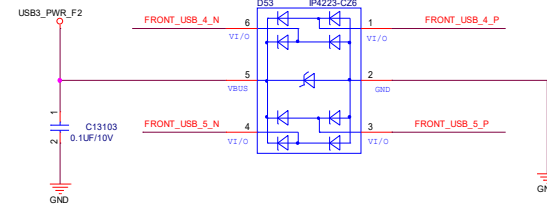
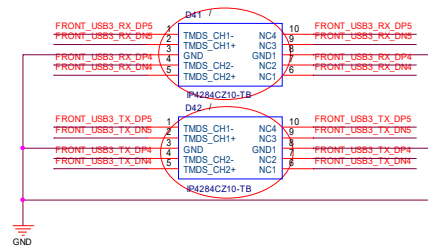
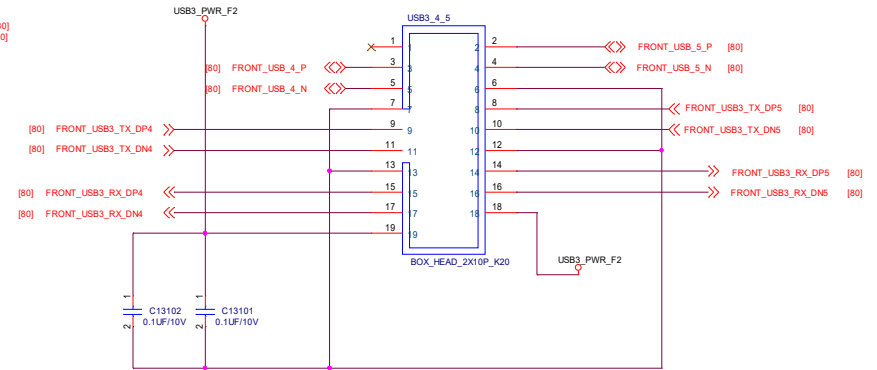
## FRONT USB 3.0 FFC



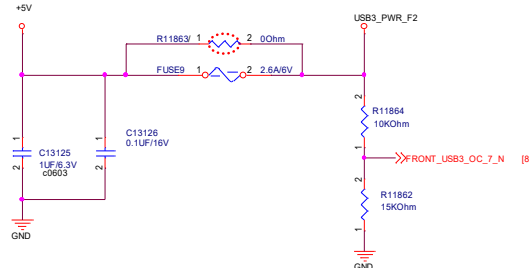
## FRONT USB 2.0 HEADER



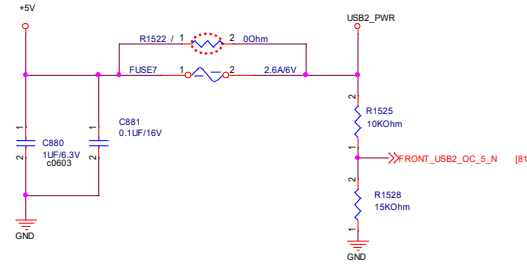
## FRONT USB 3.0 HEADER



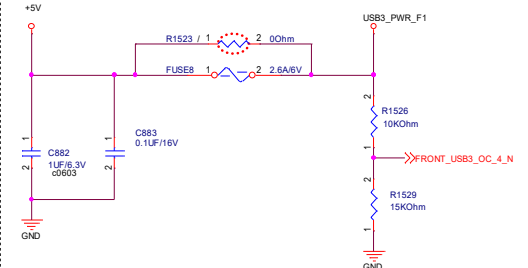
### FRONT USB 3.0\*2 Power



### FRONT USB 2.0\*2 Power

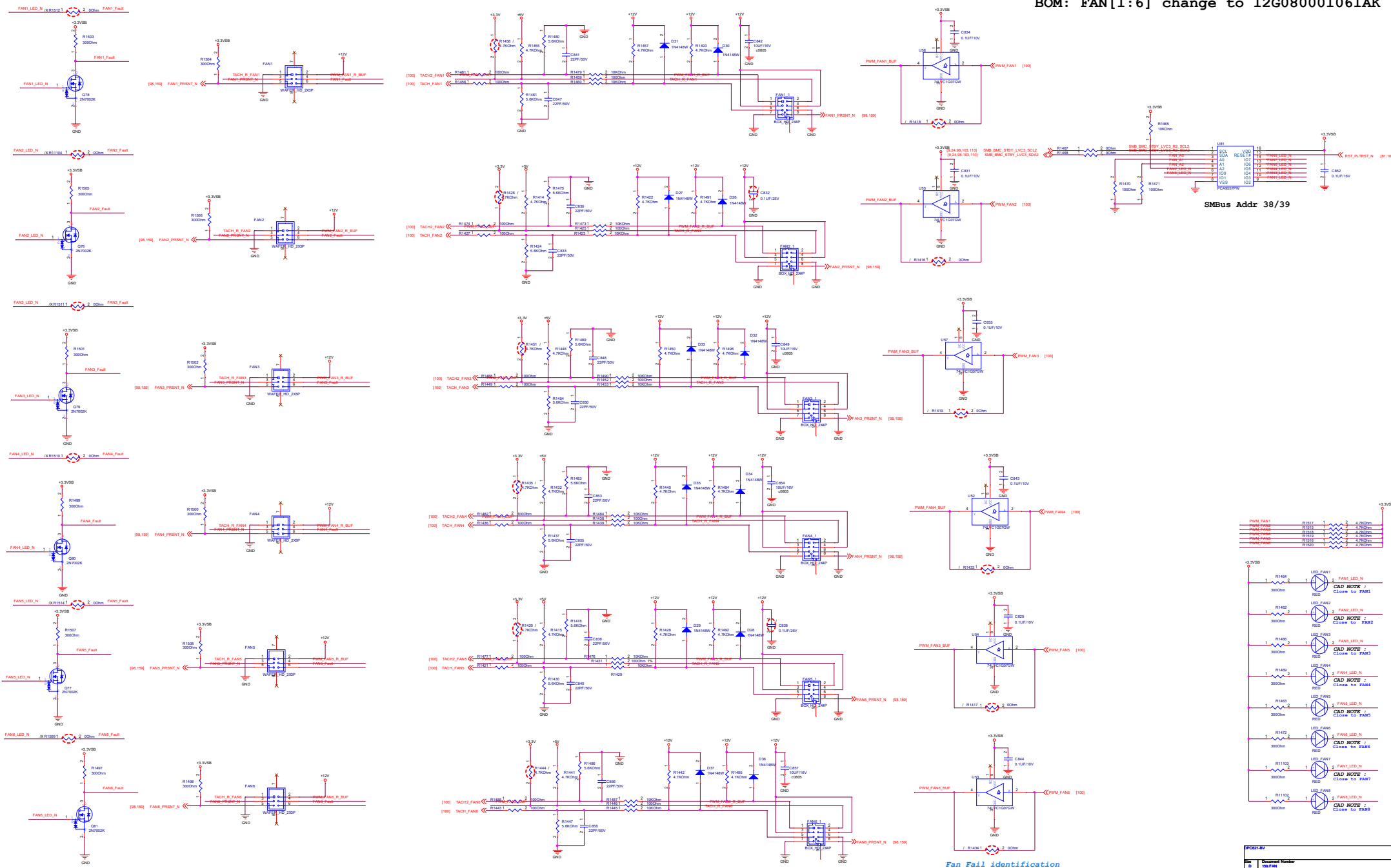


### FRONT USB 3.0\*2 Power



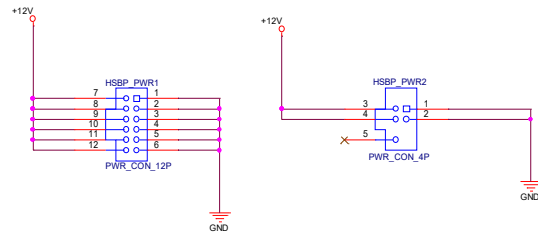
IPC021-3V

BOM: FAN[1:6] change to 12G080001061AK

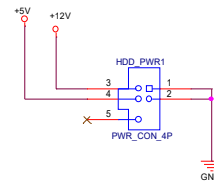




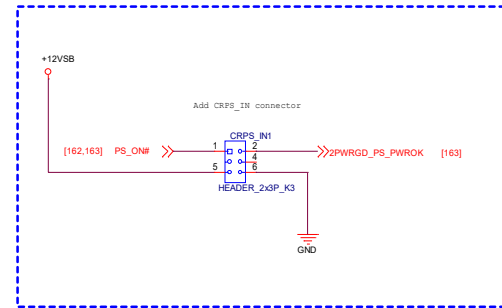
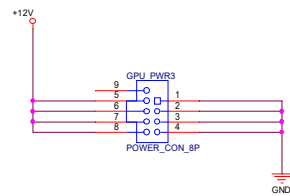
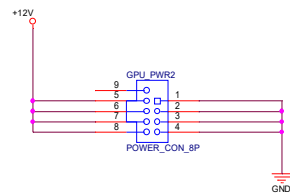
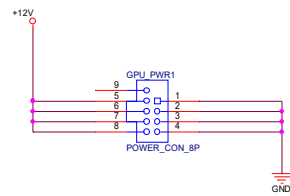
### HSBP Power Connector



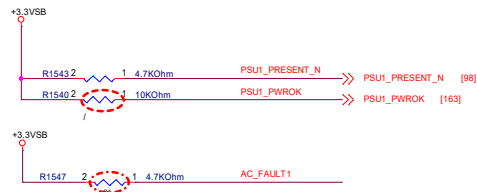
### HDD Power Connector



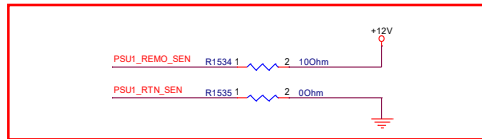
### GPGPU Power Connector







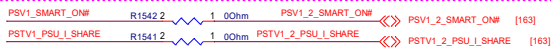
PSU1 Slave Address: 1011000X (B0/B1)



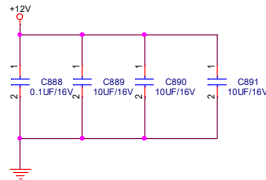
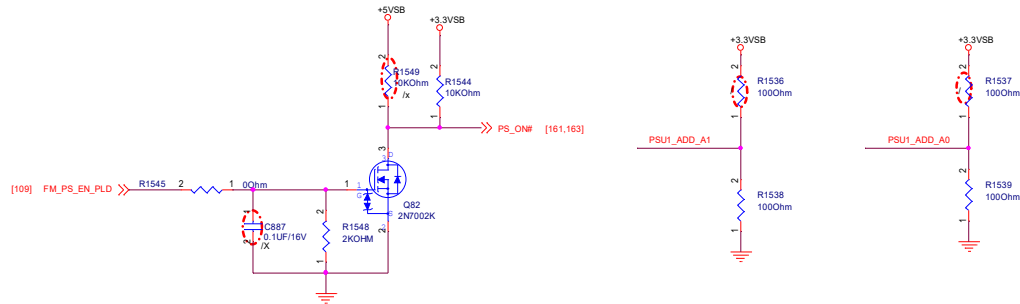
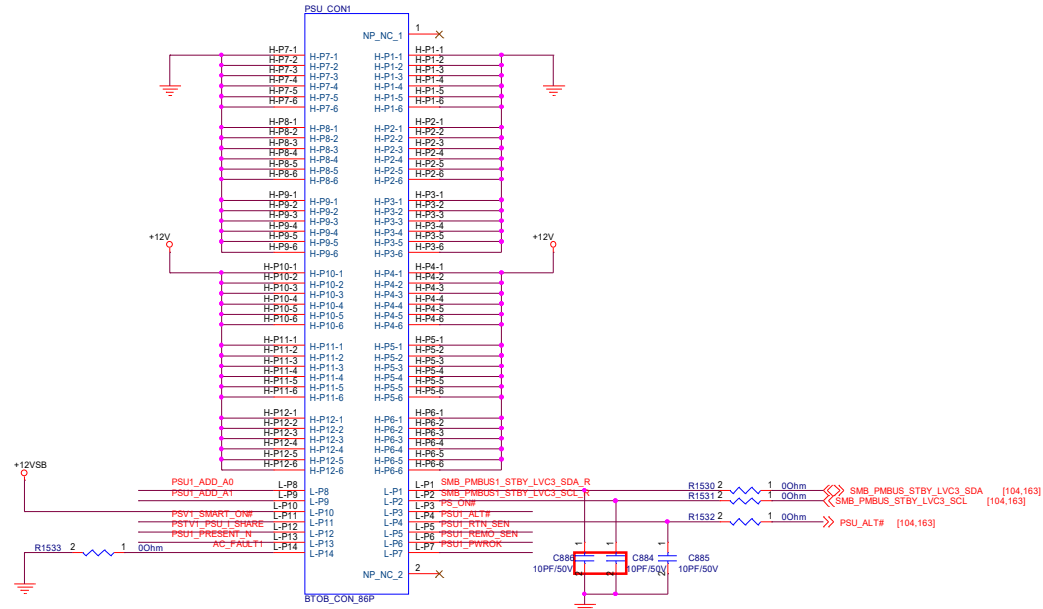
[CAD] Sense point close to PWR CONN

[Note] internal and external Remote sense resistor's ratio is 7:3, RTN\_SEN connect to connector GND

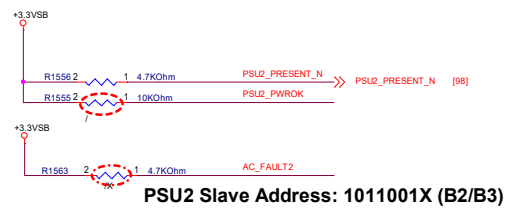
[Note] CRPS PSU spec suggest



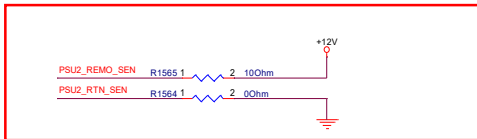
PSU1-2 Smart on connect together  
PSU1-2 I-Share connect together



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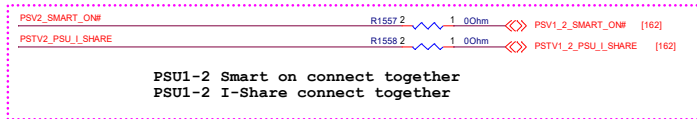


**PSU2 Slave Address: 1011001X (B2/B3)**



**[CAD] Sense point close to PWR CONN**  
**[Note] internal and external Remote sense resistor 's ratio is 7:3, RTN\_SEN connect to connector GND**

**[Note] CRPS PSU spec suggest**



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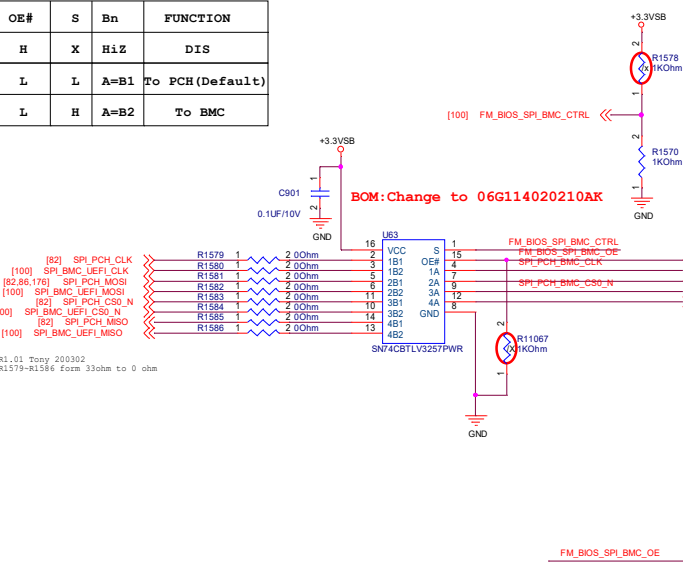
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===PFR\_Flash===

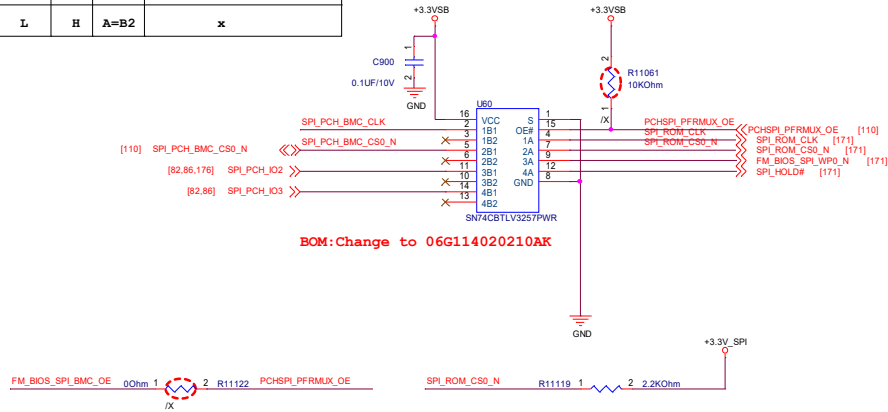
OE#	S	Bn	FUNCTION
H	X	HiZ	DIS
L	L	A=B1	To PCH(Default)
L	H	A=B2	To BMC



[82]	SPI_PCH_CLK	R1579	1	2	0Ohm
[100]	SPI_BMC_UFI_CLK	R1580	1	2	0Ohm
[82,86,176]	SPI_PCH_MOSI	R1581	1	2	0Ohm
[100]	SPI_BMC_UFI_MOSI	R1582	1	2	0Ohm
[82]	SPI_PCH_CS0_N	R1583	1	2	0Ohm
[100]	SPI_BMC_UFI_CS0_N	R1584	1	2	0Ohm
[82]	SPI_PCH_MISO	R1585	1	2	0Ohm
[100]	SPI_BMC_UFI_MISO	R1586	1	2	0Ohm

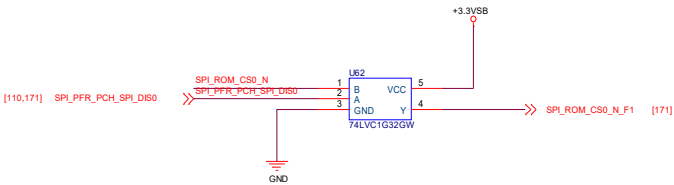
R1.01 Tony 200302  
R1579~R1586 form 33ohm to 0 ohm

OE#	S	Bn	FUNCTION
H	X	HiZ	DIS
L	L	A=B1	To MUX(U40 ())Default)
L	H	A=B2	x

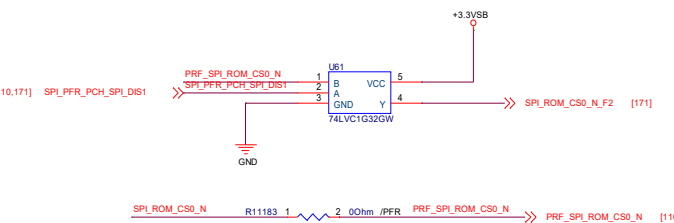


[110]	SPI_PCH_BMC_CS0_N	R11122	1	2	0Ohm
[82,86,176]	SPI_PCH_MOSI	R11123	1	2	0Ohm
[82,86]	SPI_PCH_CS0_N	R11124	1	2	0Ohm
[82,86]	SPI_PCH_MISO	R11125	1	2	0Ohm

BOM:Change to 06G114020210AK



[110,171]	SPI_PFR_PCH_SPI_DS0	R11122	1	2	0Ohm
[110,171]	SPI_PFR_PCH_SPI_DS1	R11123	1	2	0Ohm
[110,171]	SPI_PFR_PCH_SPI_DS2	R11124	1	2	0Ohm
[110,171]	SPI_PFR_PCH_SPI_DS3	R11125	1	2	0Ohm



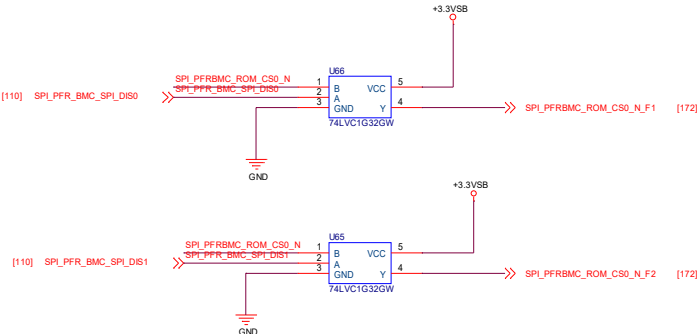
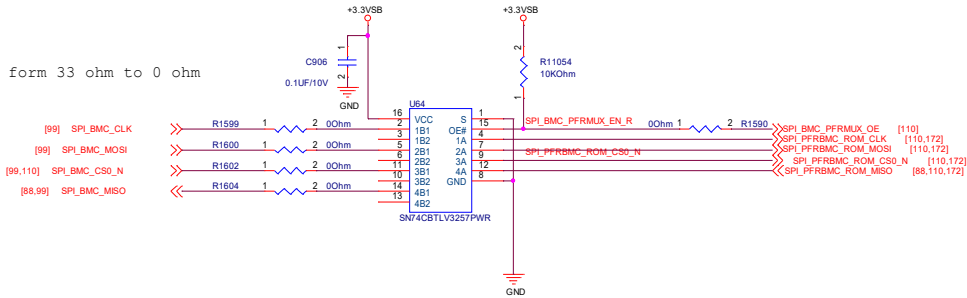
[110,171]	SPI_PFR_PCH_SPI_DS1	R11122	1	2	0Ohm
[110,171]	SPI_PFR_PCH_SPI_DS2	R11123	1	2	0Ohm
[110,171]	SPI_PFR_PCH_SPI_DS3	R11124	1	2	0Ohm
[110,171]	SPI_PFR_PCH_SPI_DS4	R11125	1	2	0Ohm

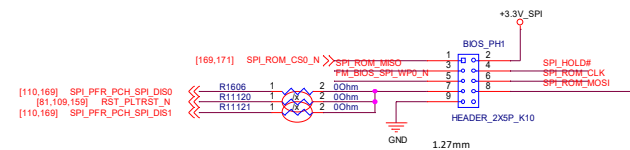
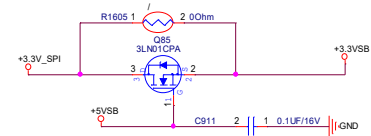
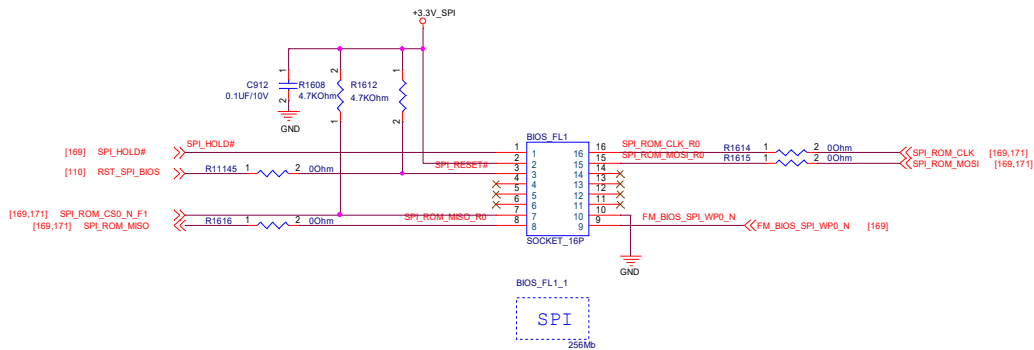
R1.01 Tony 200302  
新增&修改 BIOS SPI線路



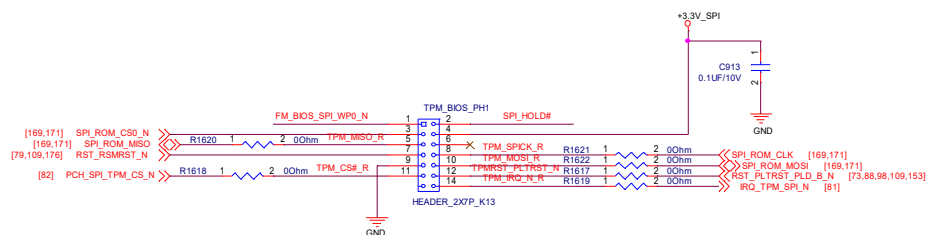
R1.01 Tony 200207  
Change BMC SPI damping form 33 ohm to 0 ohm

BOM:Change to 06G114020210AK





R1.01 Tony 200324  
Change BIOS\_PH1 from DIP to SMT



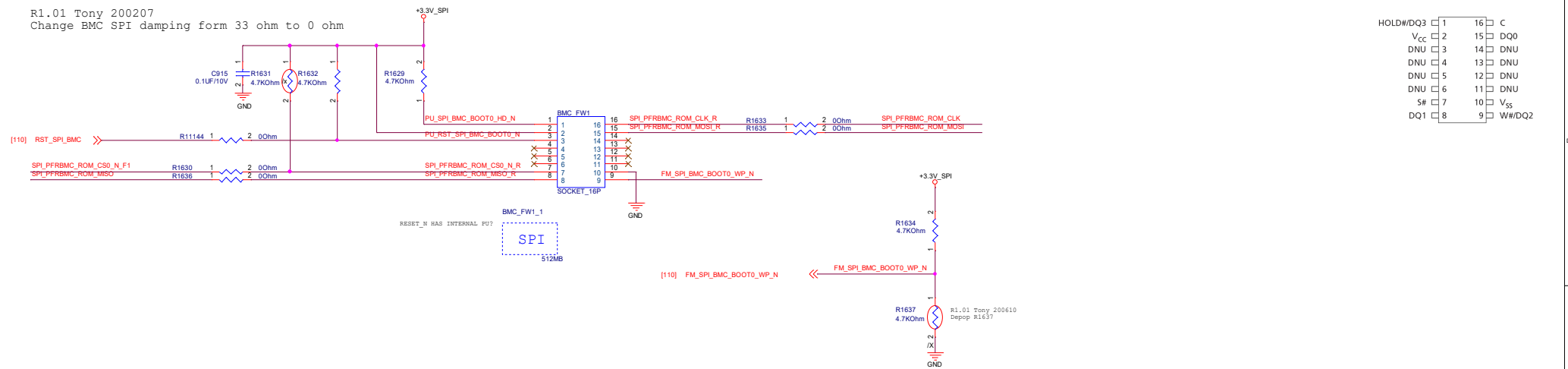
SPI\_ROM\_CS0\_N\_F2  
SPI\_ROM\_CS0\_N\_F1



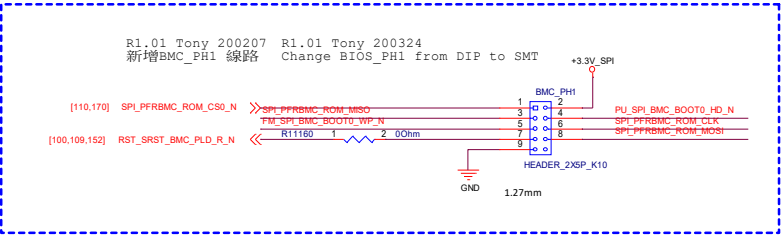
XP0281-3V

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C	171.BIOS_Flash	R1.00
Date:	Tuesday, March 14, 2023	Sheet 171 of 253

R1.01 Tony 200207  
Change BMC SPI damping form 33 ohm to 0 ohm

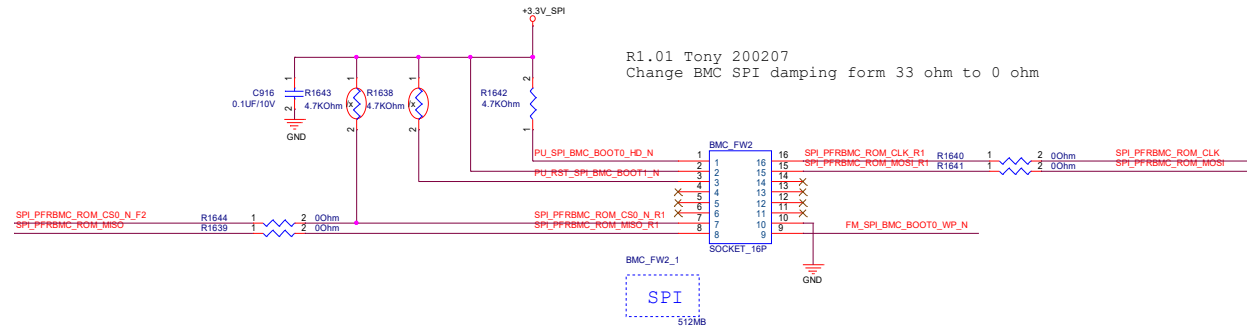


HOLD#/DQ3	1	16	C
V <sub>CC</sub>	2	15	DQ0
DNU	3	14	DNU
DNU	4	13	DNU
DNU	5	12	DNU
DNU	6	11	DNU
S#	7	10	V <sub>SS</sub>
DQ1	8	9	WW/DQ2



SPI\_PFRBMC\_ROM\_CLK << SPI\_PFRBMC\_ROM\_CLK [110,170]  
SPI\_PFRBMC\_ROM\_MOSI << SPI\_PFRBMC\_ROM\_MOSI [110,170]  
SPI\_PFRBMC\_ROM\_CS0\_N\_F1 << SPI\_PFRBMC\_ROM\_CS0\_N\_F1 [170]  
SPI\_PFRBMC\_ROM\_MISO << SPI\_PFRBMC\_ROM\_MISO [88,110,170]

SPI\_PFRBMC\_ROM\_CS0\_N\_F2 << SPI\_PFRBMC\_ROM\_CS0\_N\_F2 [170]



D

9

C

c

B

B

A

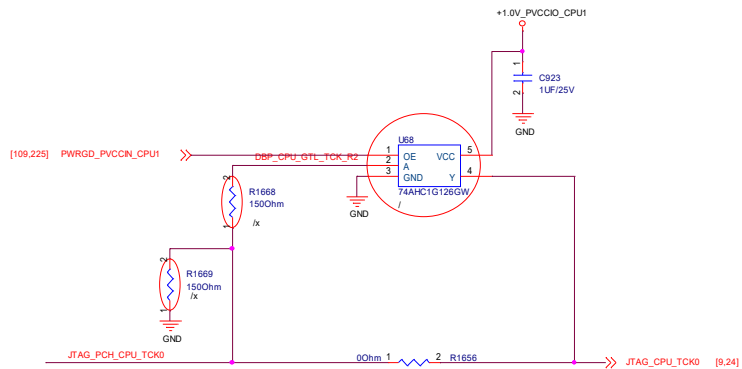
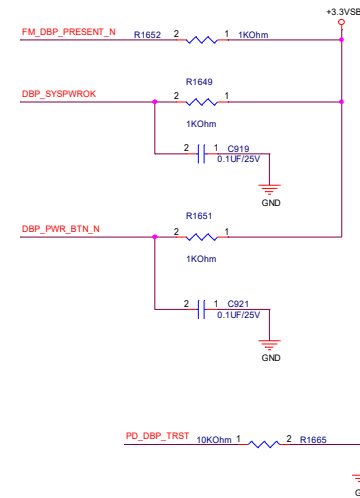
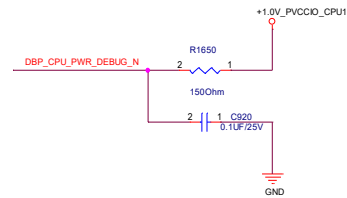
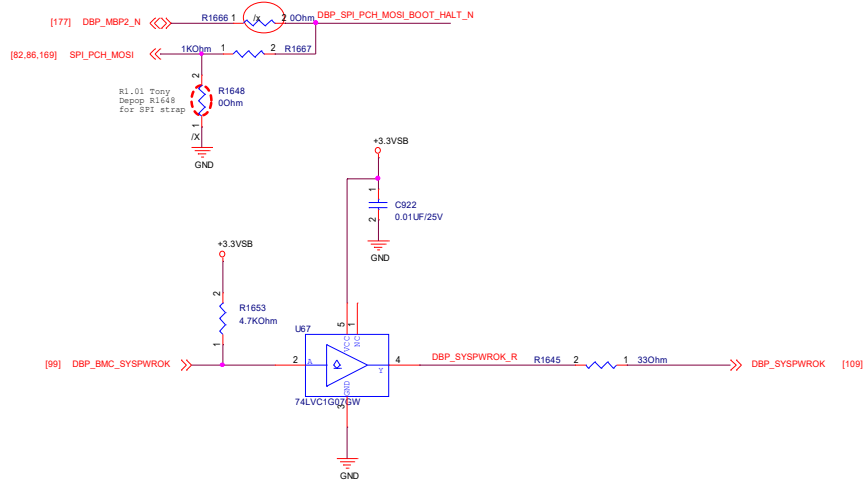
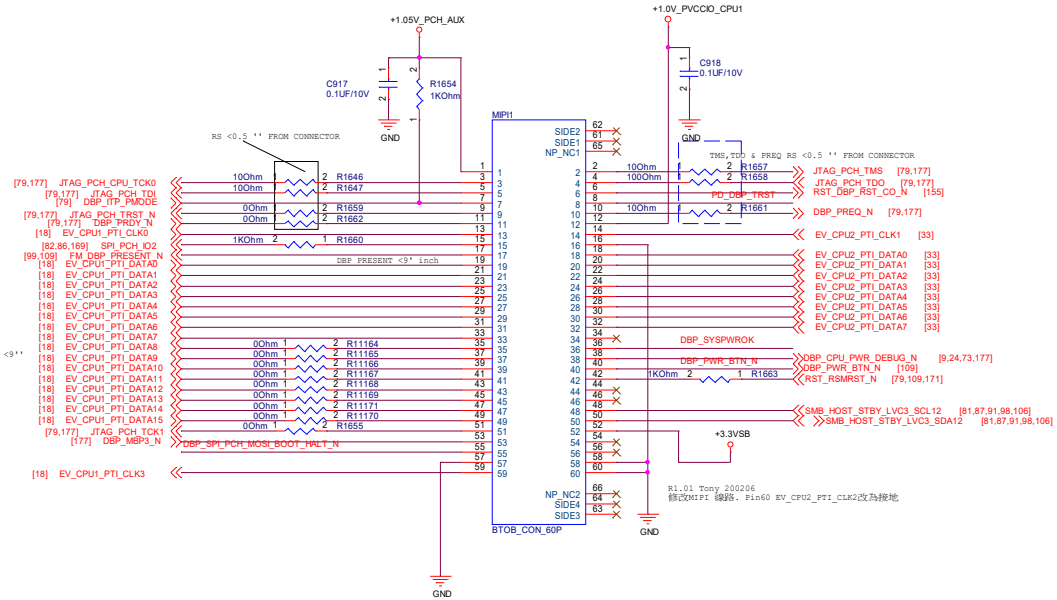
A

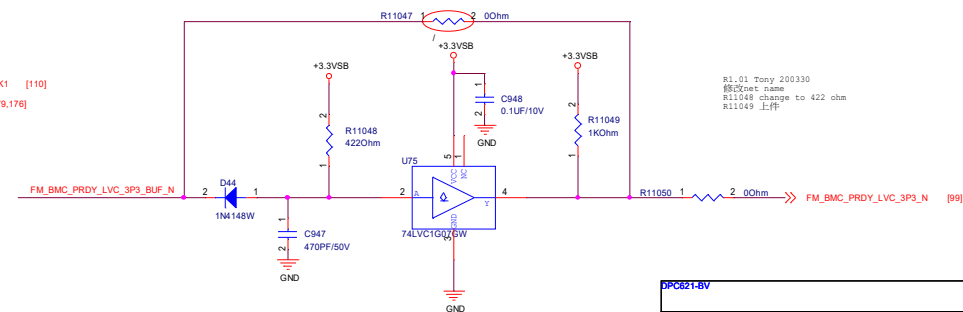
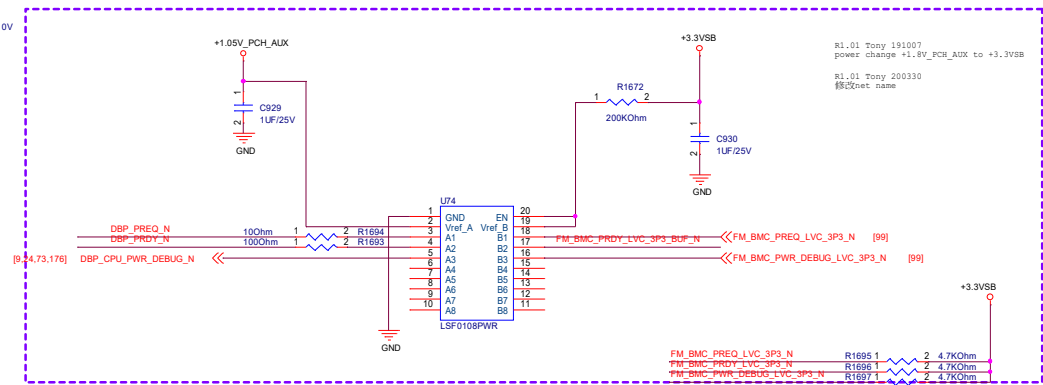
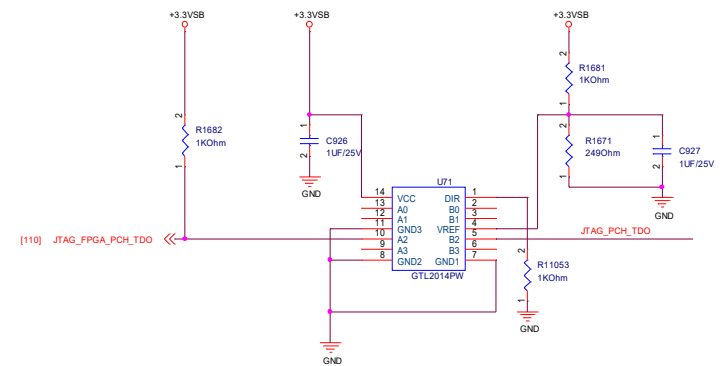
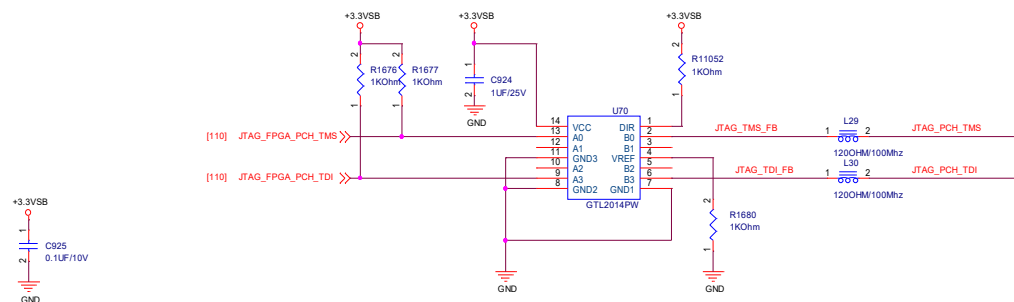
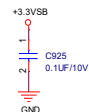
DPC821-BV			
Size C	Document Number 173.Blank	Rev R1.00	
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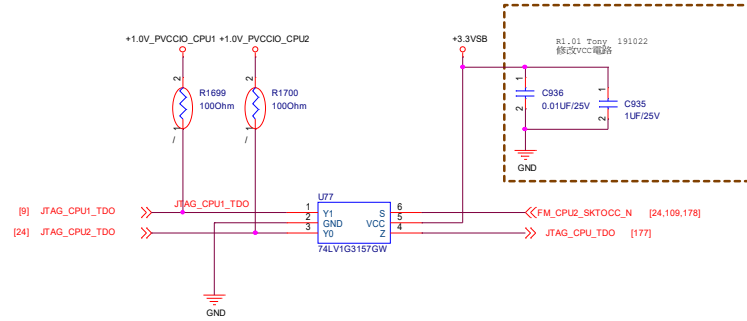
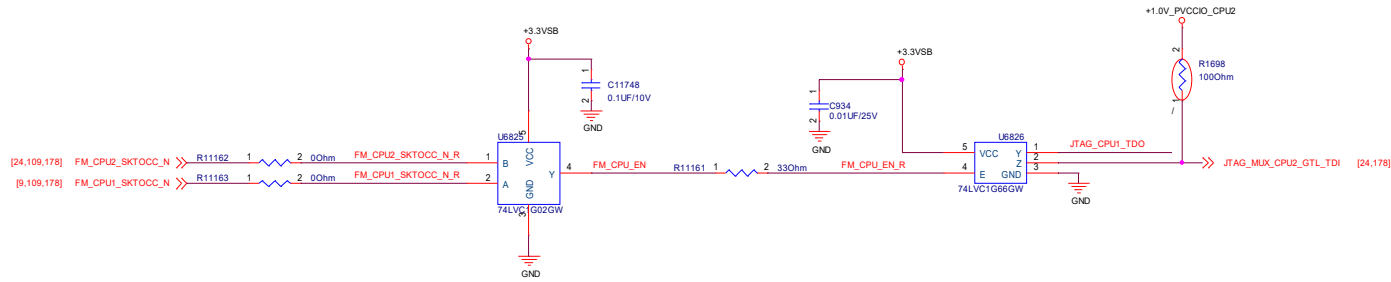
R1.01 Tony 200205  
修改MIPI 線路. 新增PTI\_DATA[8:15] to CPU



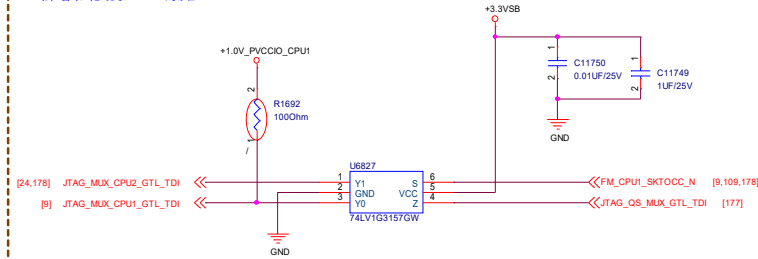




R1.01 Tony 200213  
新增和修改U76線路



R1.01 Tony 200213  
新增和修改U6827線路



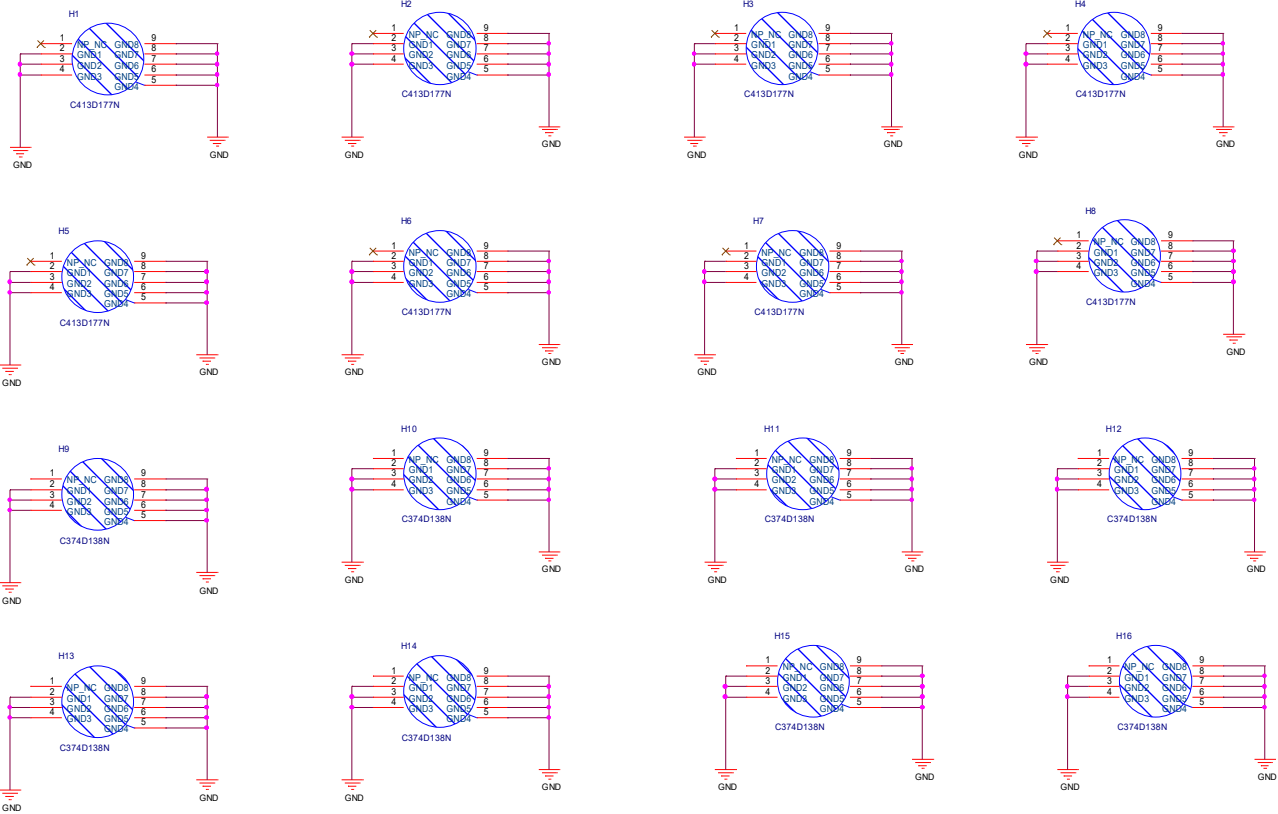
R1.01 Tony 200226  
刪除MIPI轉卡線路

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===CPU Sideband===

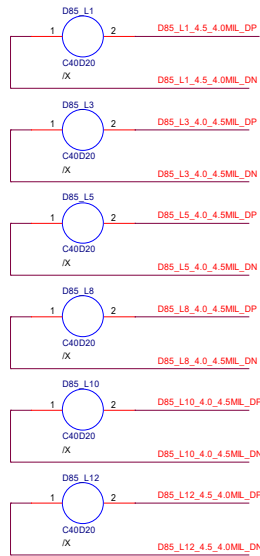
====SYS\_SIDE BAND====

SCREW\_HOLE

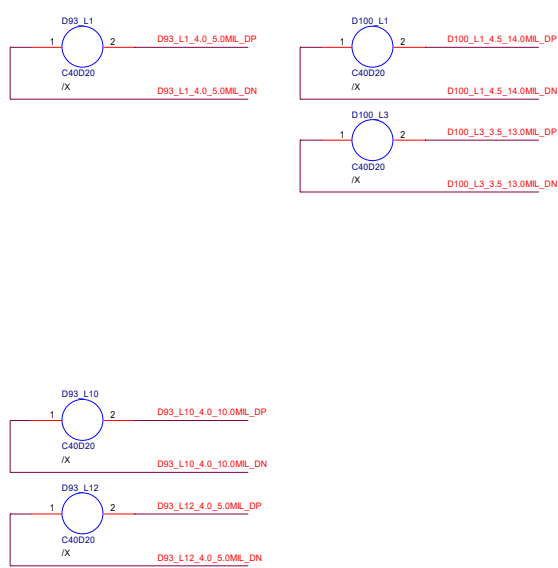


BOM CHANGE TO 13G074203000AK





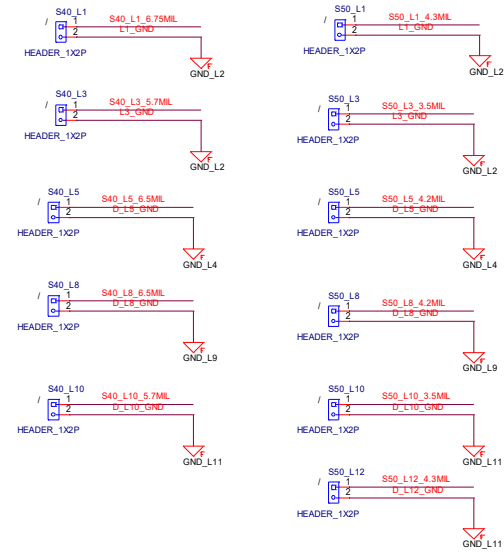
LAYER : 1/3/5/8/10/12  
IMPEDANCE : 85 OHM +/- 10%



LAYER : 1/10/12  
IMPEDANCE : 93 OHM +/- 10%

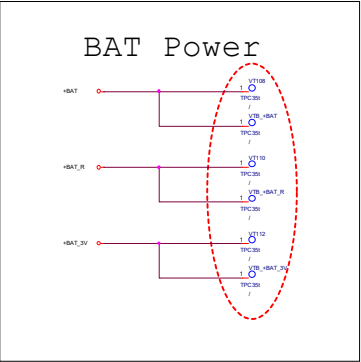
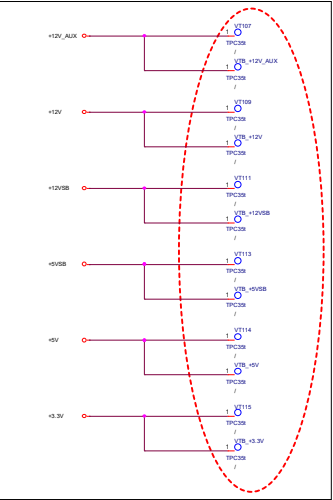
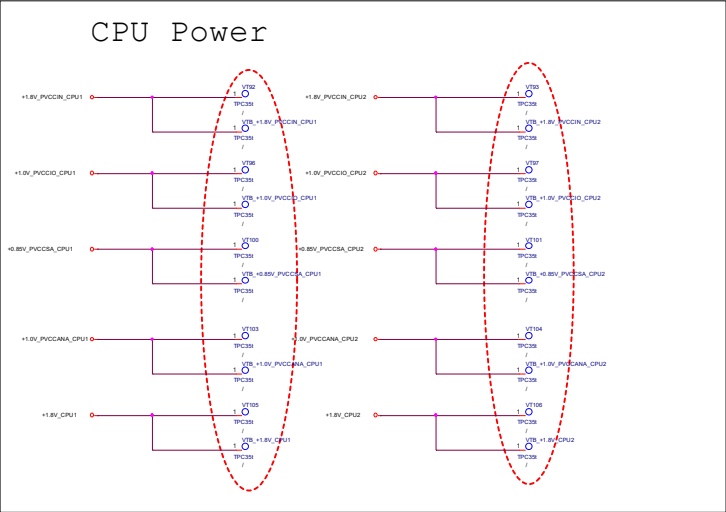
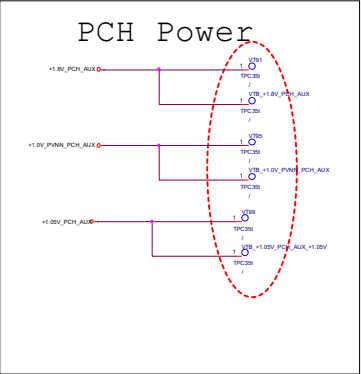
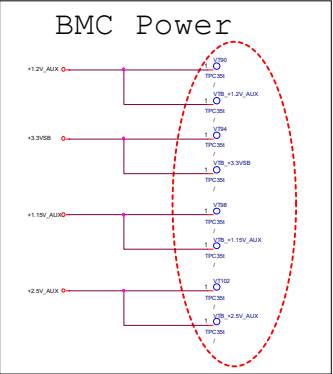
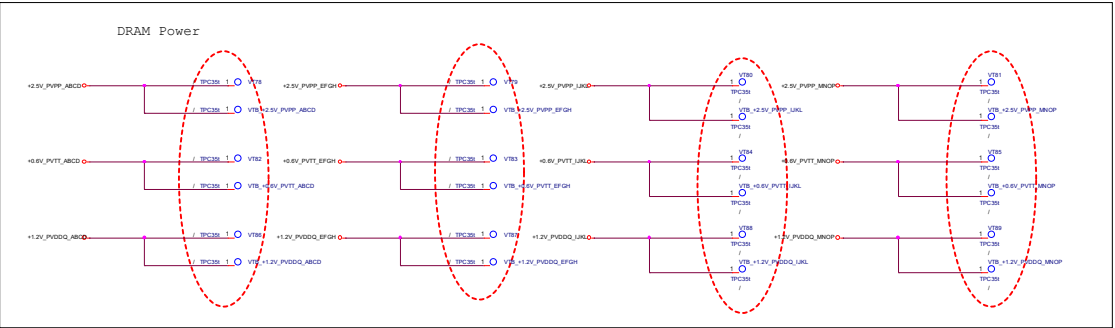
LAYER : 1/3  
IMPEDANCE : 100 OHM +/- 10%

## Single-End



LAYER : 1/3/5/8/10/12  
IMPEDANCE : 40 OHM +/- 10%

LAYER : 1/3/5/8/10/12  
IMPEDANCE : 50 OHM +/- 10%





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Rev		
	<RevCode>	

Rev

Document Number

<Doc>

Size

**A**

Date:

**Tuesday, March 14, 2023**

Sheet

194

of

253

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51

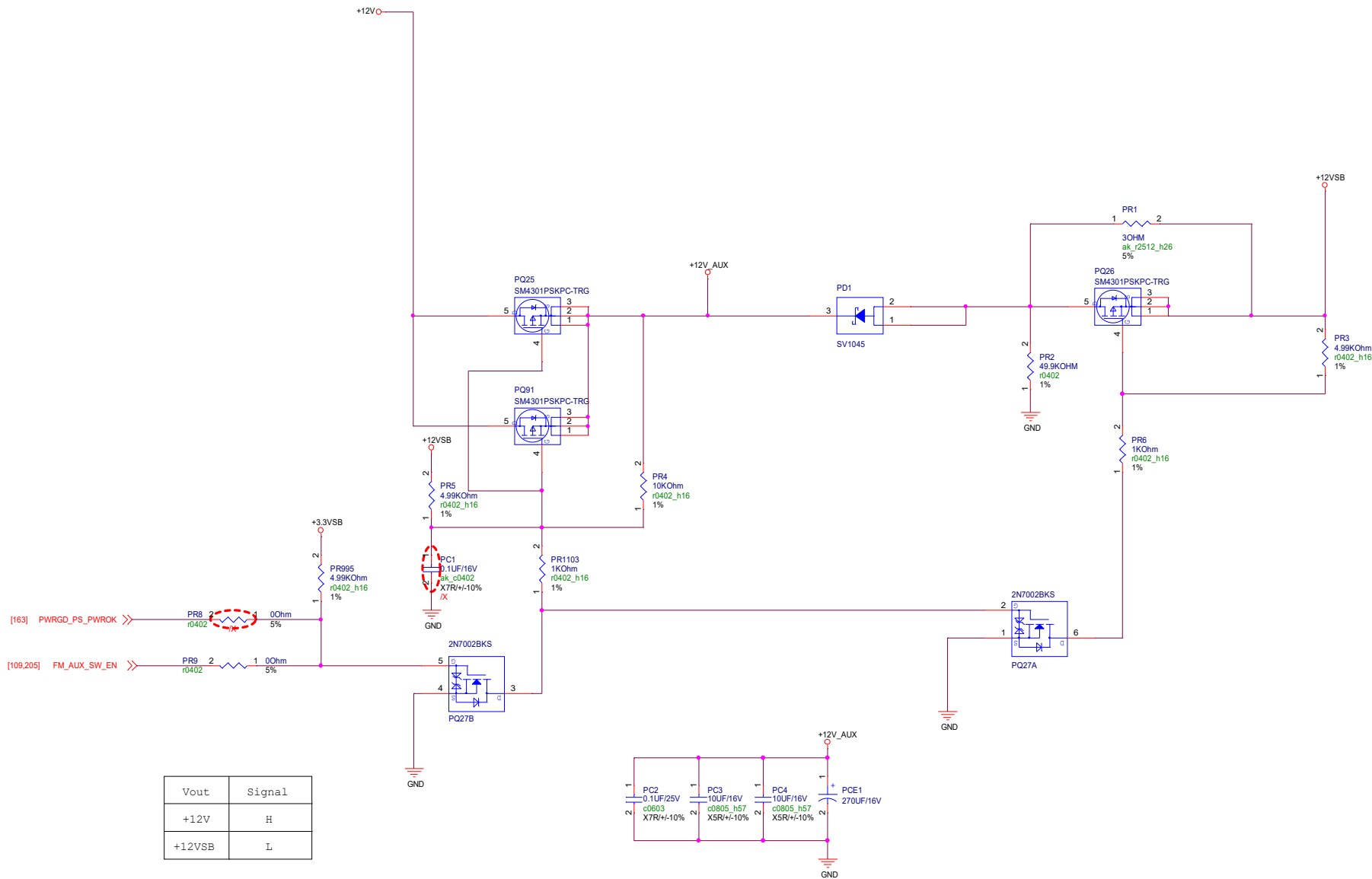
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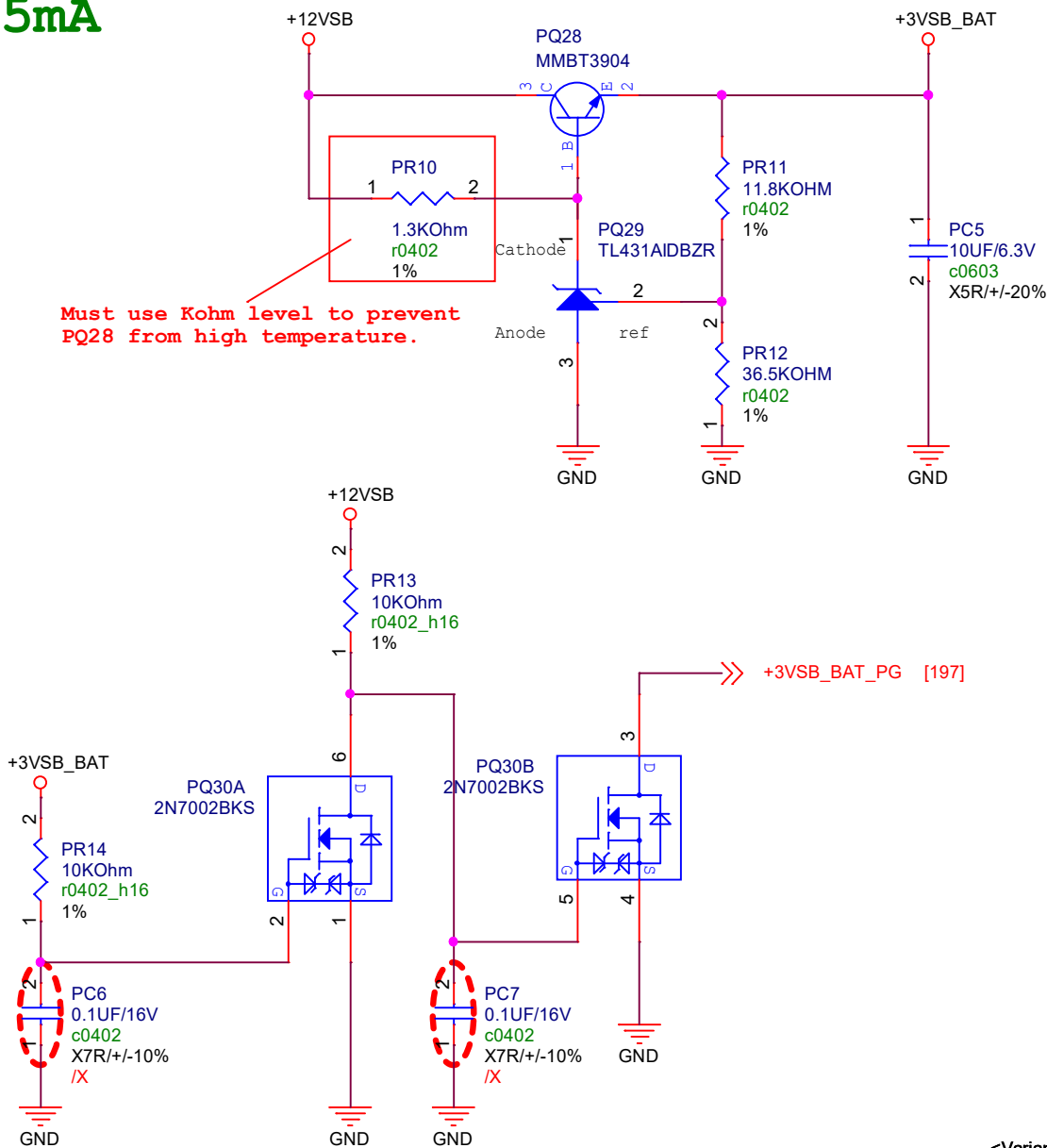
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A

+12V\_AUX

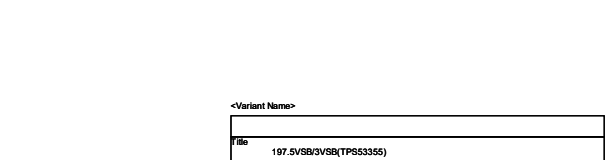
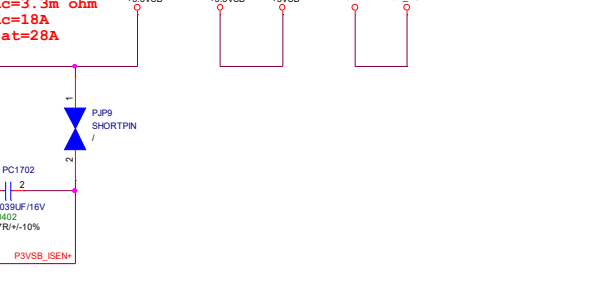
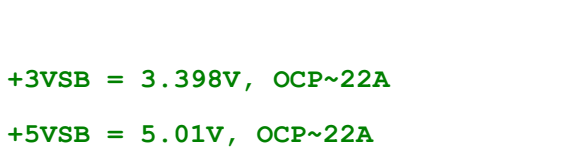
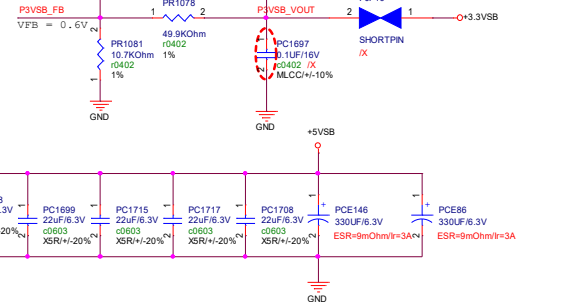
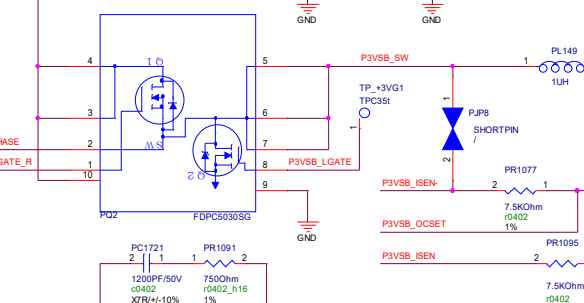
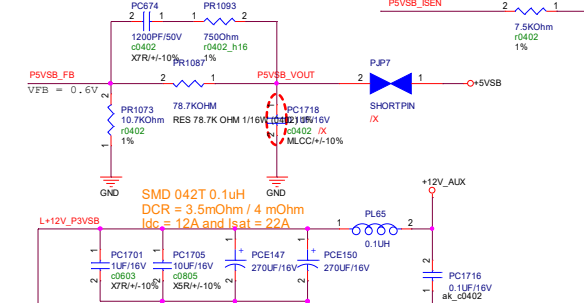
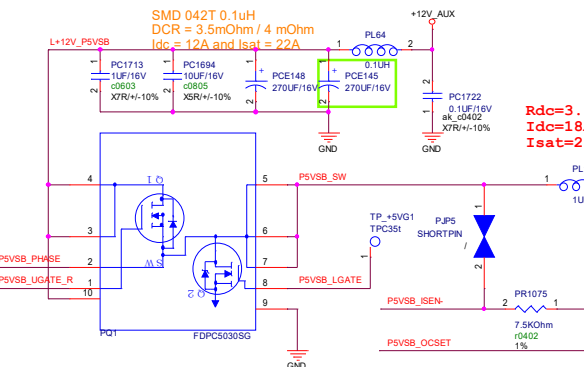
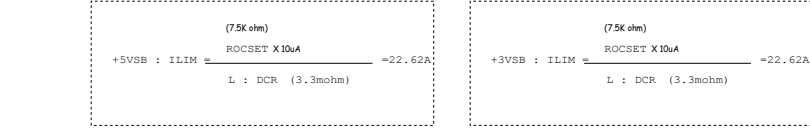
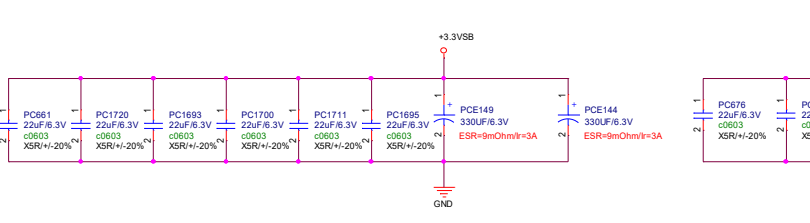
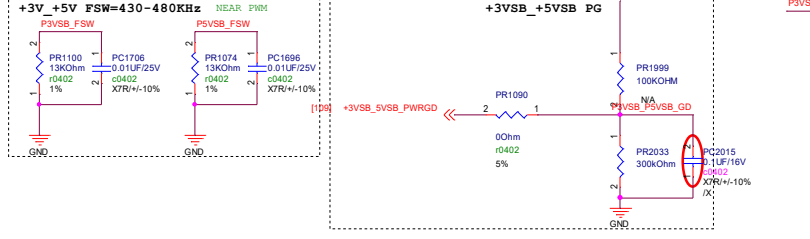
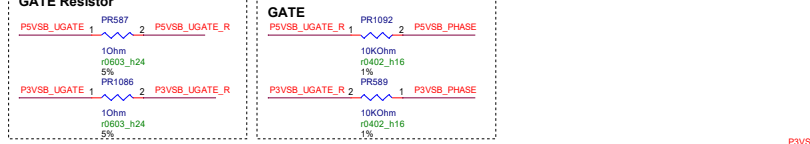
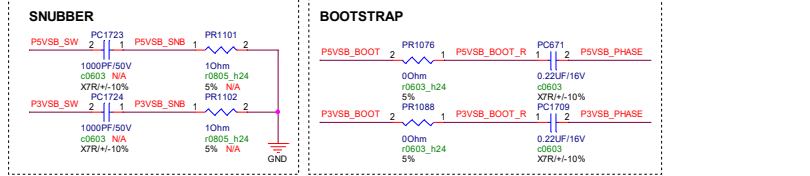
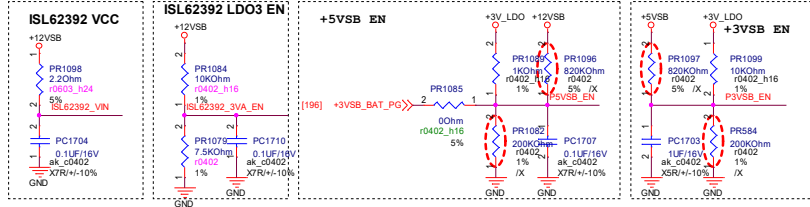
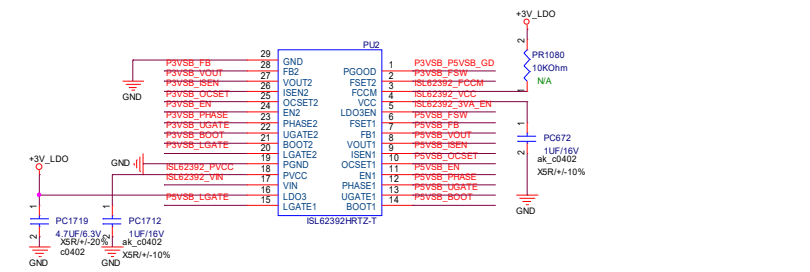


+3VSB BAT = 3.18V  
IMAX=5mA



<Variant Name>

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196.3VSB_BAT(AP431)		
Size A	Document Number <Doc>	Rev R1.00
Date:	Tuesday, March 14, 2023	Sheet 196 of 253

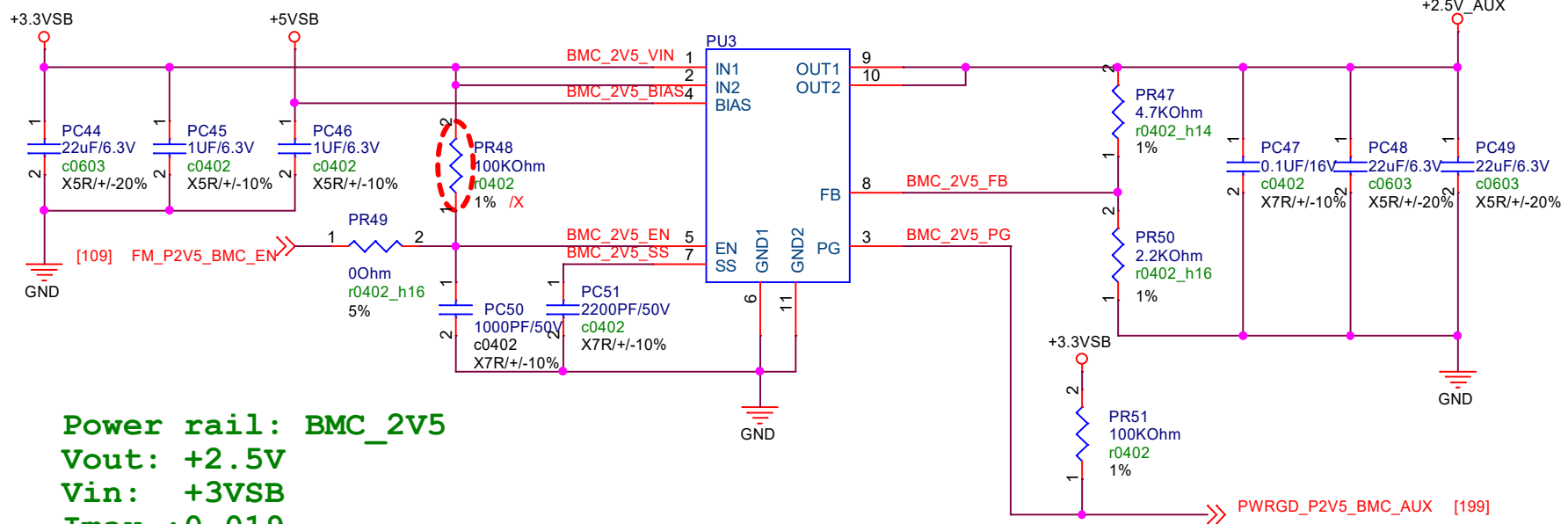


+3VSB = 3.398V, OCP~22A

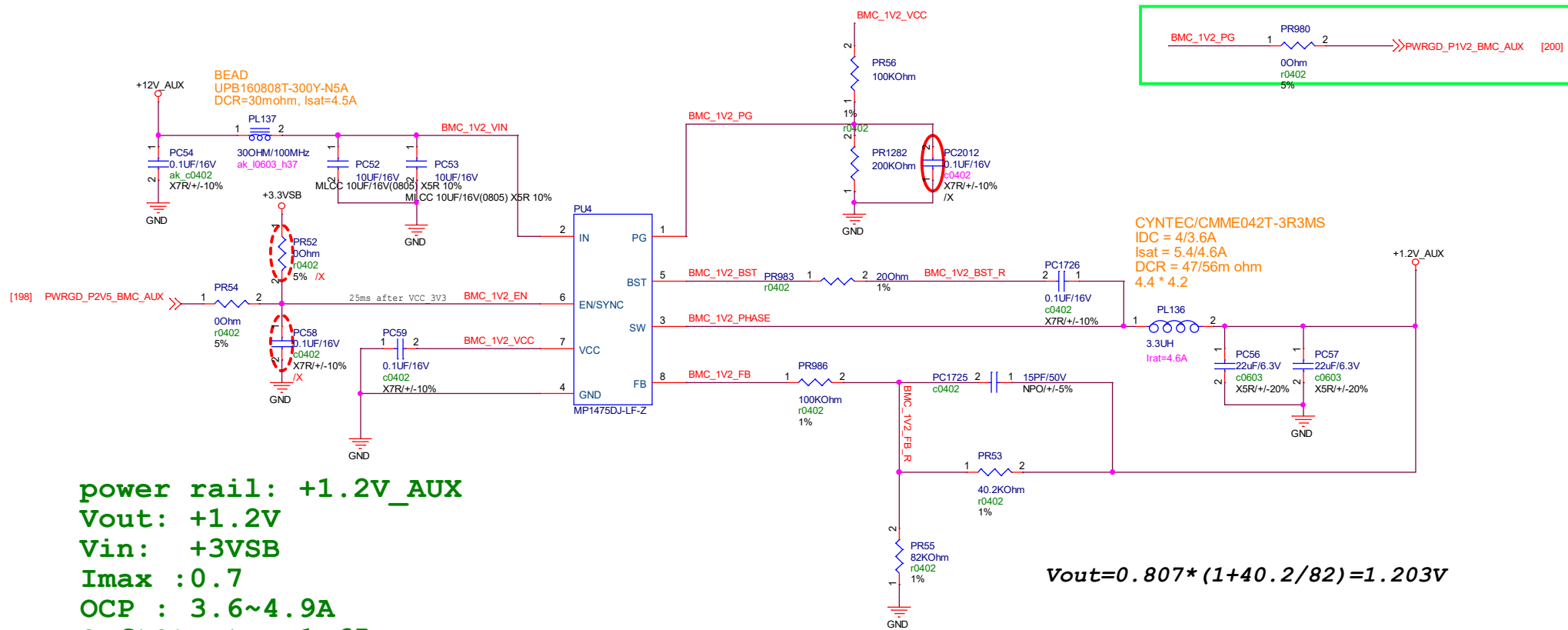
+5VSB = 5.01V, OCP~22A

<Variant Name>		
File	197.5VSB3VSB(TPS53355)	
Size	Document Number	Rev
C	<Doc>	R1.0
Date:	Tuesday, March 14, 2023	Sheet 197 of 253

# TPS74801DRCR



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198.BMC_2V5(TPS74810)		
Size	Document Number	Rev
Custom	<Doc>	<RevCo>
Date:	Tuesday, March 14, 2023	Sheet 198 of 253

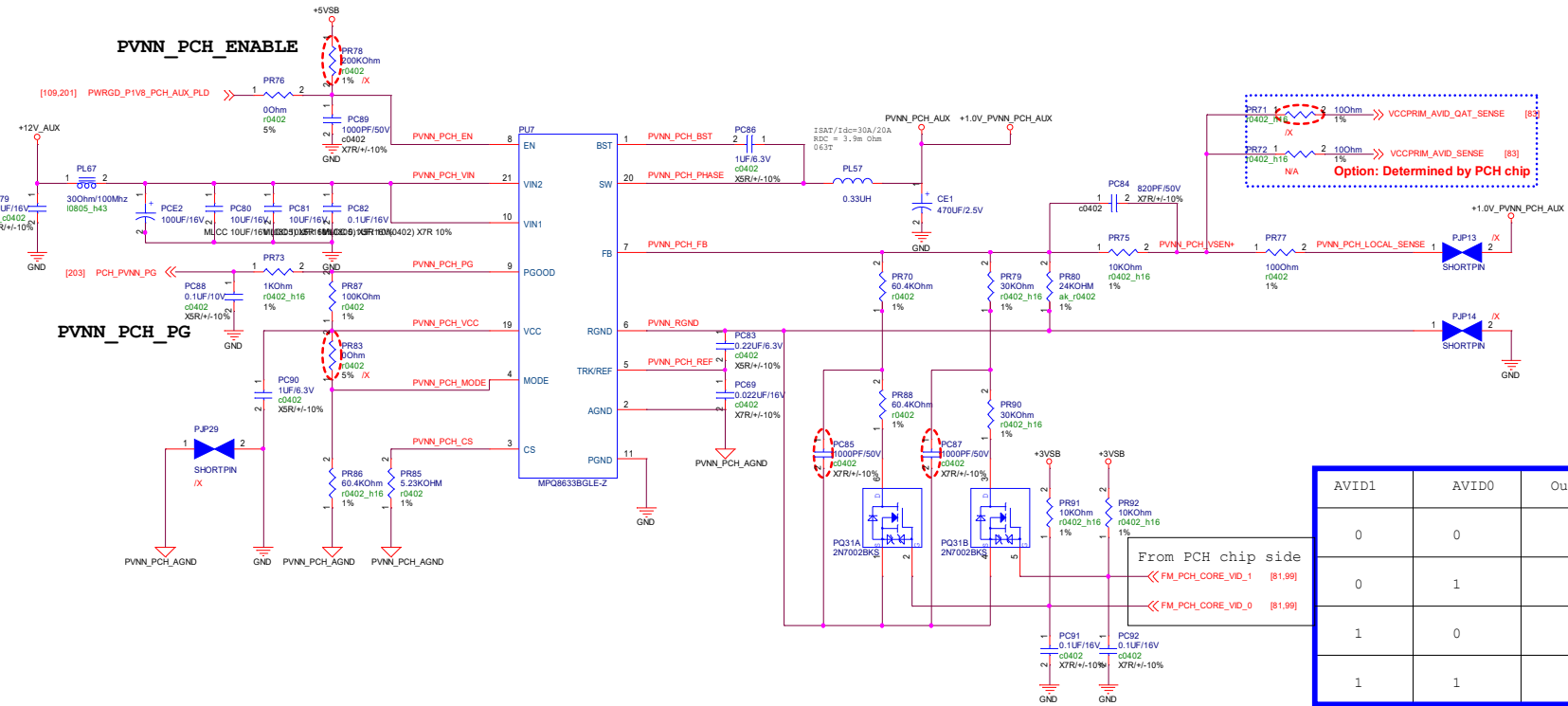


Title		
199.BMC_1V2(TPS62130)		
Size	Document Number	Rev
B	<Doc>	<RevCode>
Date:	Tuesday, March 14, 2023	
	Sheet	199 of 253

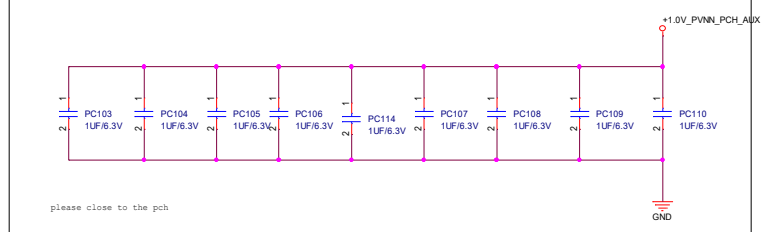
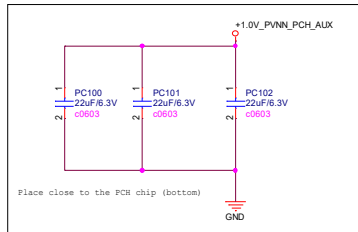
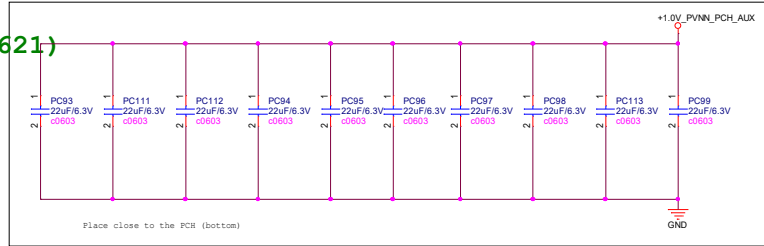




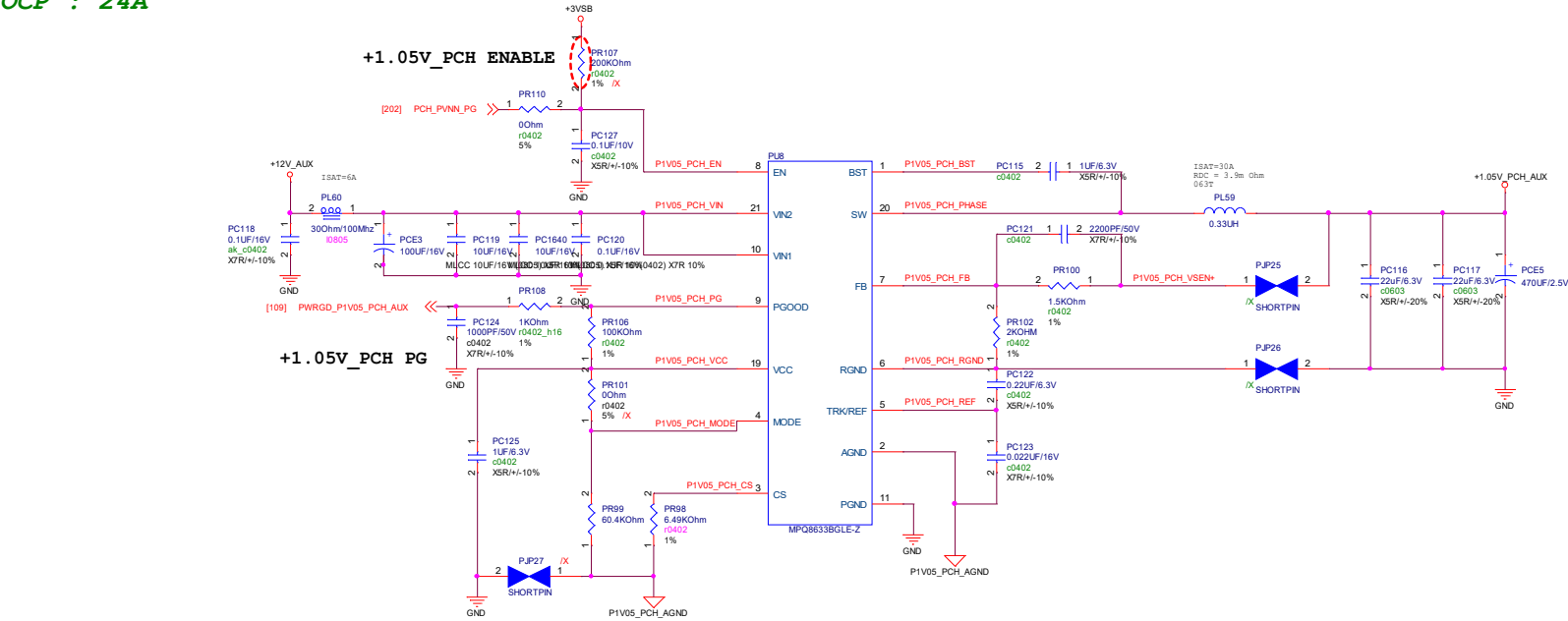




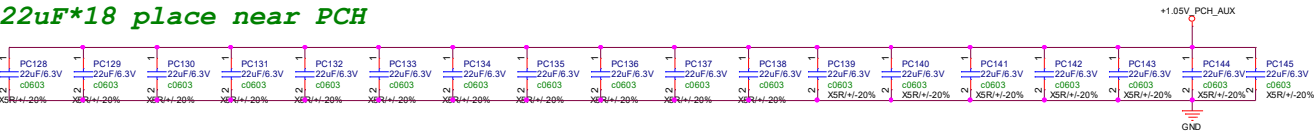
Power Rail : +1VPVNN\_PCH  
 $I_{max} / I_{tdc} = 10.5A / 9A$  (C621)  
 $F_{sw} : 1000KHz$  (CCM)  
 $OCP : 24A$



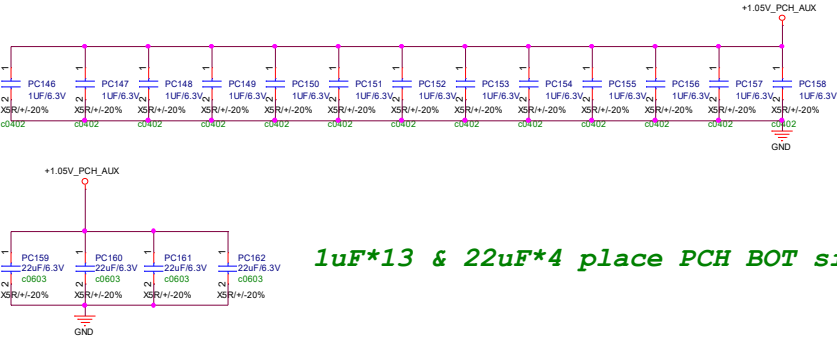
Power Rail : P1V05 PCH AUX  
Ipeak/ItDC = 10A /8.5A (C621)  
Fsw : 1000KHz  
OCP : 24A



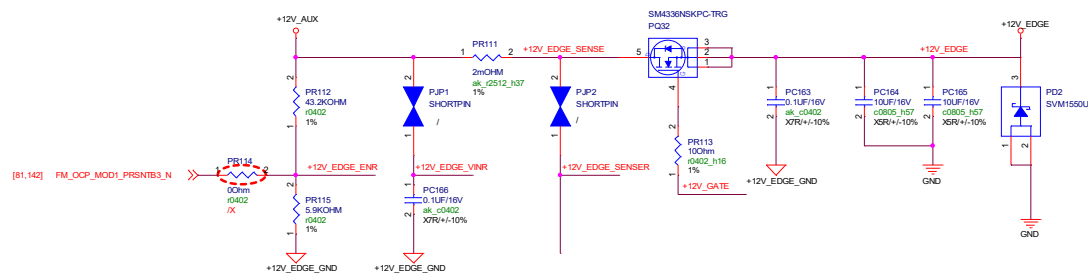
22uF\*18 place near PCH



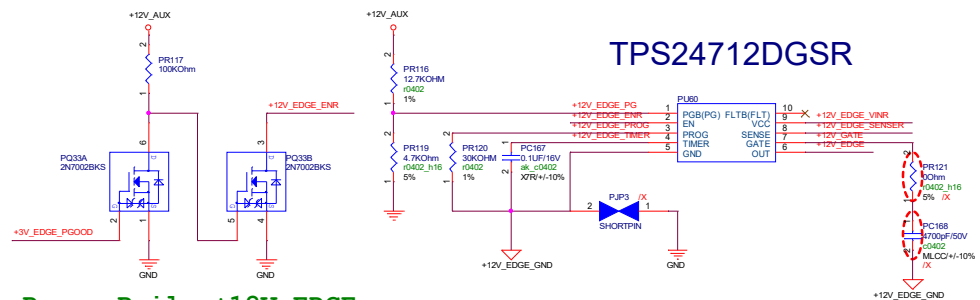
1uF\*13 & 22uF\*4 place PCH BOT side



PQ7595線路原本是PH6030AL，PartNumber改為SM4336  
BOM要上SM4336NSKP、BSC0906NS  
線路圖沒有元件可叫

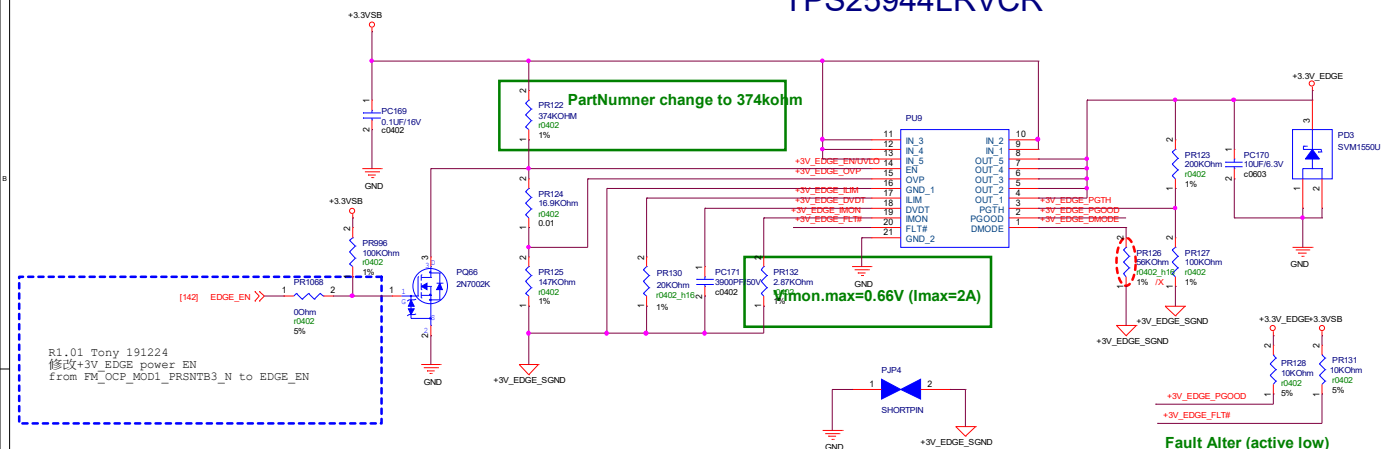


## TPS24712DGSR



```
Power Rail :+12V_EDGE
Io= 7.5A
OCP :13A
```

## TPS25944LRVCR



```
Power Rail :+3V_EDGE
Io= 1.1A
OCP :4.45A
OVP: 3.6V
UVP: 3V
Cout=10uF
Vppth=3V
```

**Fault Alter (active low)**

## +5V\_Switch

Gate Rise:10ms  
SM4336 Vgs th:1.5~2.5V  
Turnon\_V:6.5~7.5V

[109] FM\_P5V\_EN

Dummy\_load

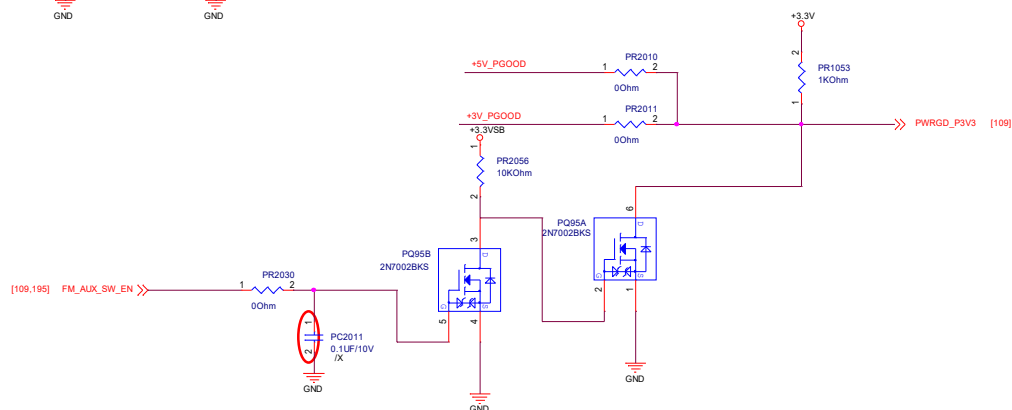
PMBT3904 Vgs th:0.65~0.85  
Turnon\_V:3~4V

## +3V\_Switch

Dummy\_load

Gate rise:27ms  
SM4336 Vgs th:1.5~2.5V  
Turnon\_V:6.5~7.5V

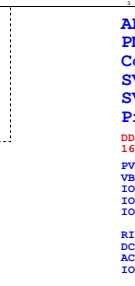
PMBT3904 Vgs th:0.65~0.85  
Turnon\_V:2.25~3



<Variant Name>

File	205.5V/3V(MOS-SWITCH)	Rev	R1.0
Size	Document Number		
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```
ABCD_DIMM
PMBus address:58/B
Config ID:0
SVID Bus: BUS#2
SVID address: 00h
Protocol ID:07h
```

DDR4 LR-DIMM 3D4H,2DPC,8Rx4,  
16Gb,3200MT/s,8 DIMMs/VR,256  
PVDDQ SPECIFICATIONS:  
VBOOT = 1.2V  
IOUT STEP = 98.5A@11.6A/us  
IOUT PEAK = 118A  
IOUT TDC = 118A

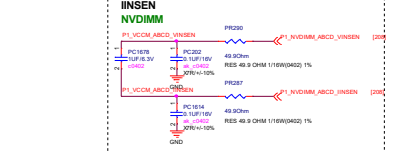
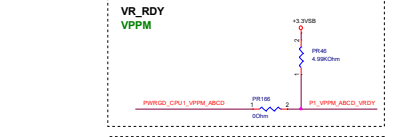
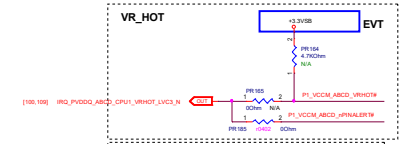
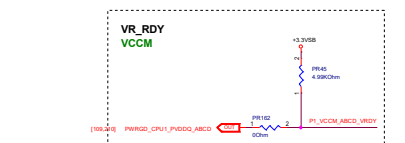
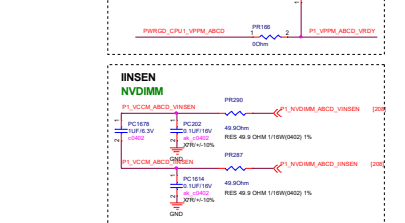
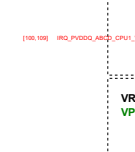
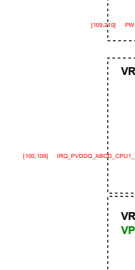
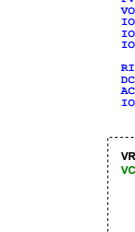
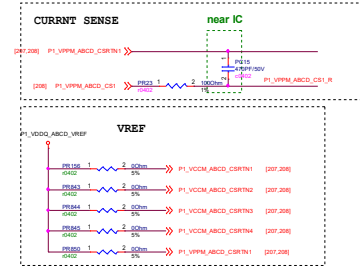
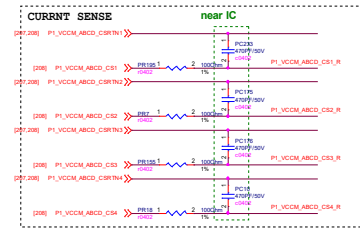
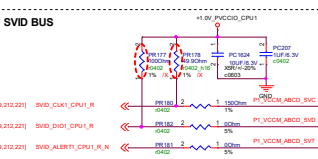
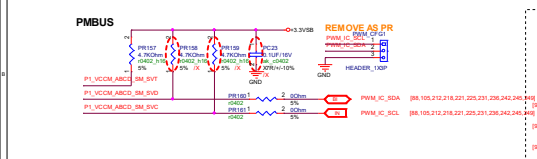
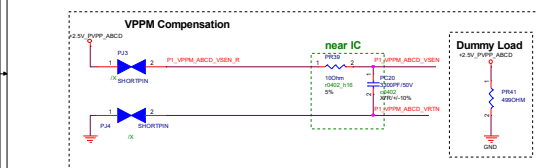
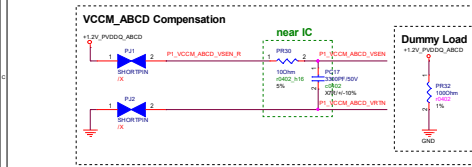
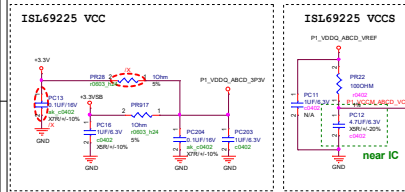
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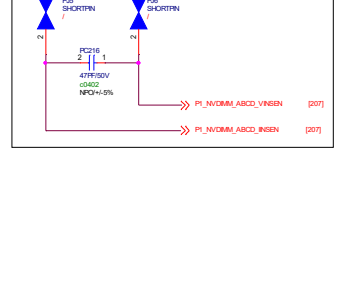
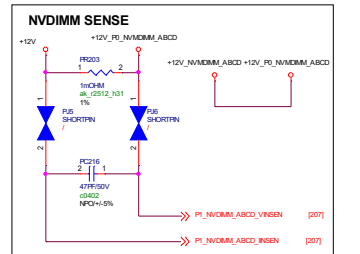
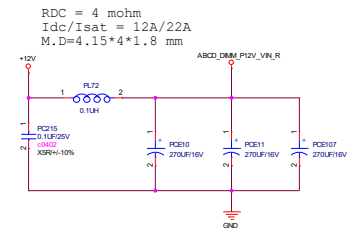
RIPPLE GUIDELINE = +/- 6mV
DC TOL = +/- 6mV
AC & DC TOL = +60mV/-40mV
IOUT DI/DT = 19.5A/uS

PVPP SPECIFICATIONS:
VOUT = 2.575V
IOUT TDC = 8.8A
IOUT PEAK = 11.87A
IOUT STEP = 7.06A

RIPPLE GUIDELINE = +/- 25mV
DC TOL = +/- 38mV
AC & DC TOL = +137mV/-127mV
IOUT DI/DT = 28.6A/US

```



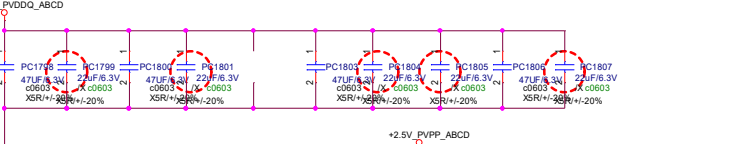
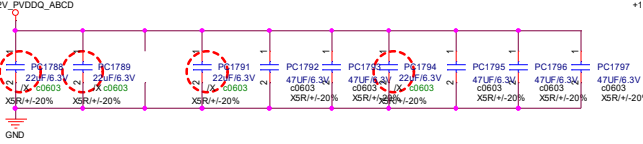
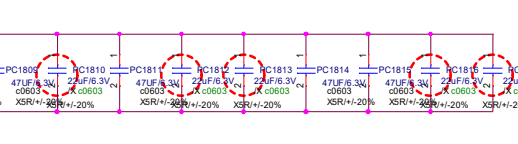
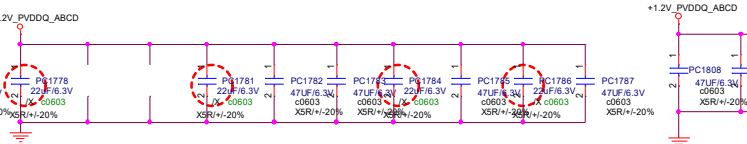
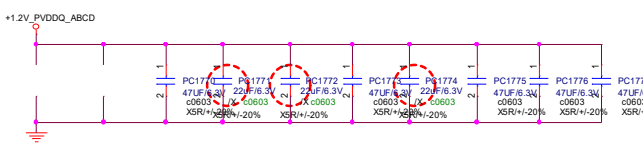
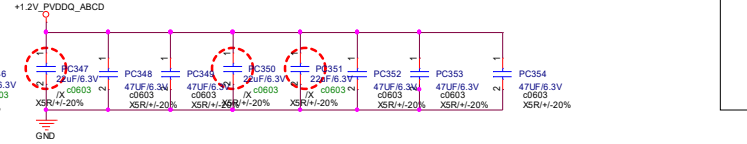
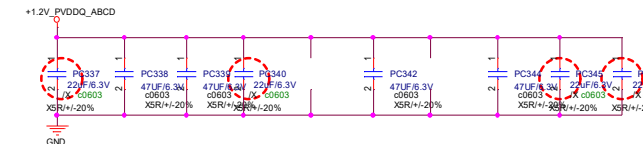
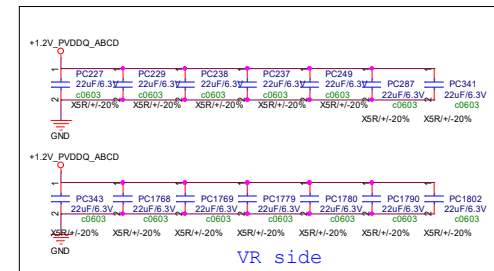
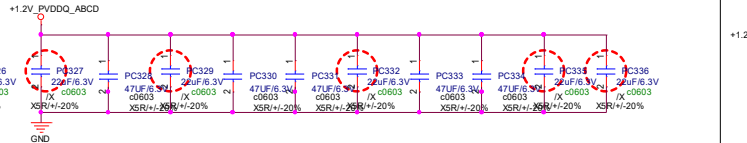
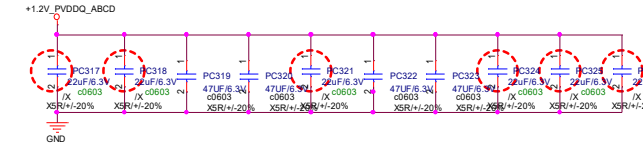
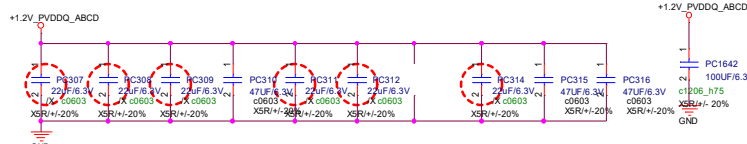
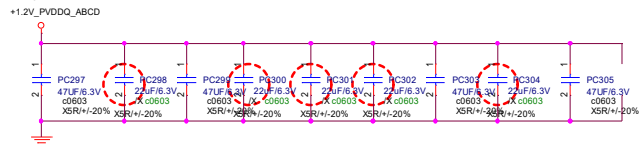
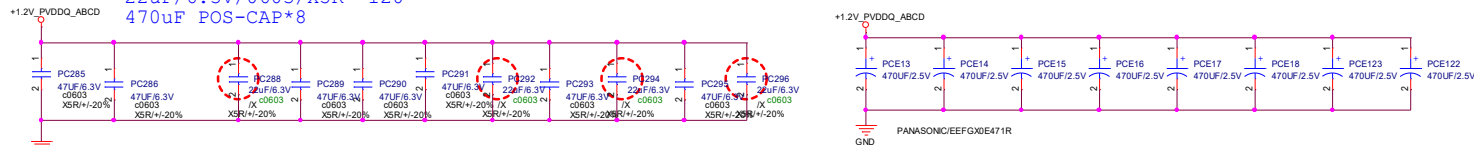


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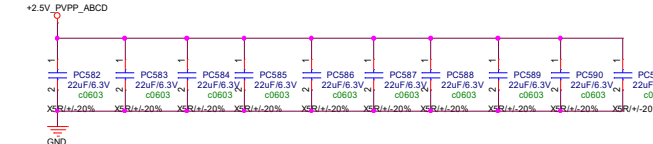
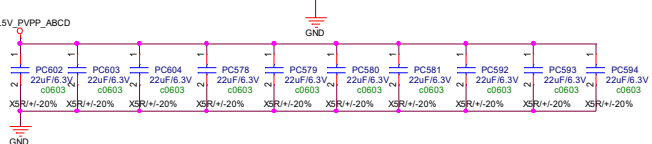




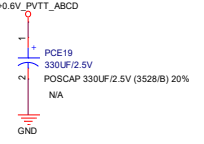
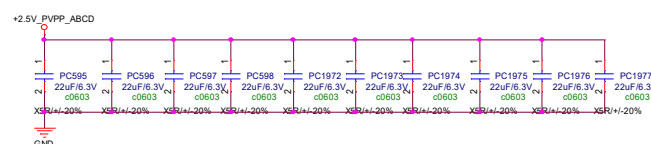
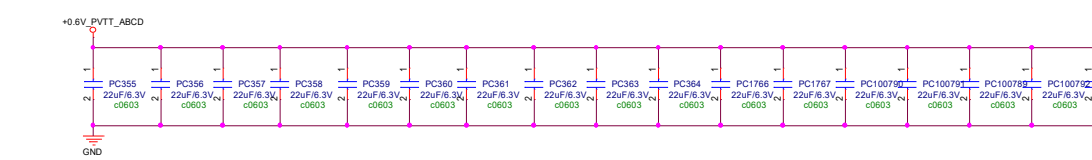
VCCM total Cap  
22uF/6.3V/0603/X5R \*120  
470uF POS-CAP\*8

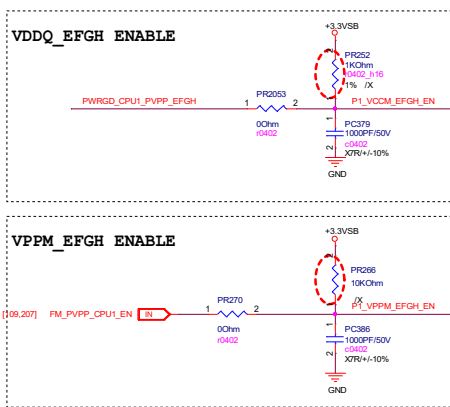
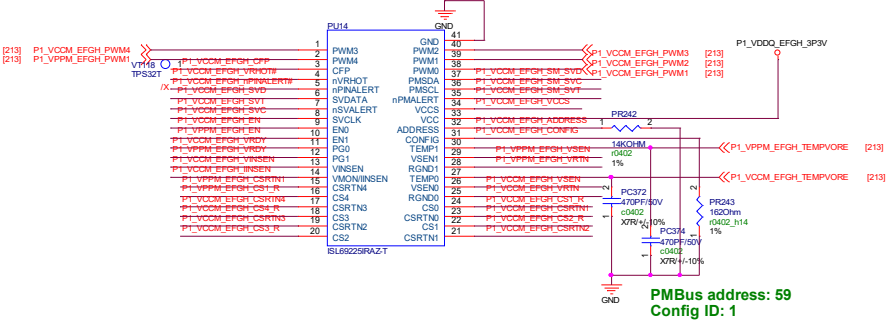


VPP total Cap  
22uF/6.3V/0603/X5R \*30  
330uF POS-CAP\*2



VTM total Cap  
22uF/6.3V/0603/X5R \*17  
330uF POS-CAP\*1





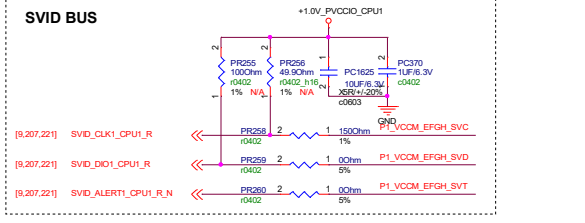
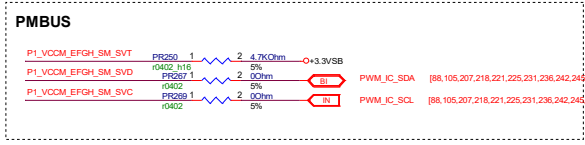
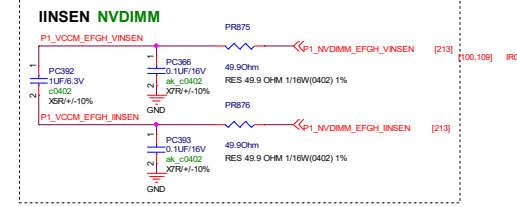
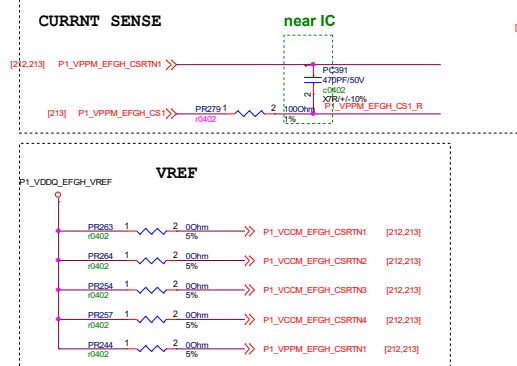
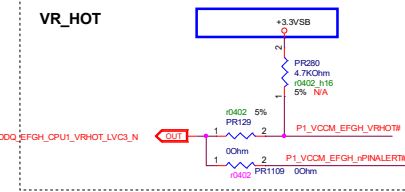
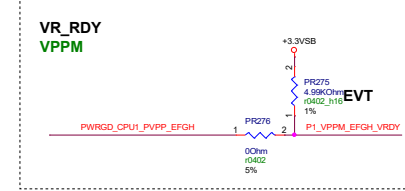
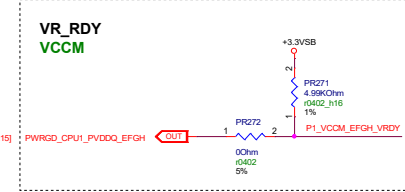
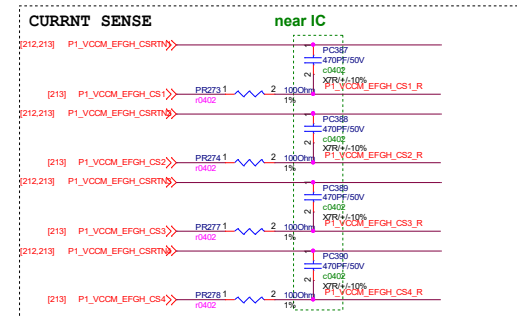
**EFGH DIMM**  
**PMBuss address:59/B2**  
**Config ID:1**  
**SVID Bus: BUS#2**  
**SVID address: 00h**  
**Protocol ID:07h**

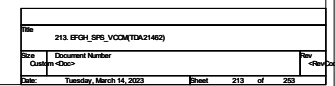
**PVDDQ SPECIFICATIONS:**  
**VBOOT = 1.2V**  
**IOUT STEP = 98.5A@11.6A/us**  
**IOUT PEAK = 118A**  
**IOUT TDC = 118A**

**RIPPLE GUIDELINE = +/- 6mV**  
**DC TOL = +/- 6mV**  
**AC & DC TOL = +60mV/-40mV**  
**IOUT DI/DT = 19.5A/us**

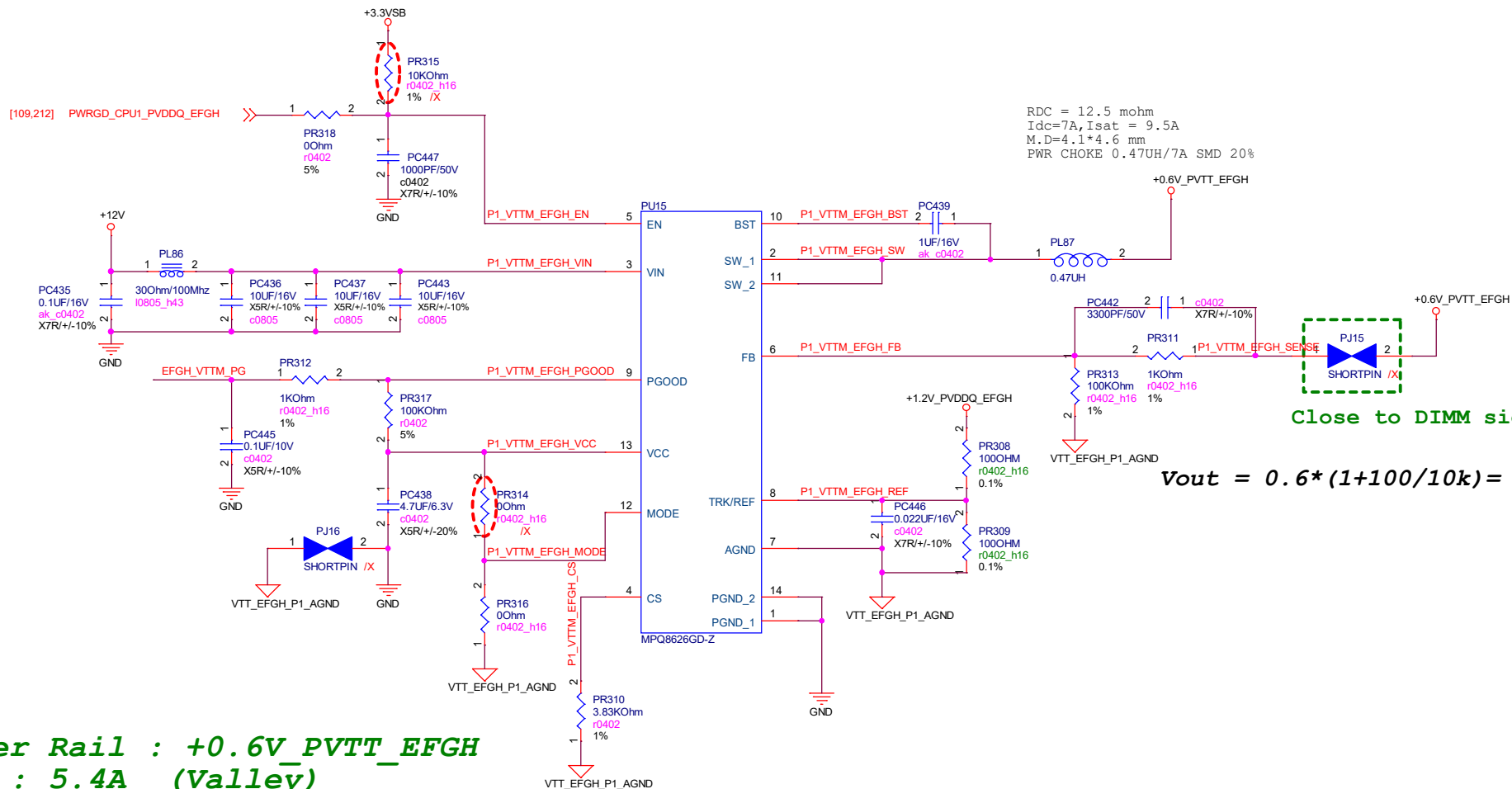
**PVPP SPECIFICATIONS:**  
**VOUT = 2.575V**  
**IOUT TDC = 8.8A**  
**IOUT PEAK = 11.87A**  
**IOUT STEP = 7.06A**

**RIPPLE GUIDELINE = +/- 25mV**  
**DC TOL = +/- 38mV**  
**AC & DC TOL = +137mV/-127mV**  
**IOUT DI/DT = 28.6A/US**



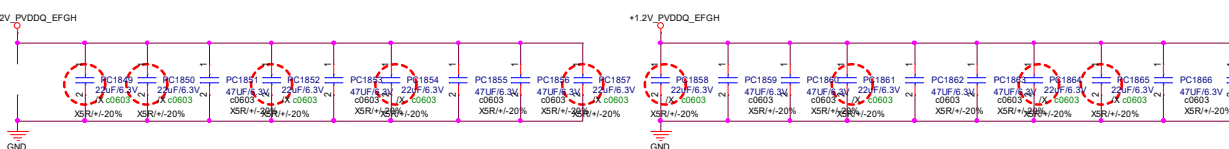
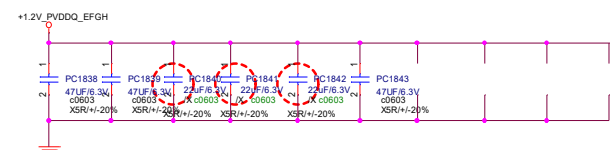
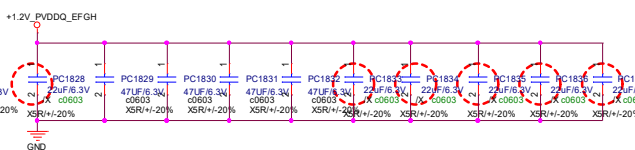
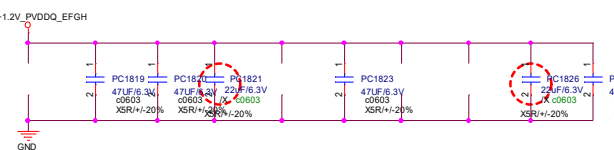
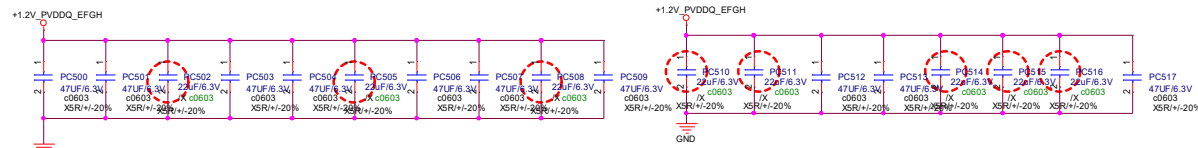
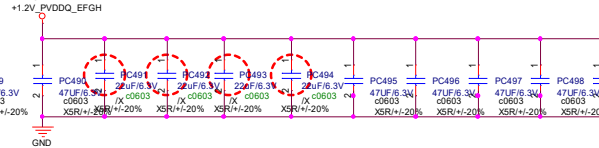
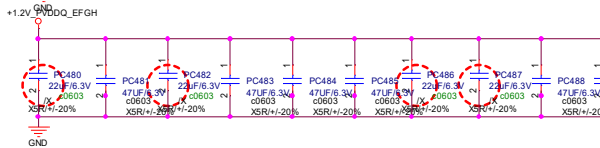
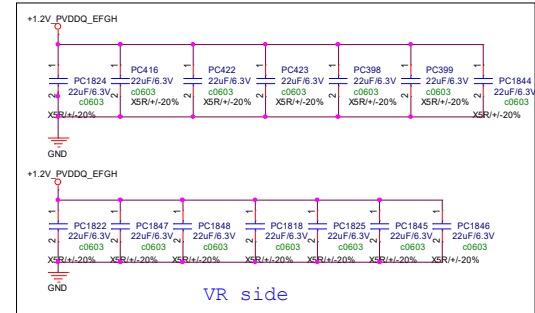
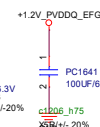
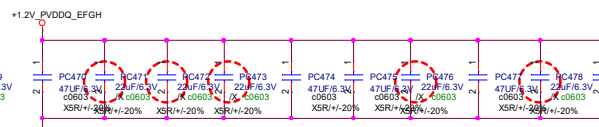
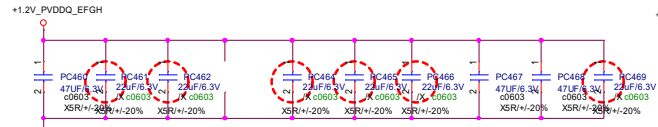
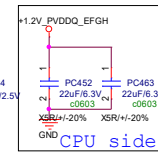
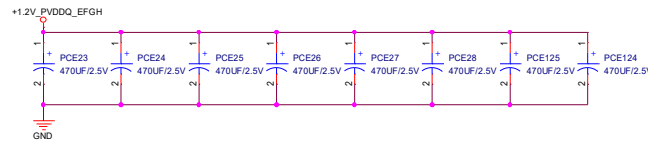
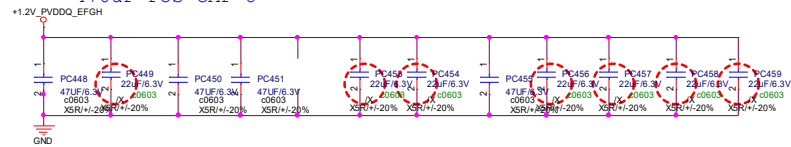


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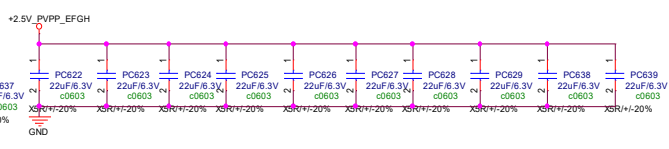
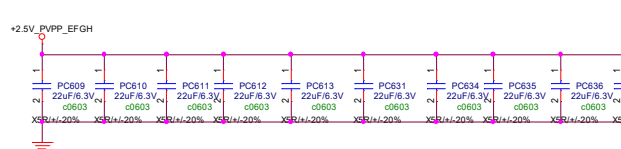
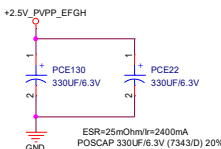


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215. EFGH_POL_VTTM(TPS53317)		
Size	Document Number	Rev
B	<Doc>	<RevCode>
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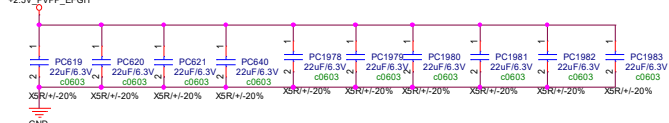
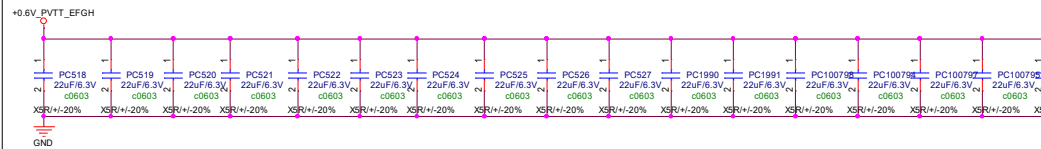
VCCM total Cap  
22uF/6.3V/0603/X5R \*120  
470uF POS-CAP\*8



VPP total Cap  
22uF/6.3V/0603/X5R \*30  
330uF POS-CAP\*2



VTTM total Cap  
22uF/6.3V/0603/X5R \*17  
330uF POS-CAP\*1



217. =====CPU1\_VCORE=====

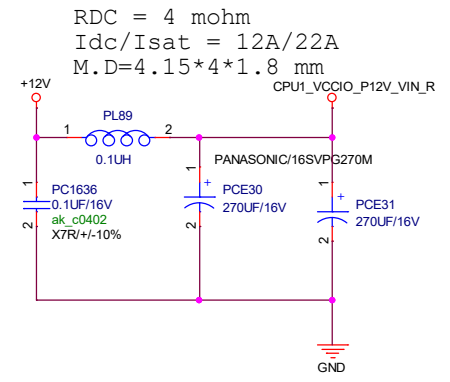
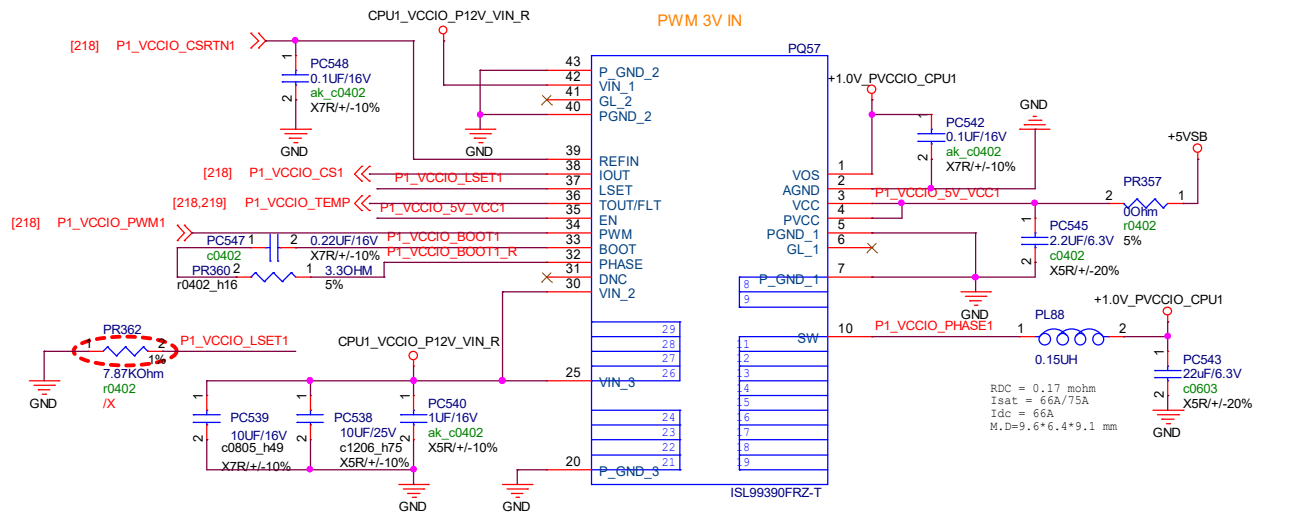
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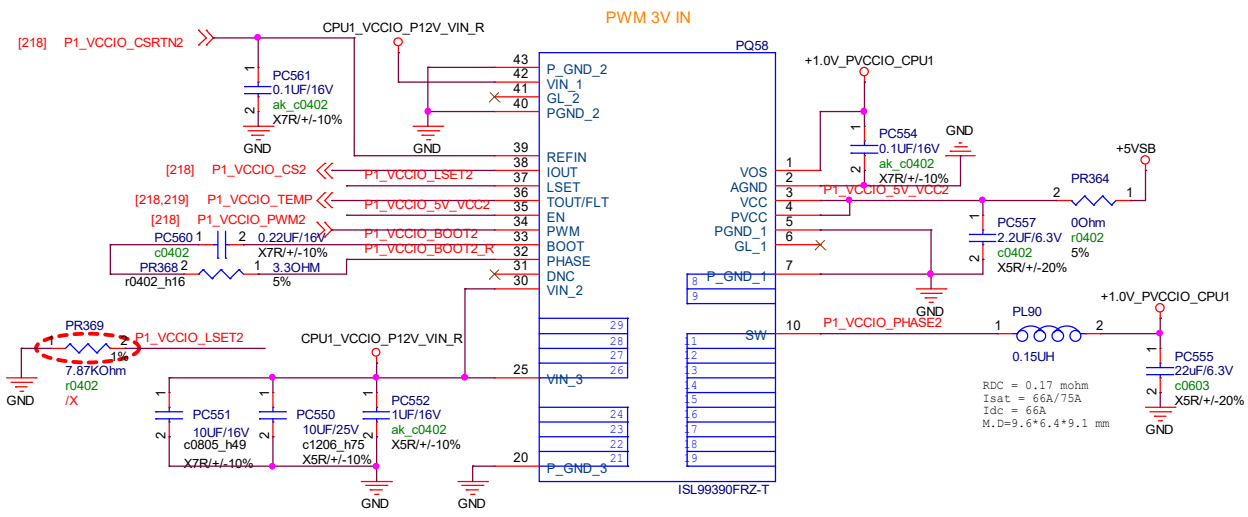
Title	Author	Year	Journal	Volume	Issue	Page
1. The Effect of Temperature on the Rate of Reaction	John Doe	2018	Journal of Chemical Education	95	3	456-462
2. Kinetics of the Reaction Between Hydrogen Peroxide and Potassium Iodide	Jane Smith	2017	Journal of Chemical Education	94	2	234-240
3. The Effect of Concentration on the Rate of Reaction	Michael Brown	2016	Journal of Chemical Education	93	1	123-129
4. The Effect of Surface Area on the Rate of Reaction	Sarah White	2015	Journal of Chemical Education	92	4	567-573
5. The Effect of Catalysts on the Rate of Reaction	David Green	2014	Journal of Chemical Education	91	5	678-684



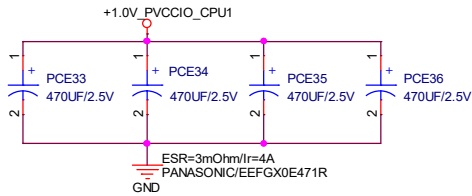




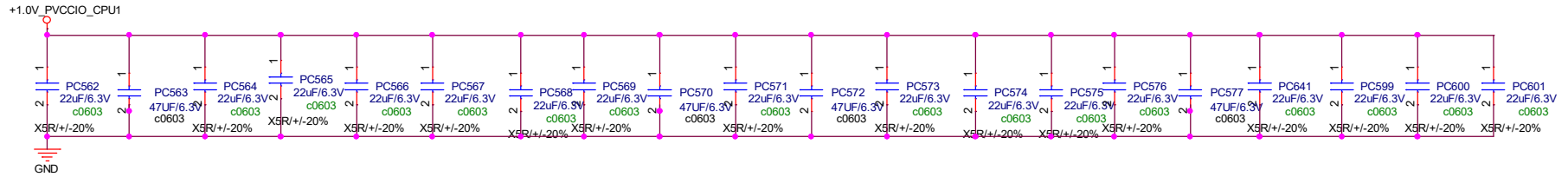
RDC = 4 mohm  
Idc/Isat = 12A/22A  
M.D=4.15\*4\*1.8 mm



Title			219. CPU1_SPS_VCCIO(TDA21462)
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VCCIO total Cap  
22uF/6.3V/0603/X5R \*20  
470uF POS-CAP\*4



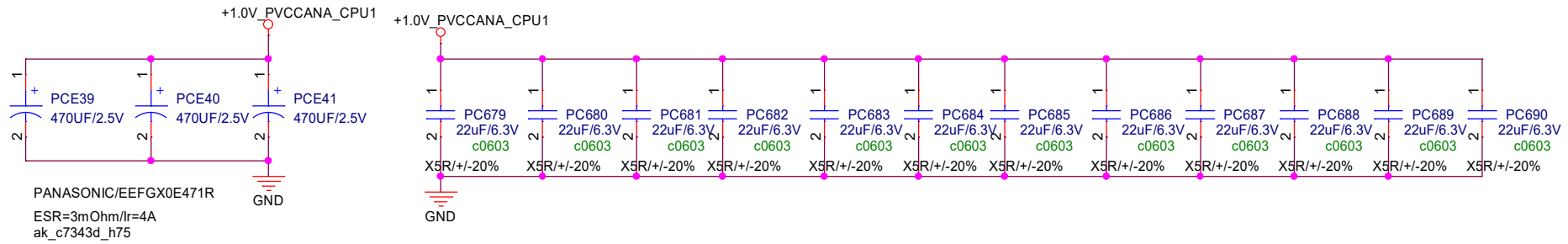
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220. CPU1_CAP_VCCIO		
Size	Document Number	Rev
B	<Doc>	<RevCode>
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	Sheet	220 of 253



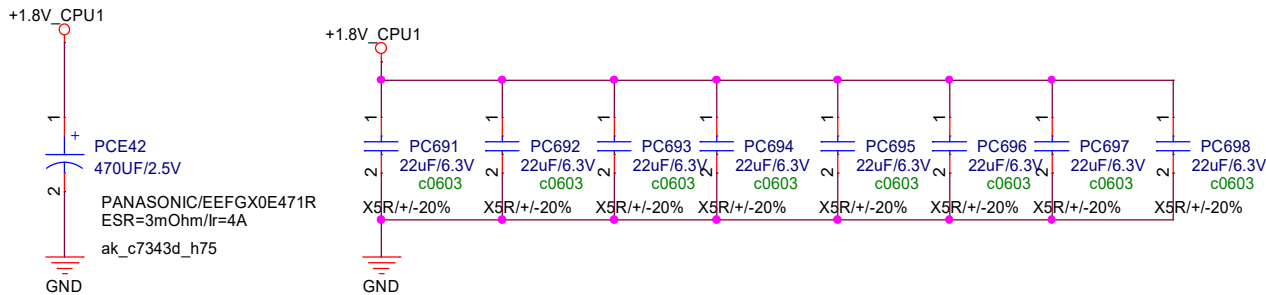




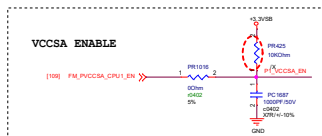
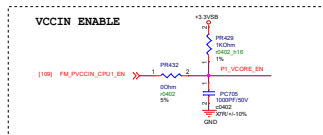
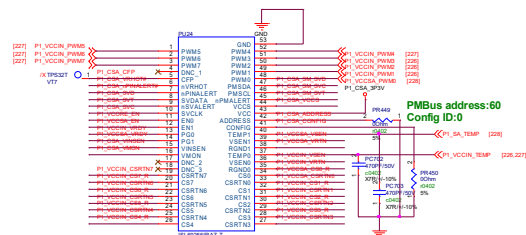
PVCCANA total Cap  
 22uF/6.3V/0603/X5R \*12  
 470uF POS-CAP\*3



VCC1V8total Cap  
 22uF/6.3V/0603/X5R \*8  
 470uF POS-CAP\*1



Title		
224. CPU1_CAP_VCC1V8+VCCANA		
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VCCSA  
PMBus address:60/C0  
Config ID:0  
SVID Bus: BUS#1  
SVID address: 01h  
Protocol ID:07h

VCCIN  
PMBus address:60/C0  
Config ID:0  
SVID Bus: BUS#1  
SVID address: 00h  
Protocol ID:04h

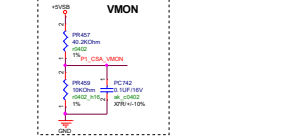
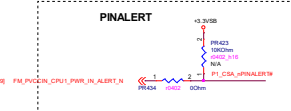
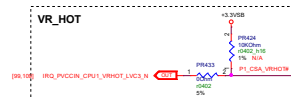
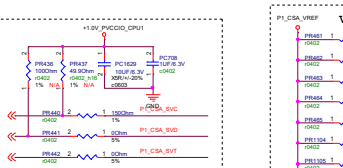
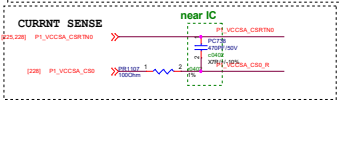
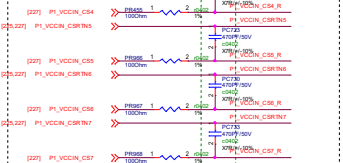
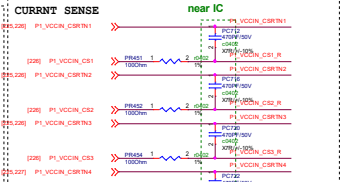
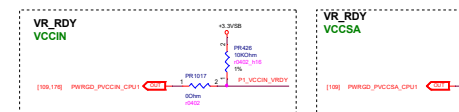
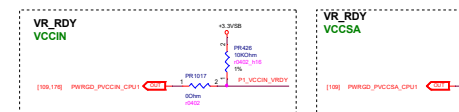
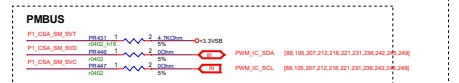
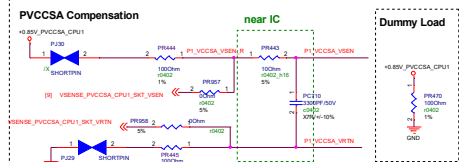
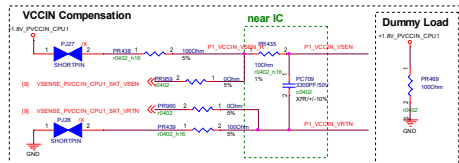
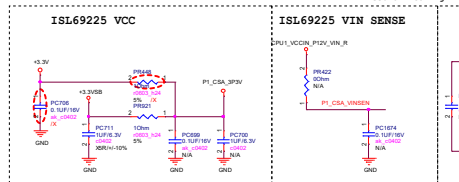
#### PVCCIN SPECIFICATIONS:

VBOOT=1.8V  
RIPPLE GUIDELINE = +/- 10mV  
DC TOL = +/- 0.5  
TOB = +/- 22mV  
TDC= 192.6A  
PEAK=459.7A  
STEP=374.4A  
DI/DT=1140A/us

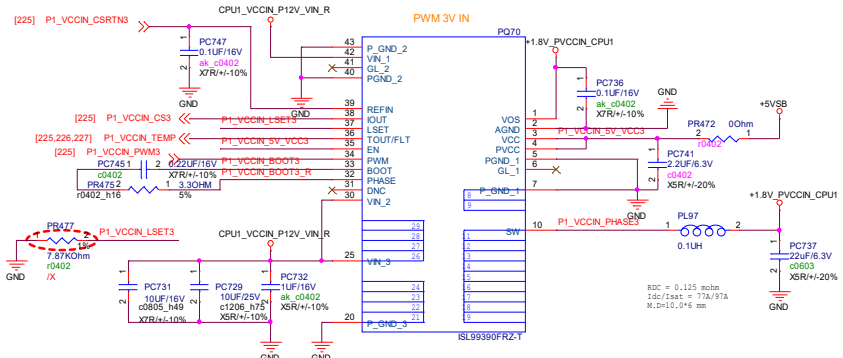
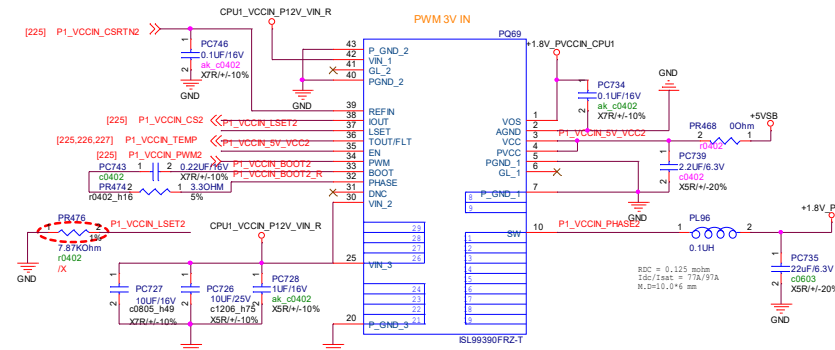
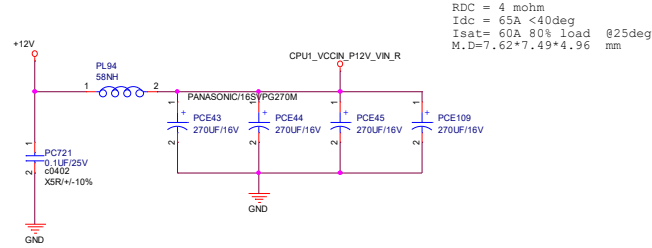
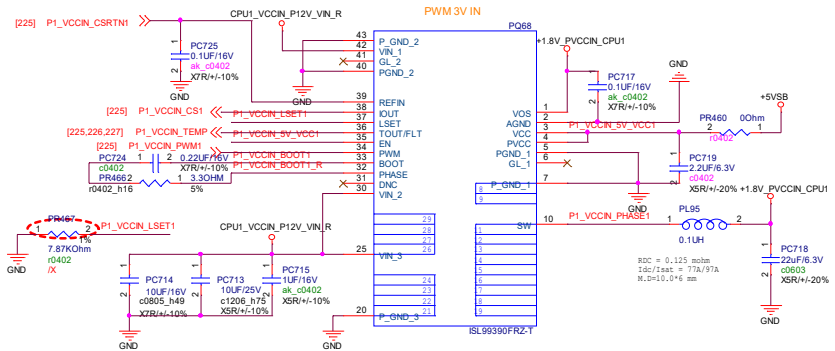
#### VCCSA SPECIFICATIONS:

VBOOT = 0.91V  
IOUT TDC = 37A  
IOUT PEAK = 37A  
IOUT STEP = 18.4A  
IOUT DI/DT = 7.1A/US  
AC & RIPPLE TOL = +47mV/-43mV  
RIPPLE GUIDELINE = +/- 10mV

330 ohm Config ID = 0

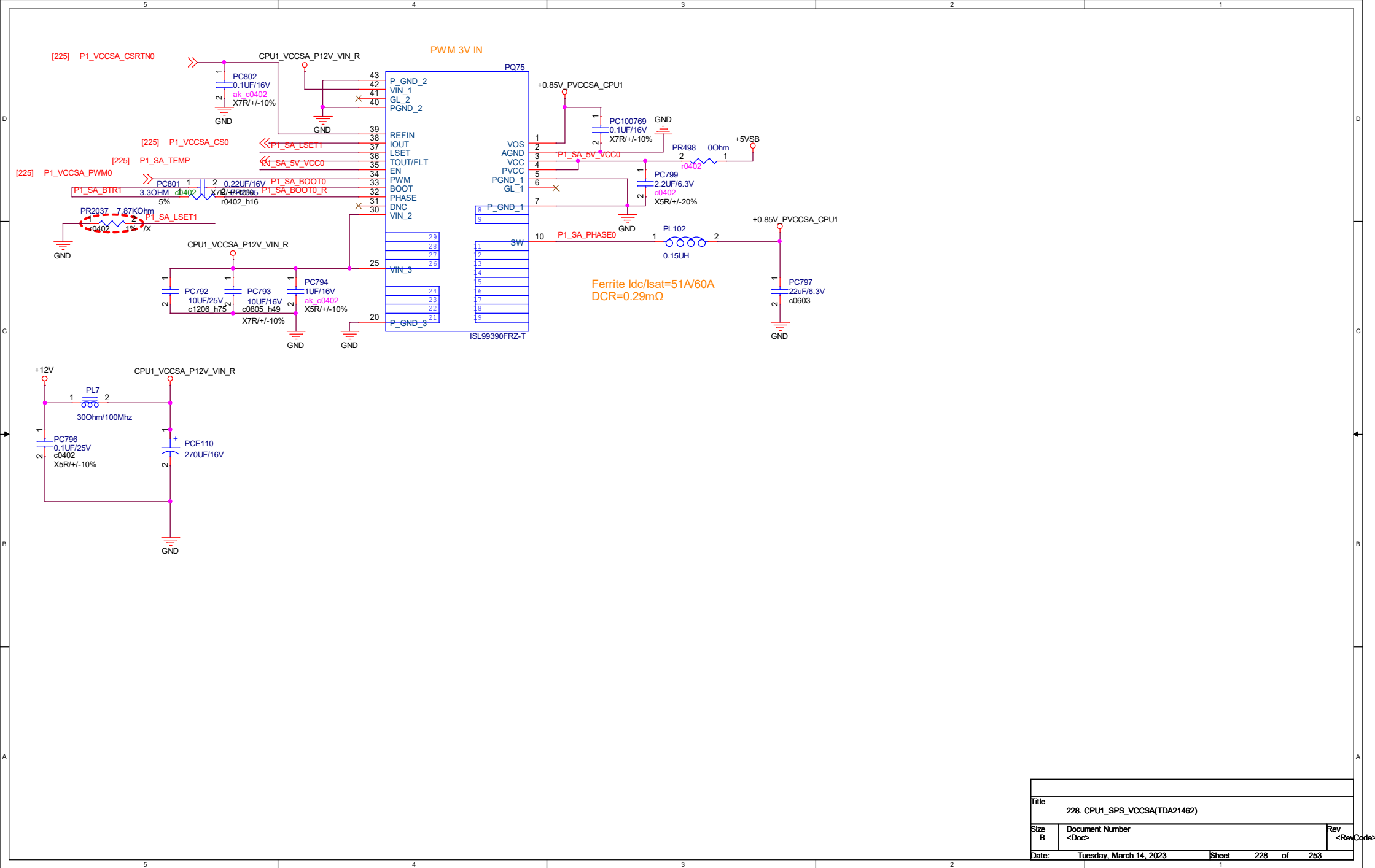


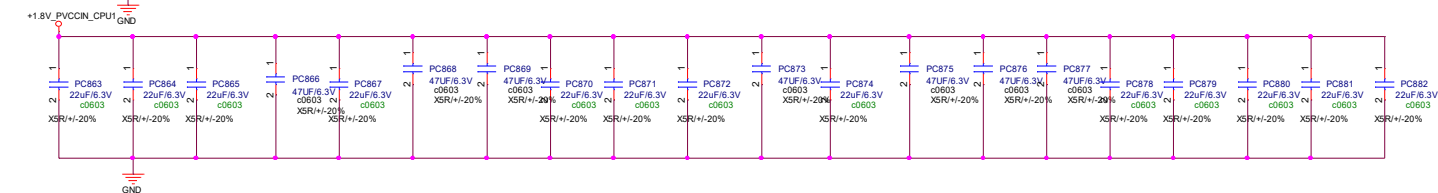
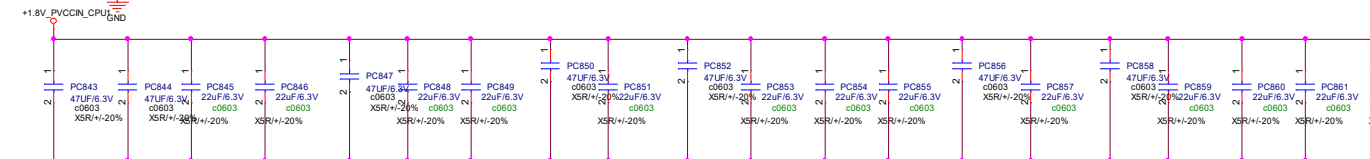
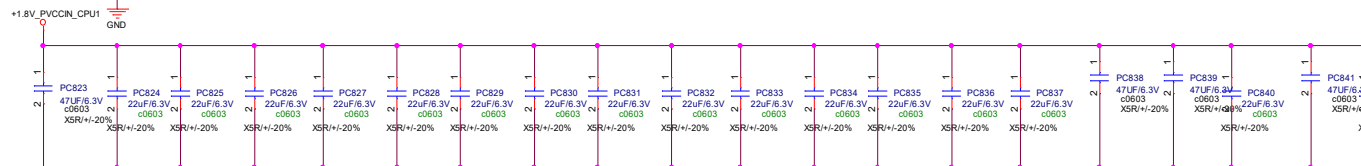
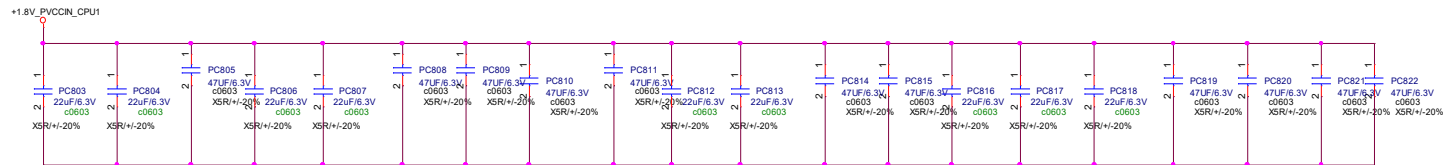
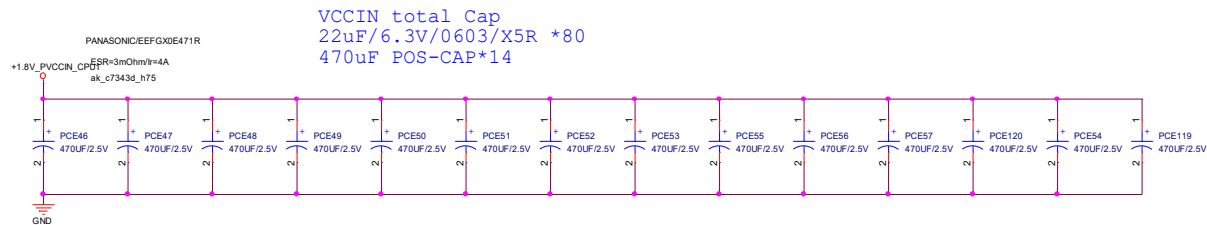




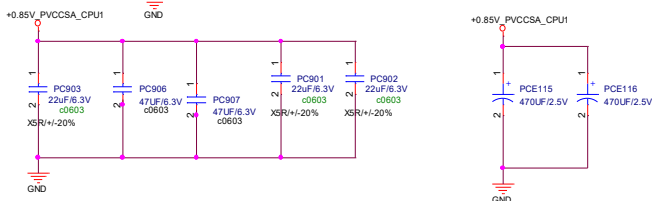
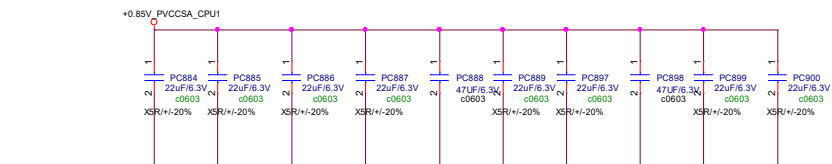
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226 CPU1_SPS1-3_VCCIN(TDA21490			
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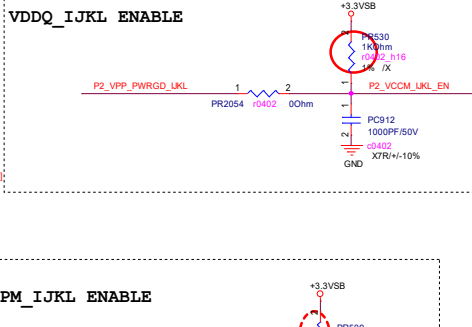
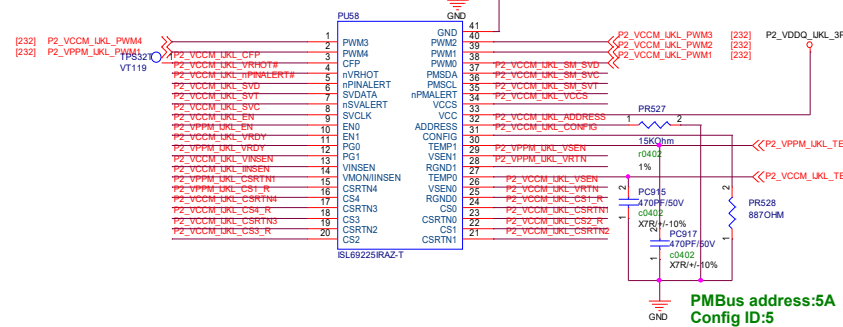




VCCSA total Cap  
 22uF/6.3V/0603/X5R \*15  
 470uF/2.5V\*2





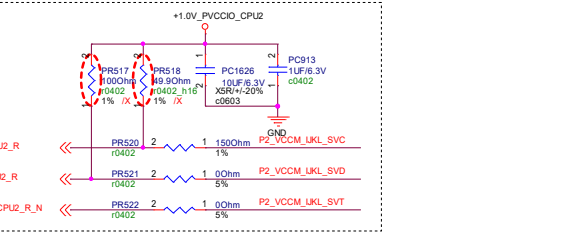
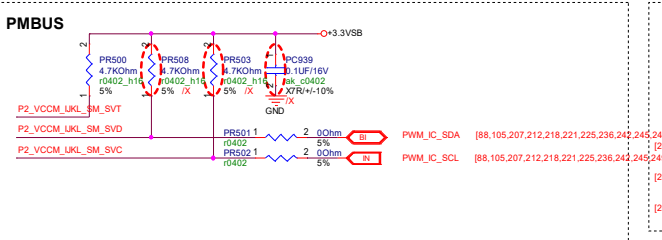
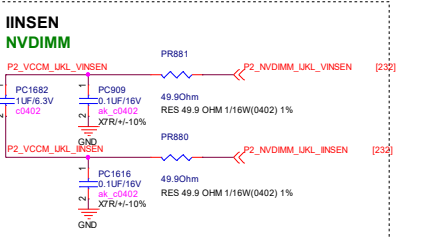
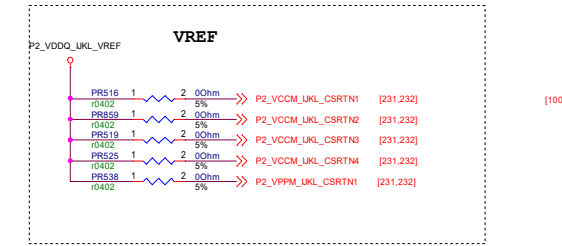
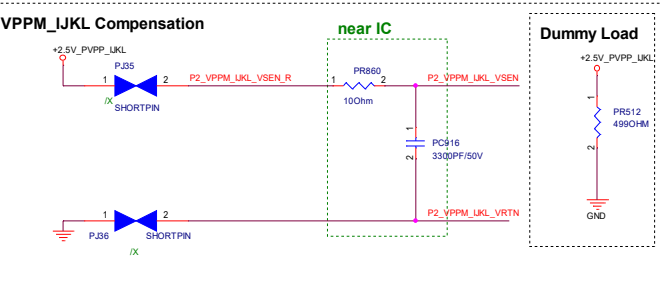
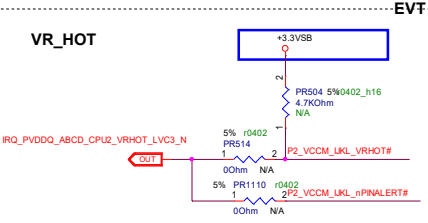
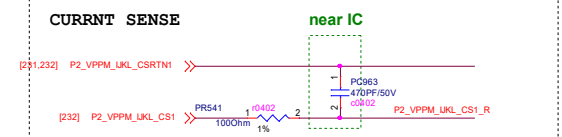
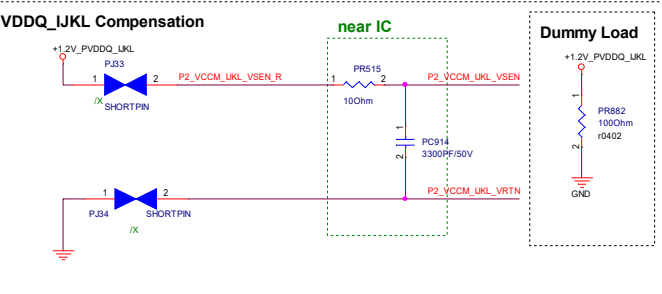
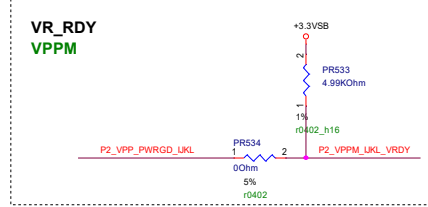
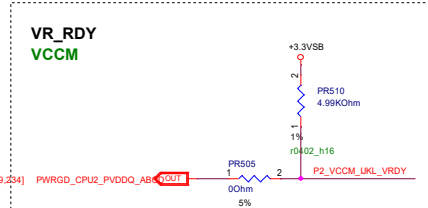
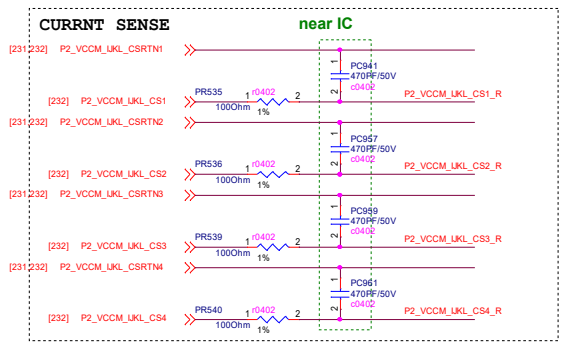
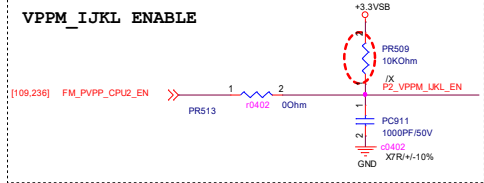
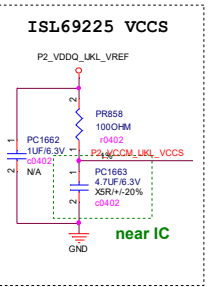
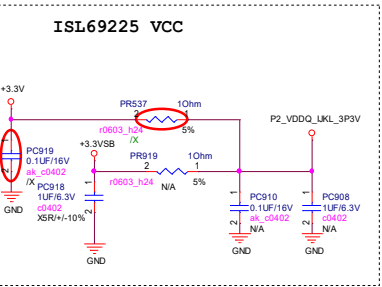


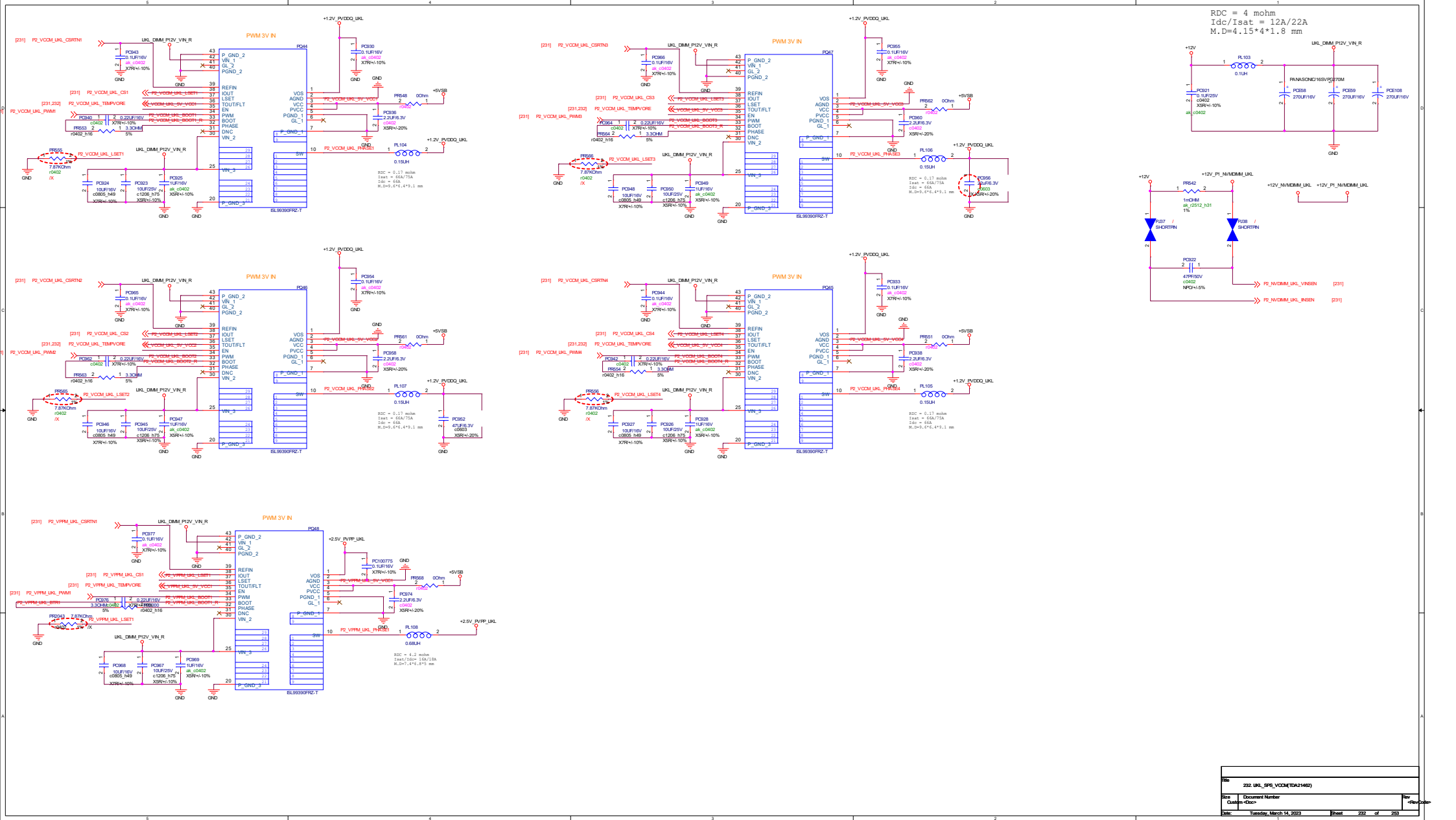
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Config ID:2  
SVID Bus: BUS#2  
SVID address: 00h  
Protocol ID:07h

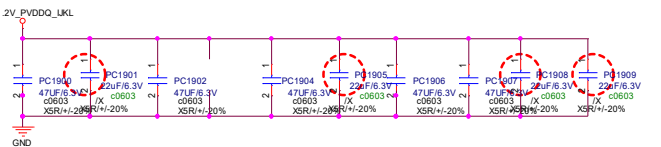
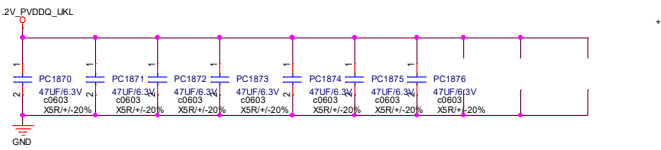
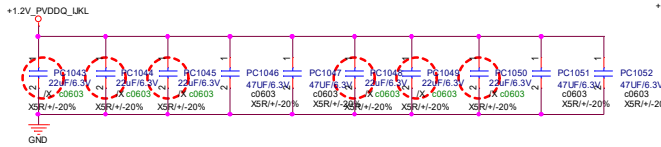
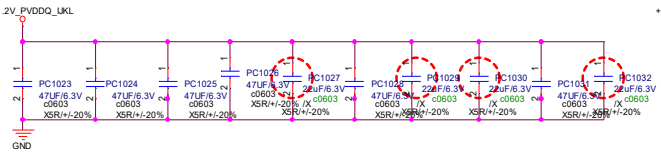
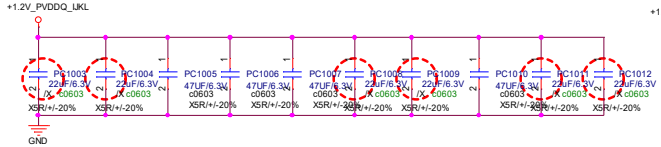
PVDDQ SPECIFICATIONS:  
VBOOT = 1.2V  
IOUT STEP = 98.5A@11.6A/us  
IOUT PEAK = 118A  
IOUT TDC = 118A

VRDY SPECIFICATIONS:  
VOUT = 2.575V  
IOUT TDC = 8.8A  
IOUT PEAK = 11.87A  
IOUT STEP = 7.06A

VRDY SPECIFICATIONS:  
VOUT = 2.575V  
IOUT TDC = 8.8A  
IOUT PEAK = 11.87A  
IOUT STEP = 7.06A







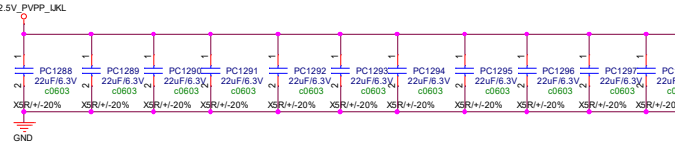
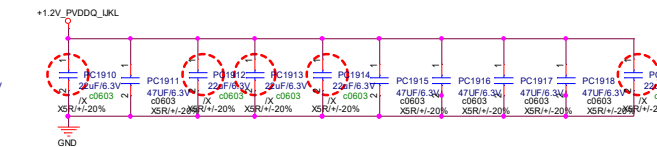
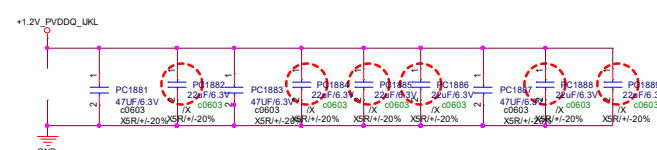
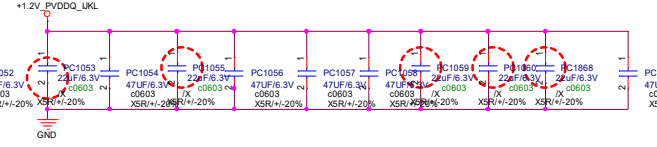
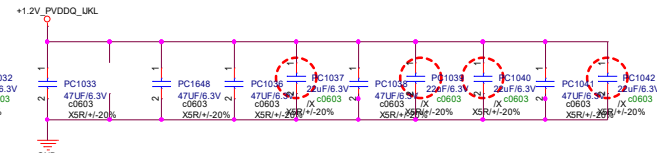
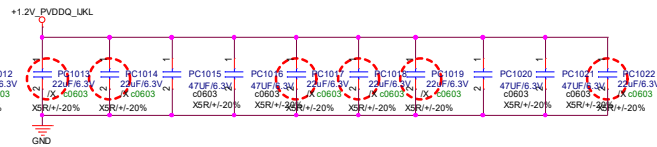
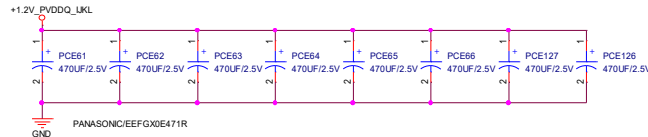
+2.5V\_PVPP\_LKL

PCE131  
330UF/6.3V

PCE60  
330UF/6.3V

GND

ESR=25mOhm/1r=2400mA  
POSCAP 330UF/6.3V (7343/D) 20%



+0.6V\_PVTT\_L

1

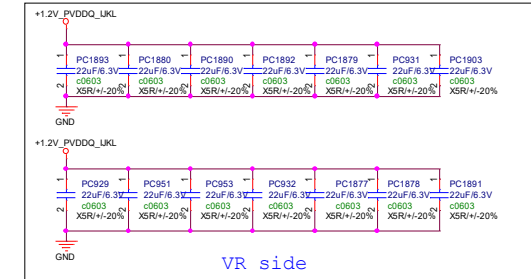
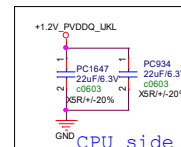
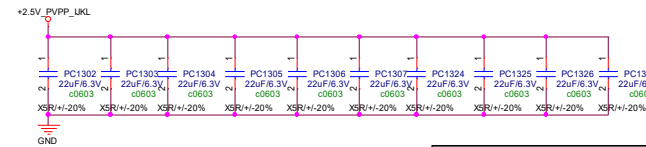
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PC

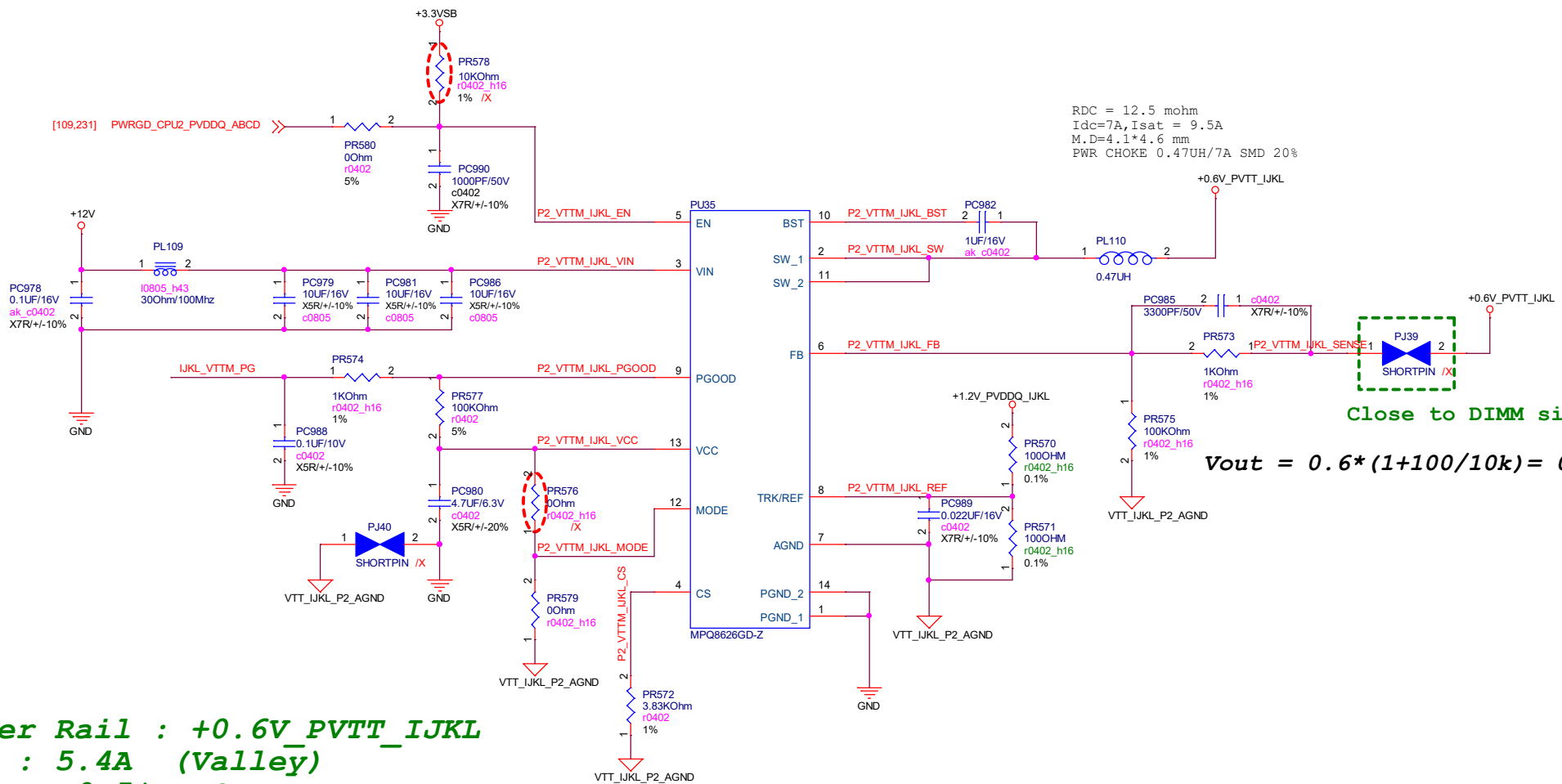
330

PO

N/A







Title		
234. IJKL_POL_VTTM(TPS53317)		
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D

C

B

A

Code:

&lt;RevCode&gt;

Title
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235. IJKL\_SPS\_VPPM(TDA21462)

Size

Size	DocuM
Custom	<Doc>

Document Number
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Date:

Tuesday, March 14, 2023

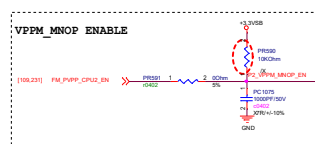
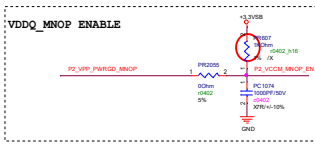
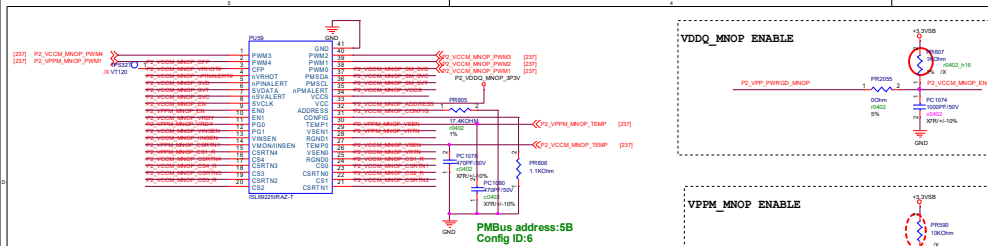
Sheet

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of

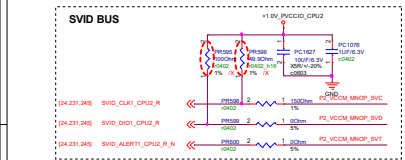
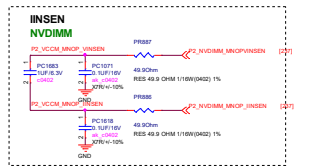
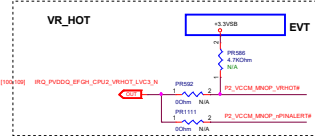
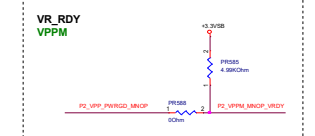
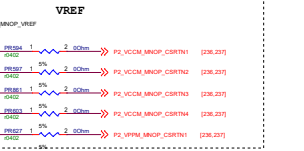
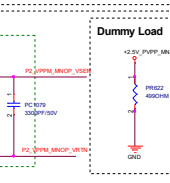
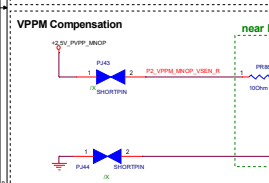
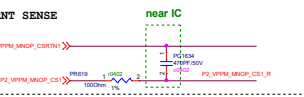
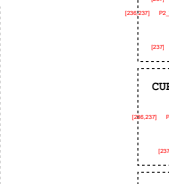
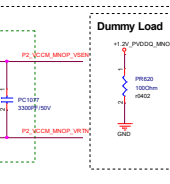
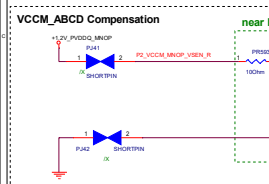
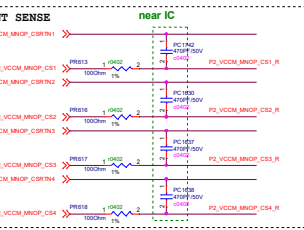
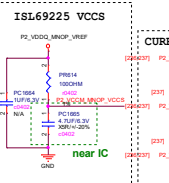
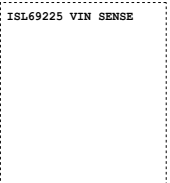
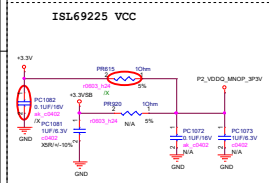
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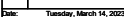
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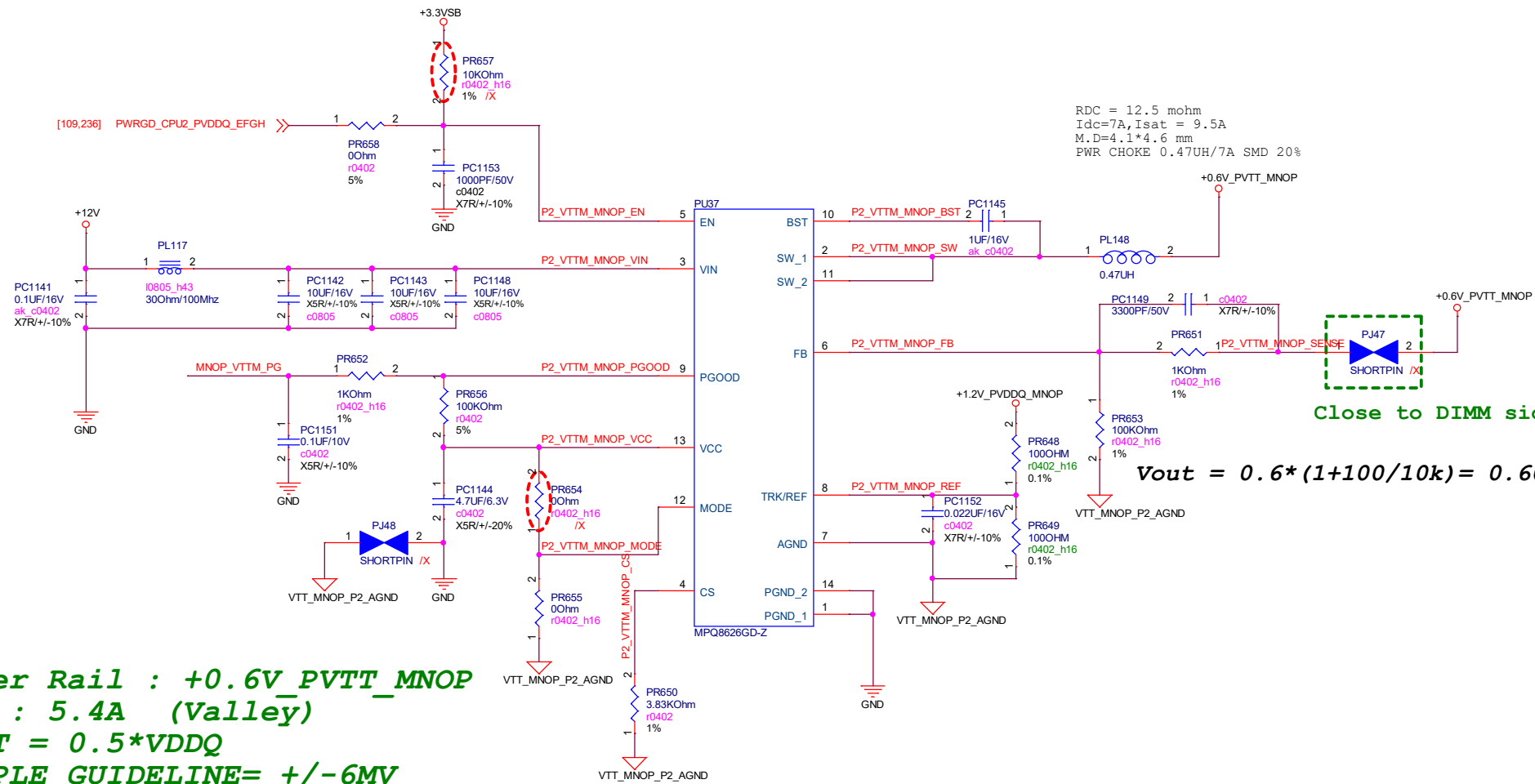
EFPH DIMM  
PMBus address: 5B/B6  
Config ID: 3  
SVID Bus: BUS#2  
SVID address: 00h  
Protocol ID: 07h

PVDDQ SPECIFICATIONS:  
VBOOT = 1.2V  
IOUT STEP = 98.5A@11.6A/us  
IOUT PEAK = 118A  
IOUT TDC = 118A  
  
RIPPLE GUIDELINE = +/- 6mV  
DC TOL = +/- 6mV  
AC & DC TOL = +60mV/-40mV  
IOUT DI/DT = 19.5A/us  
  
VPVP SPECIFICATIONS:  
VOUT = 2.575V  
IOUT TDC = 8.8A  
IOUT PEAK = 11.87A  
IOUT STEP = 7.06A  
  
RIPPLE GUIDELINE = +/- 25mV  
DC TOL = +/- 38mV  
AC & DC TOL = +137mV/-127mV  
IOUT DI/DT = 28.6A/US





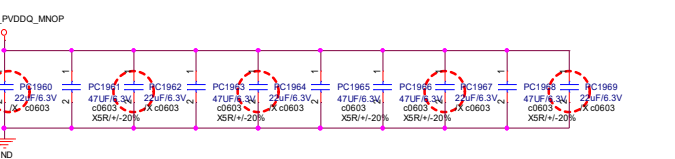
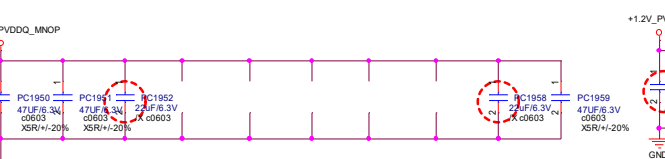
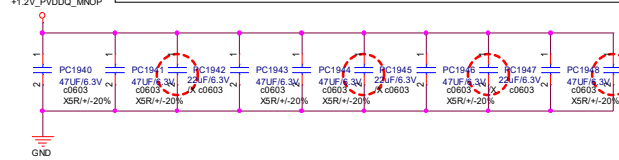
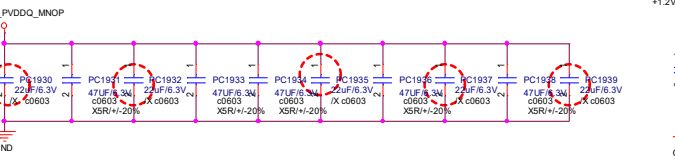
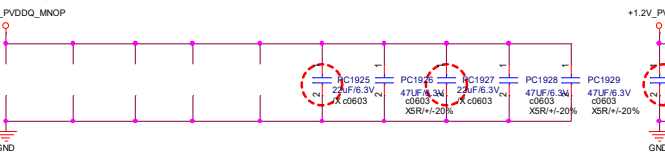
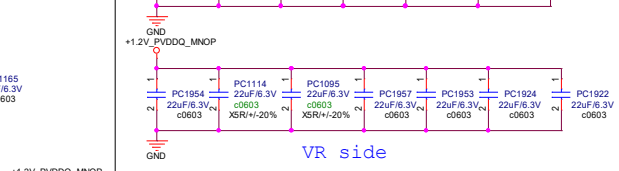
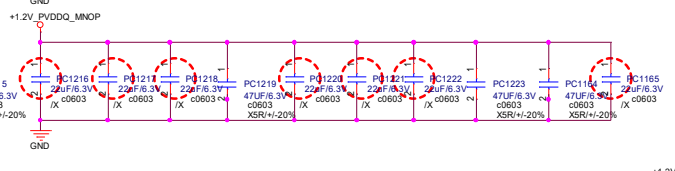
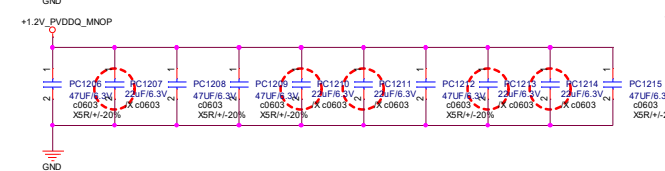
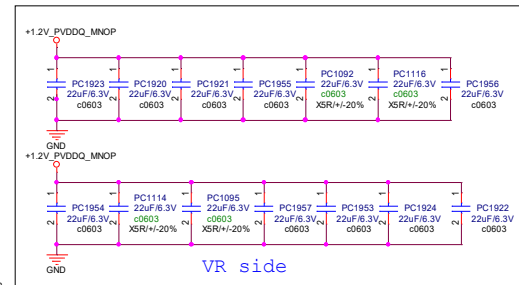
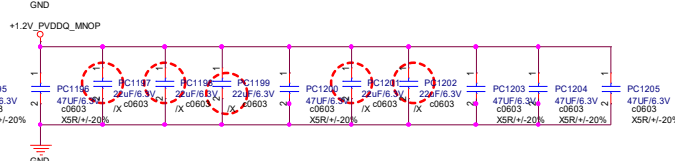
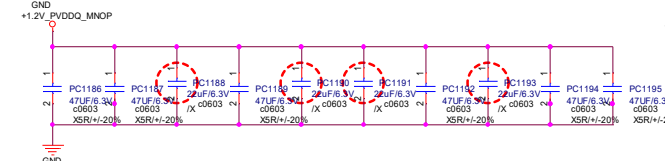
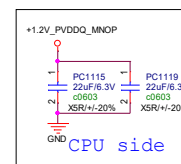
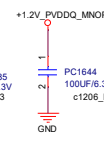
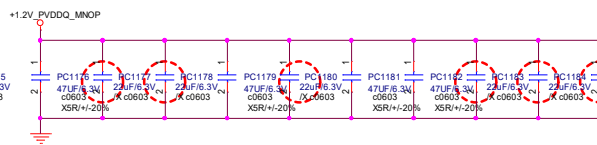
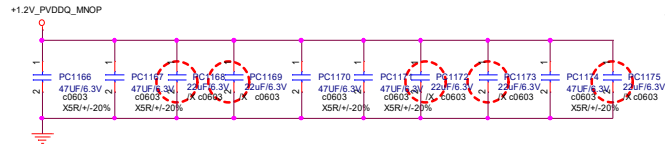
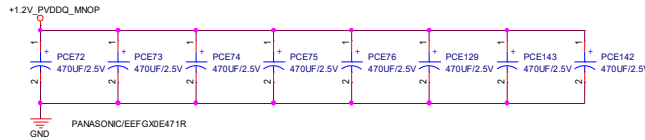
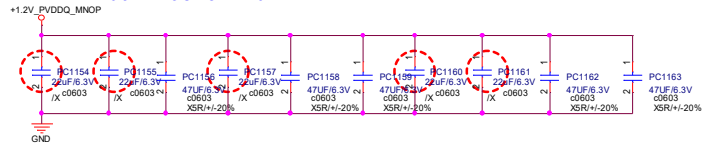
5					4					3					2					1																																																																																														
D																																																																																																																		
C																																																																																																																		
B																																																																																																																		
A																																																																																																																		
																				<table><tr><td colspan="5">Title</td></tr><tr><td colspan="5">238. MNOP_SPS_VPPM(TDA21462)</td></tr><tr><td>Size</td><td colspan="20">Document Number</td><td>Rev</td><td colspan="3" rowspan="2">&lt;RevCode&gt;</td></tr><tr><td>Custom</td><td colspan="20">&lt;Doc&gt;</td><td colspan="4"></td></tr><tr><td>Date:</td><td colspan="17">Tuesday, March 14, 2023</td><td>Sheet</td><td>238</td><td>of</td><td>253</td><td colspan="3" rowspan="2"></td></tr></table>					Title					238. MNOP_SPS_VPPM(TDA21462)					Size	Document Number																				Rev	<RevCode>			Custom	<Doc>																								Date:	Tuesday, March 14, 2023																	Sheet	238	of	253								
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238. MNOP_SPS_VPPM(TDA21462)																																																																																																																		
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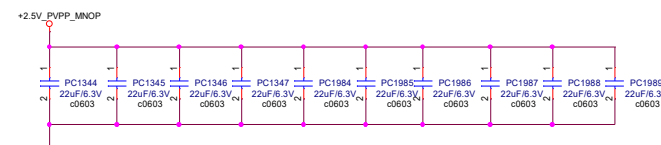
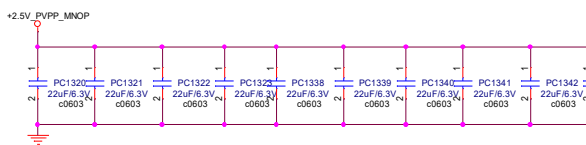
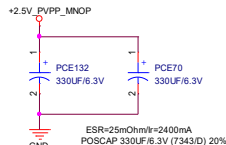
**Power Rail : +0.6V\_PVTT\_MNOP**  
**OCF : 5.4A (Valley)**  
**VOUT = 0.5\*VDDQ**  
**RIPPLE GUIDELINE= +/-6MV**  
**DC TOL= +/-9MV**  
**AC & RIPPLE = 0.642V/0.564V**  
**IOUT TDC = +/- 2.27A**  
**IOUT STEP = 3.7A**  
**IOUT DI/DT = 8A/US**  
**Freq : 1MHz**

Title		
239. MNOP_POL_VTTM(TPS53317)		
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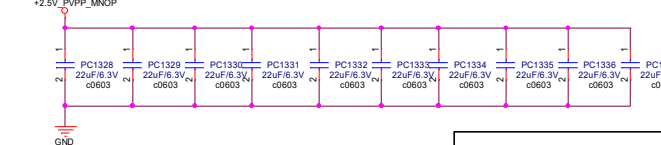
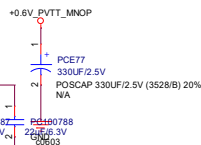
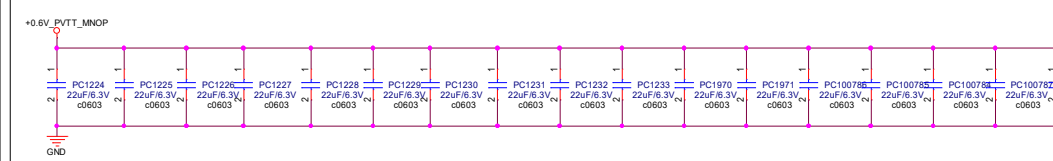
VCCM total Cap  
22uF/6.3V/0603/X5R \*120  
470uF POS-CAP\*6



VPP total Cap  
22uF/6.3V/0603/X5R \*30  
330uF POS-CAP\*2



VTTM total Cap  
22uF/6.3V/0603/X5R \*17  
330uF POS-CAP\*1

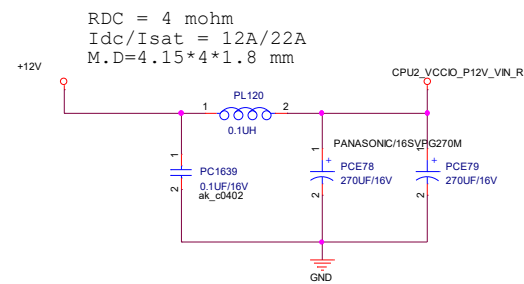
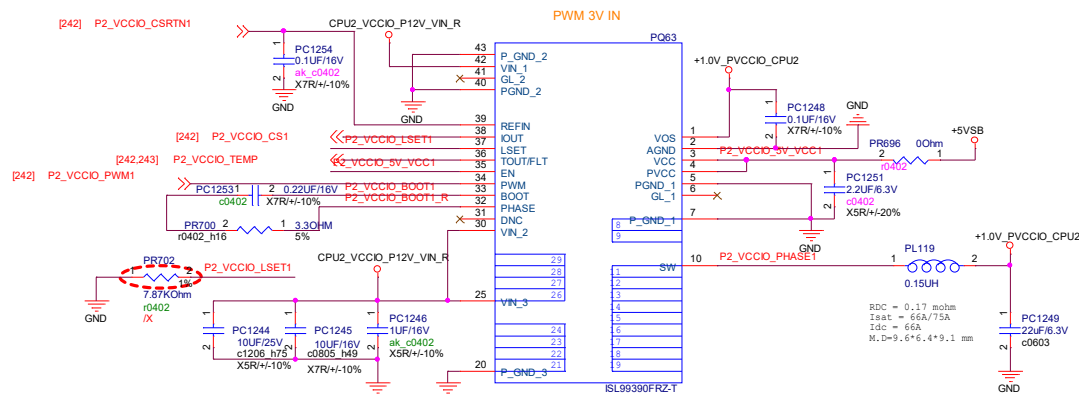


File	240. MNOP_CAP_VCCM+VPP+VTT		
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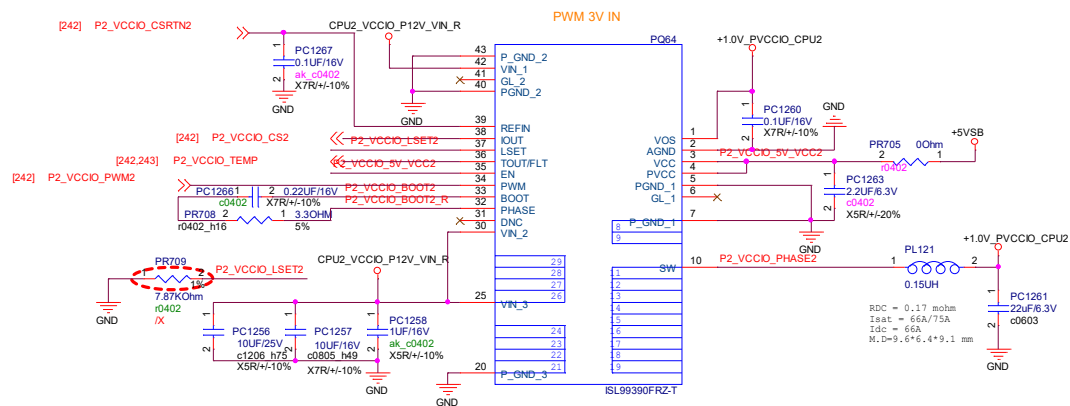




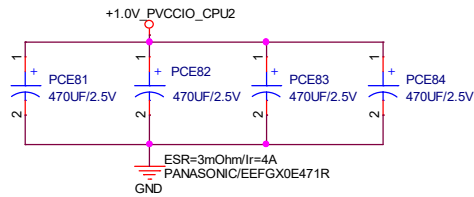




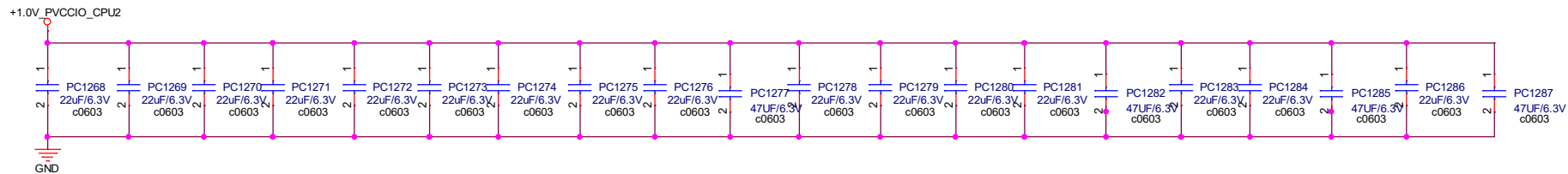
RDC = 4 mohm  
Idc/Isat = 12A/22A  
M.D=4.15\*4\*1.8 mm



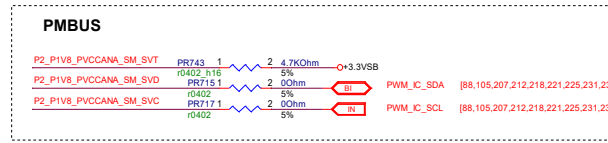
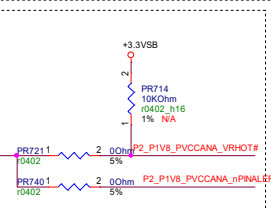
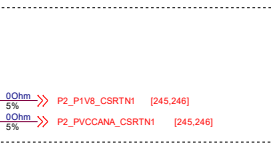
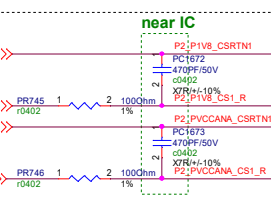
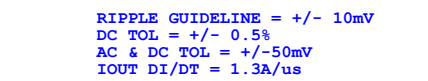
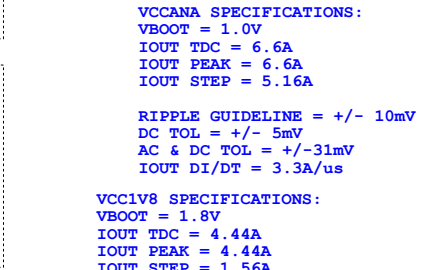
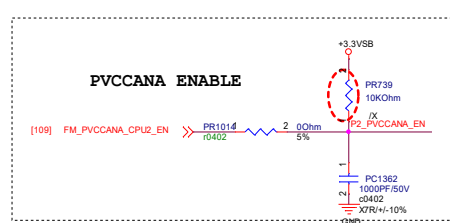
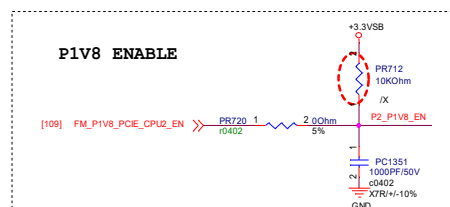
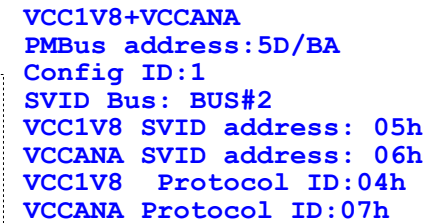
Title			243. CPU2_SPS_VCCIO(TDA21462)
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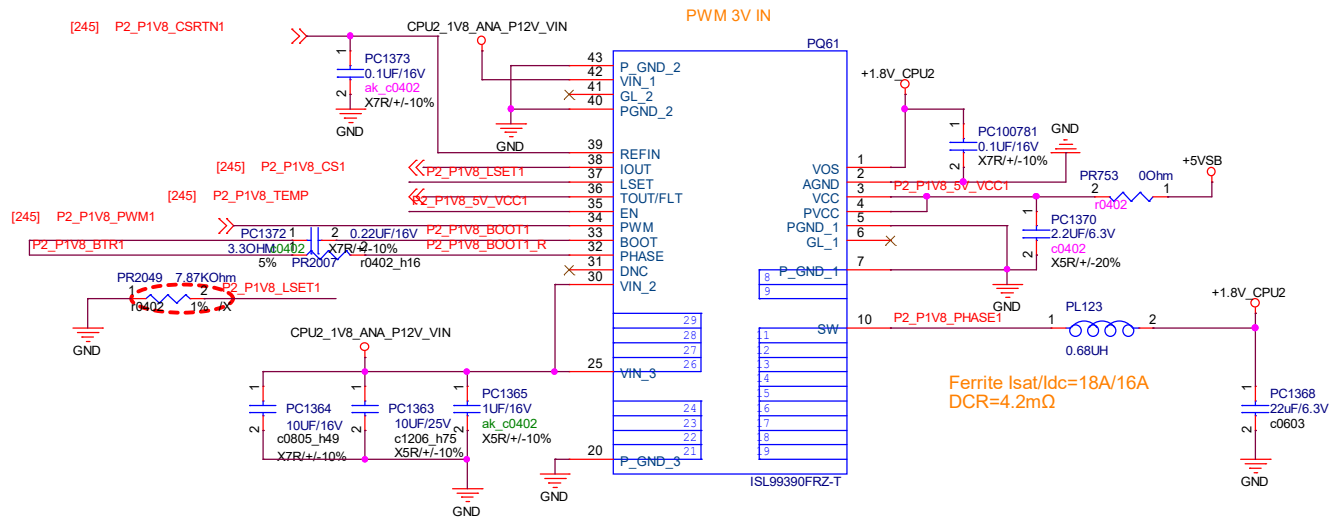


VCCIO total Cap  
22uF/6.3V/0603/X5R \*10  
470uF POS-CAP\*4

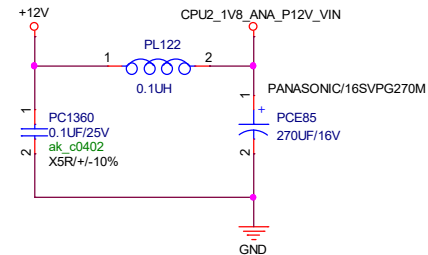


Title		
244. CPU2_CAP_VCCIO		
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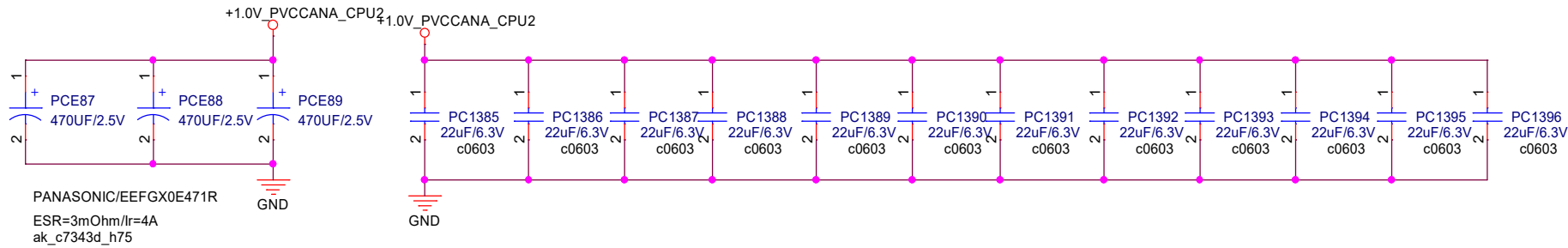
RDC = 4 mohm  
 Id<sub>c</sub>/I<sub>sat</sub> = 12A/22A  
 M.D=4.15\*4\*1.8 mm



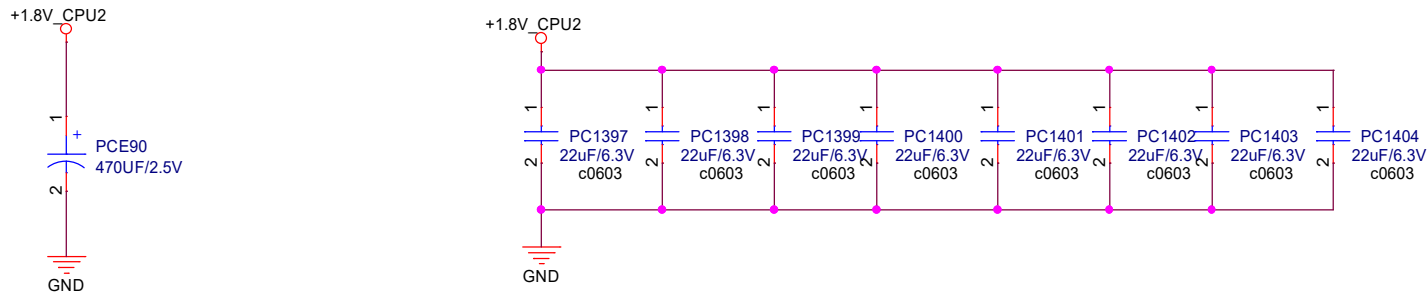
Title		
246. CPU2_SPS_VCC1P8(TDA21462)		
Size	Document Number	Rev
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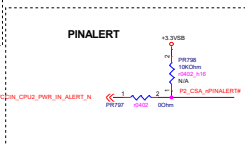
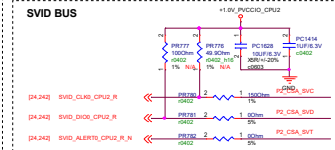
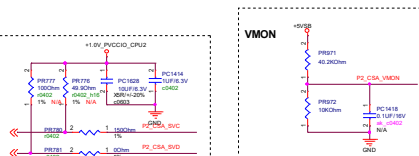
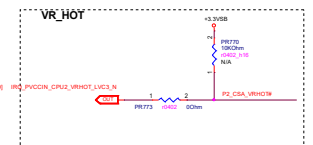
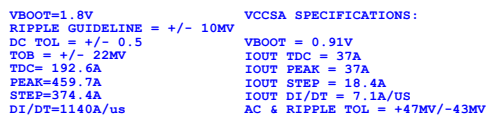
PVCCANA total Cap  
 22uF/6.3V/0603/X5R \*12  
 470uF POS-CAP\*3



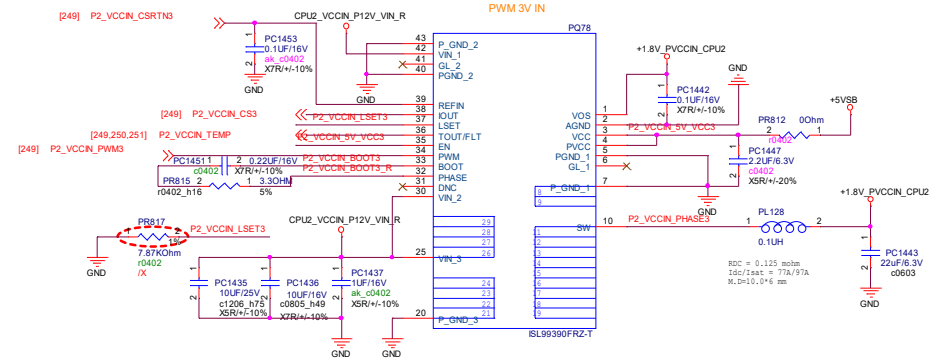
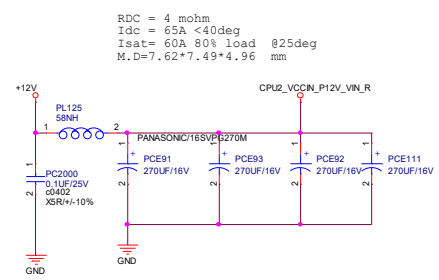
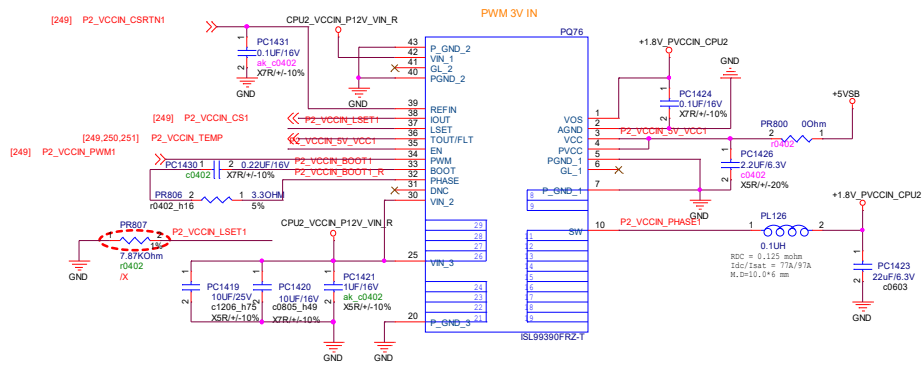
VCC1V8total Cap  
 22uF/6.3V/0603/X5R \*8  
 470uF POS-CAP\*1



Title			
248. CPU2_CAP_VCC1V8+VCCANA			
Size	Document Number		Rev
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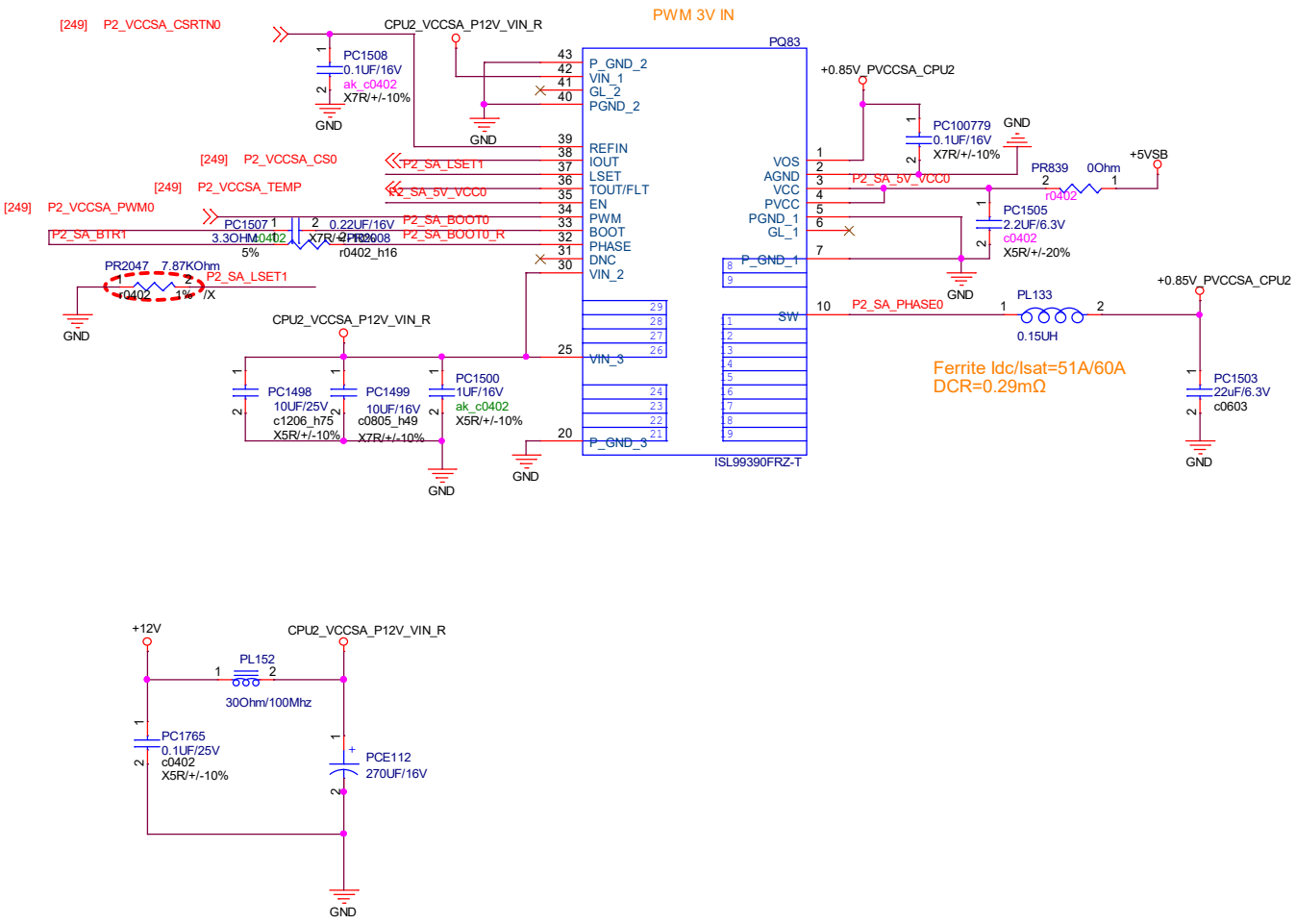


RDC = 4 mohm  
 Idc = 65A <40deg  
 Isat = 60A 80% load @25deg  
 M.D=7.62\*7.49\*4.96 mm

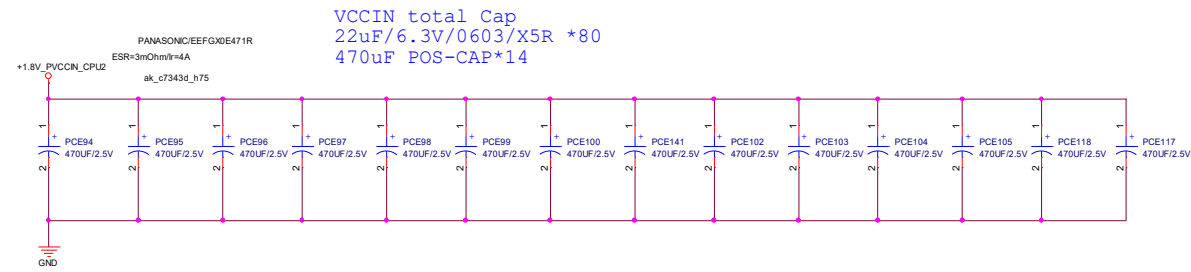


File	250. CPU2_SPS1-3_VCCIN.TDA21400
Rev	1
Doc Number	250. CPU2_SPS1-3_VCCIN.TDA21400
Outline/Doc	250. CPU2_SPS1-3_VCCIN.TDA21400
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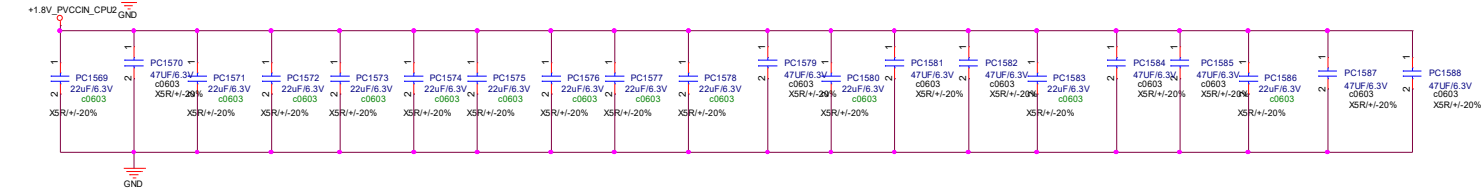
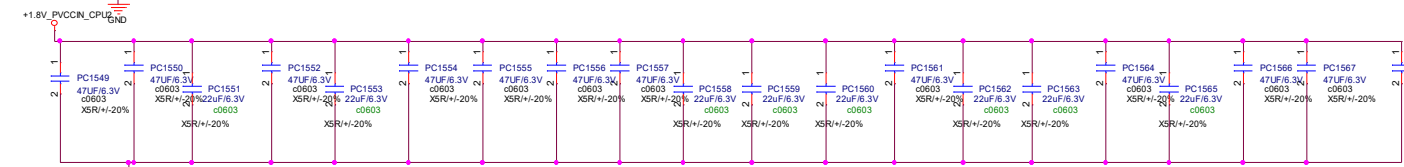
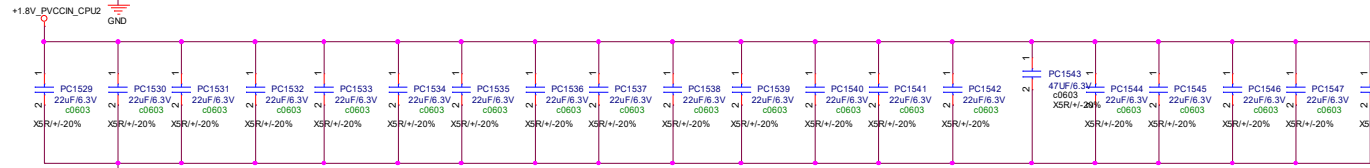
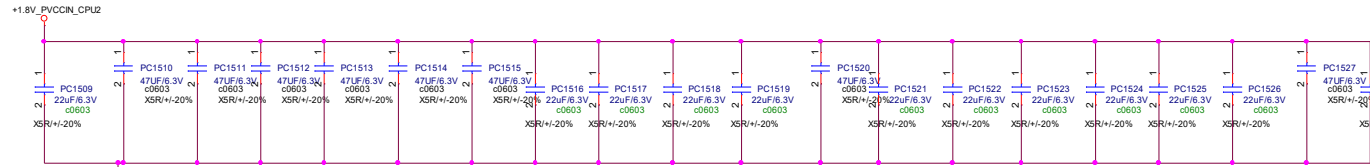




Title		
252.CPU2_SPS_VCCSA(TDA21462)		
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VCCIN total Cap  
 22uF/6.3V/0603/X5R \*80  
 470uF POS-CAP\*14



VCCSA total Cap  
 22uF/6.3V/0603/X5R \*15  
 470uF/2.5V\*2

