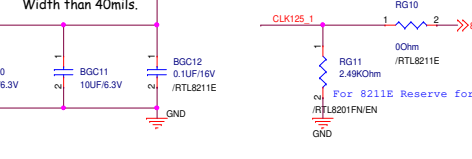
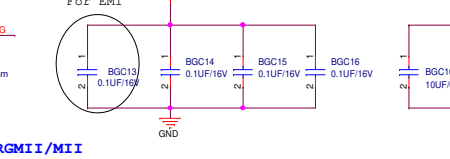
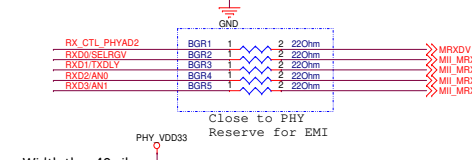
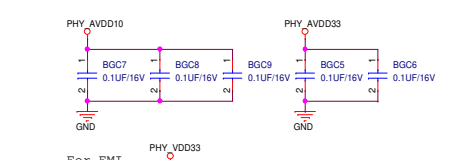
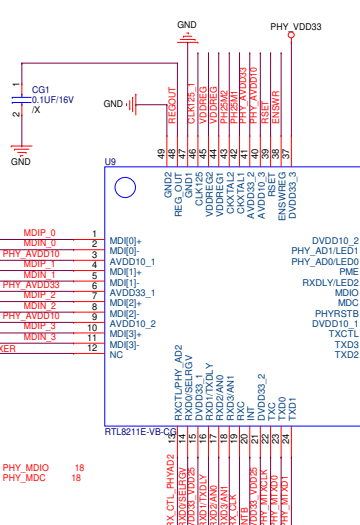
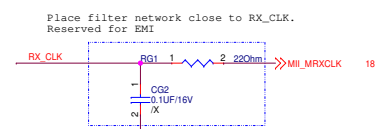
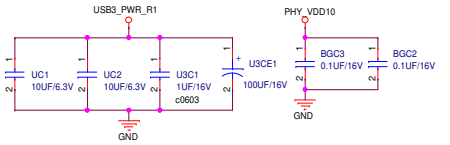
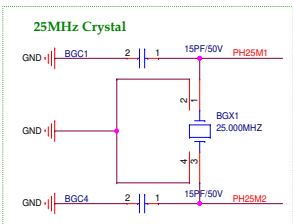
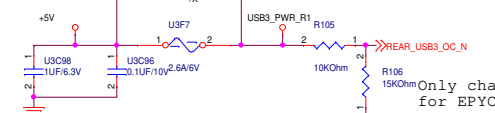
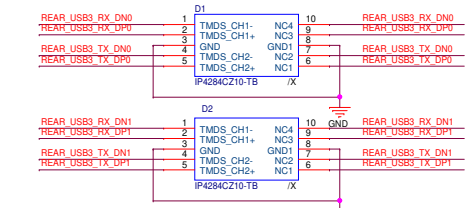
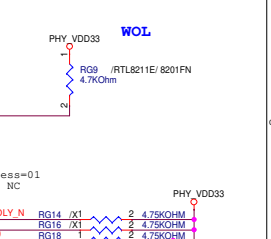
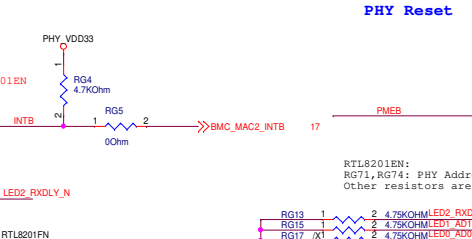
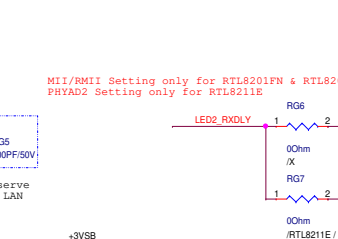
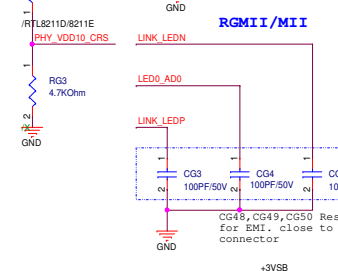
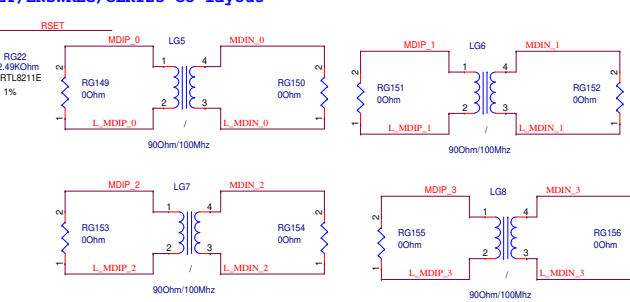


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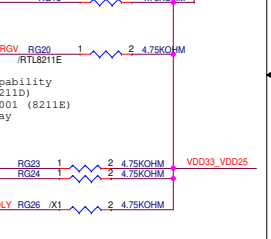
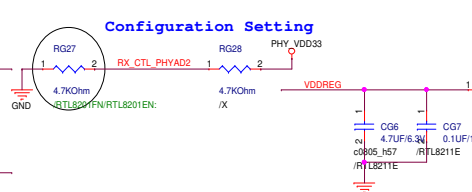


PHY_MRXCLK	18
PHY_MTXCLK	18
PHY_MTXEN	18,20
PHY_MTXD0	18,20
PHY_MTXD1	18,20
PHY_MTXD2	18,20
PHY_MTXD3	18,20
PHY_MTXD4	18,20
PHY_MTXD5	18,20

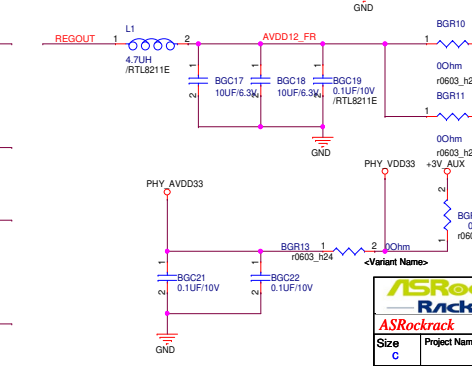
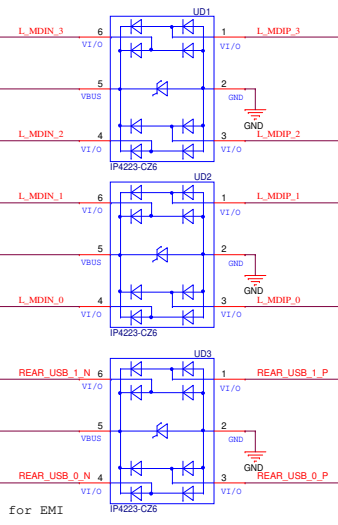
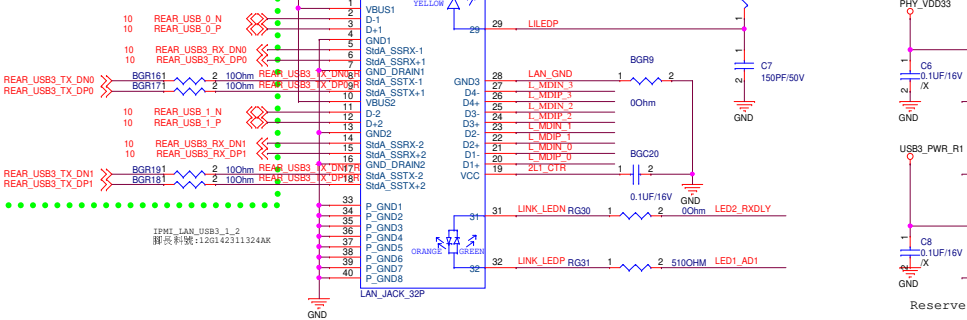
RSET/ENSWREG/CLK125 Co-layout



Only change to 07G028069010AK for EPYCD8 R1.00 BOM (20170927)

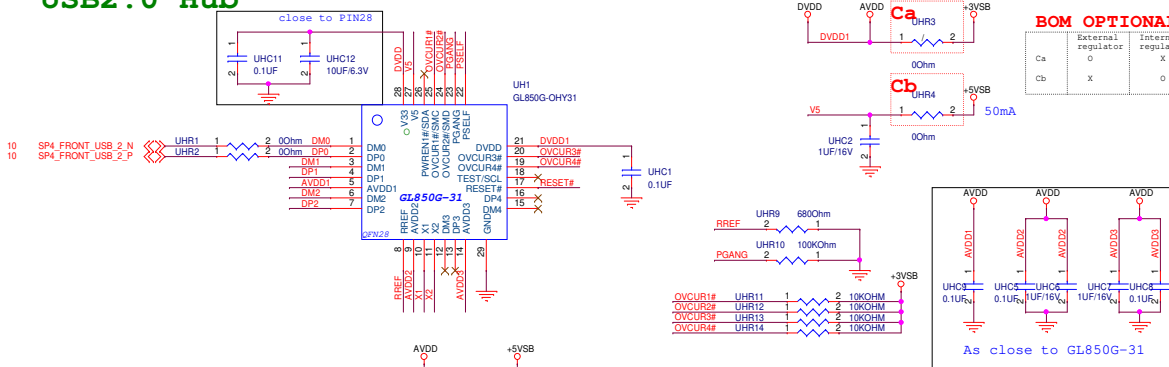


R1.01 Modify



ASRock Title : 035_IPMI_LAN_8211E
ASRock Engineer: Rex-Chang
 Size C Project Name EPYC3000D4I-2T Rev R1.00
 Date: Tuesday, January 26, 2021 Sheet 35 of 82

USB2.0 Hub

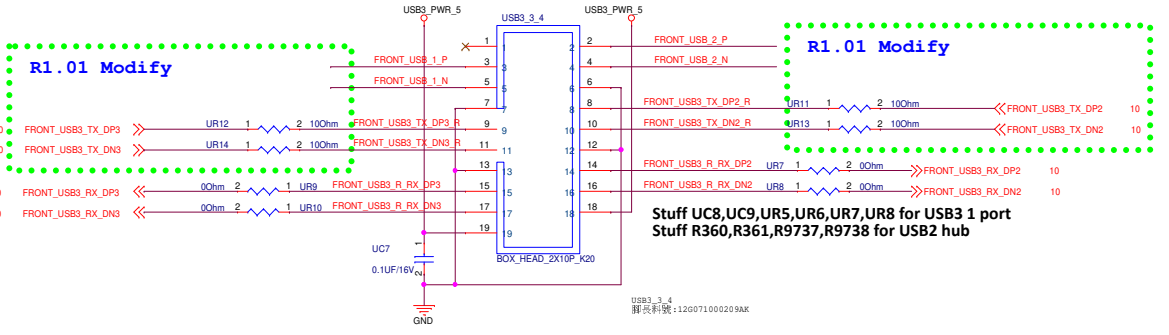
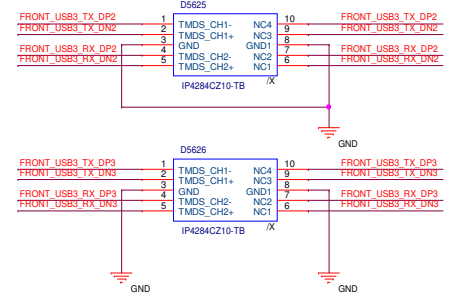
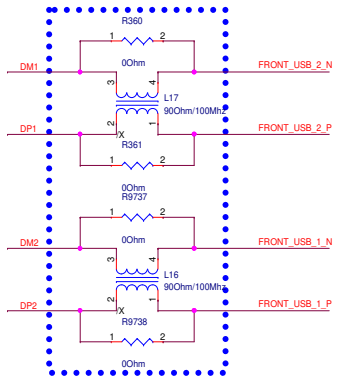
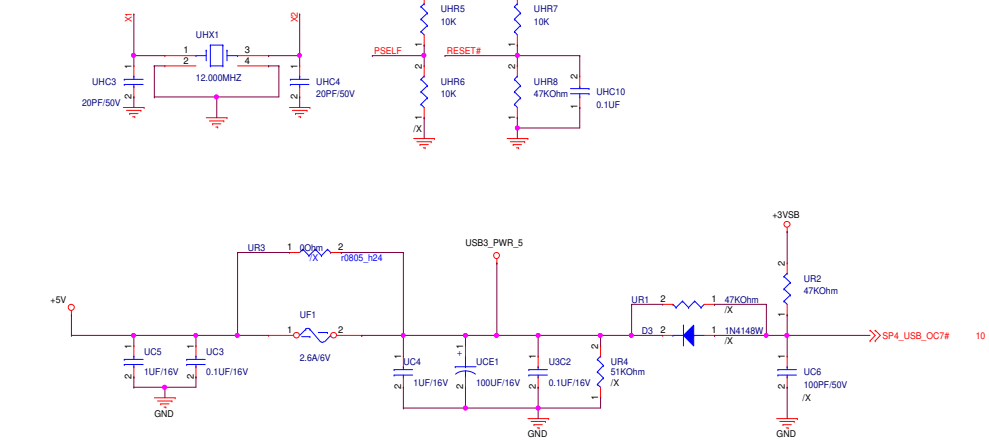


Work port number	I/O Strapping
1 (port1)	DP2,DM2 pull high
2 (port1/2)	DP3,DM3 pull high
3 (port1/2/3)	DP4,DM4 pull high

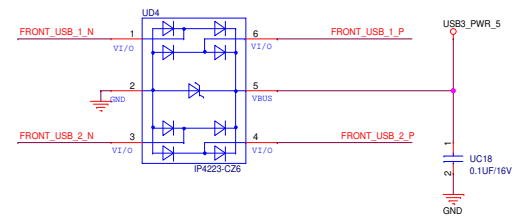
BOM OPTIONAL		
	External regulator	Internal regulator
Ca	o	x
Cb	x	o

OVCUR[1..4]#	Non-removable Configuration of Portn
Floating	Non-removable
Pull High	Removable

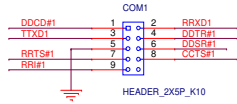
PSELFP	Mode
H	self-power (support 0.5A device)
L	Bus-power (support 0.1A device)



Stuff UC8,UC9,UR5,UR6,UR7,UR8 for USB3 1 port
Stuff R360,R361,R9737,R9738 for USB2 hub



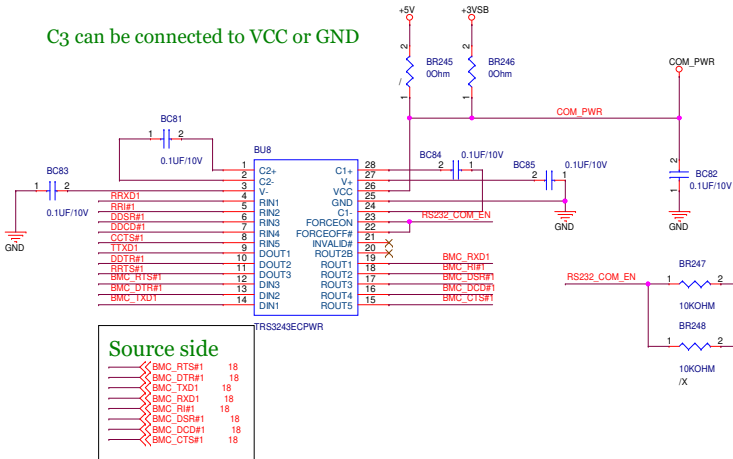
COM Port



V_{CC} vs CAPACITOR VALUES

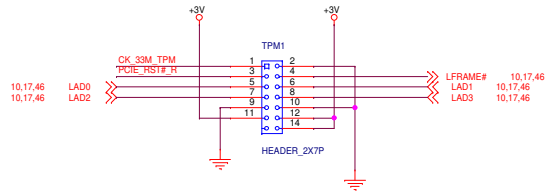
V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

C3 can be connected to VCC or GND

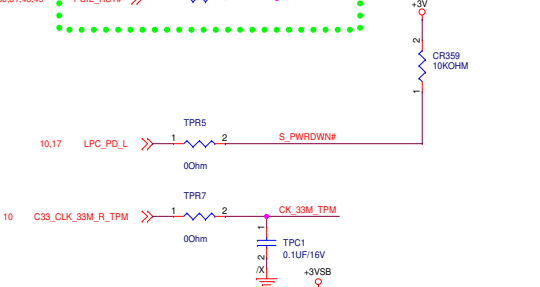
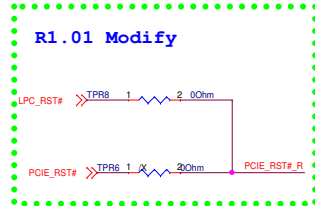
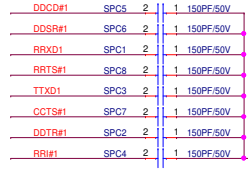
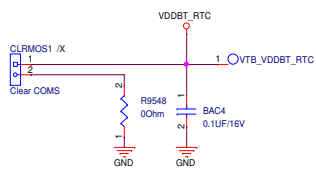


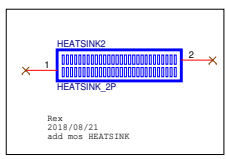
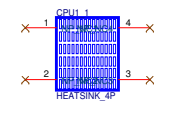
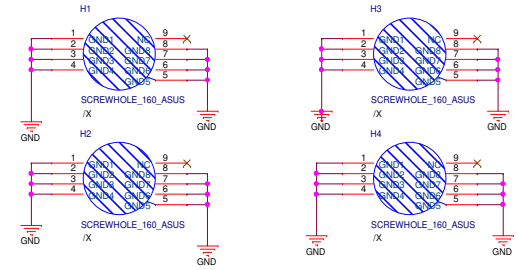
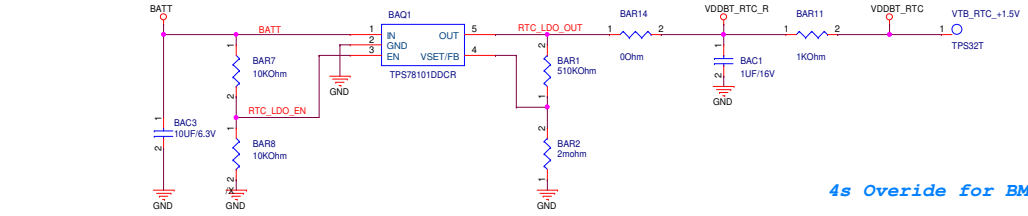
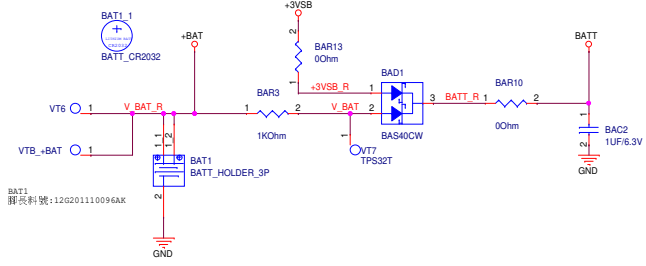
Source side

- BC83
- BC81
- BC84
- BC85
- TPM1
- COM1

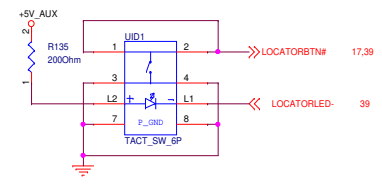
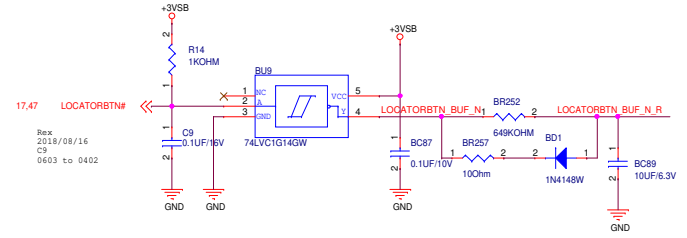
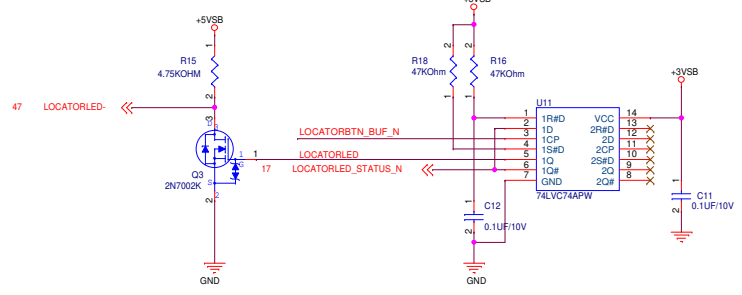


CLRCOMS BTN





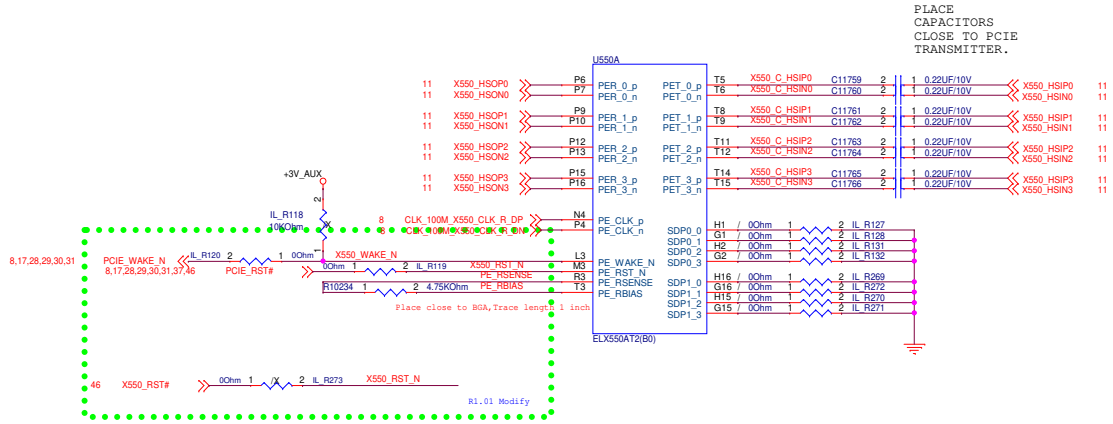
4s Override for BMC reset



<Variant Name>

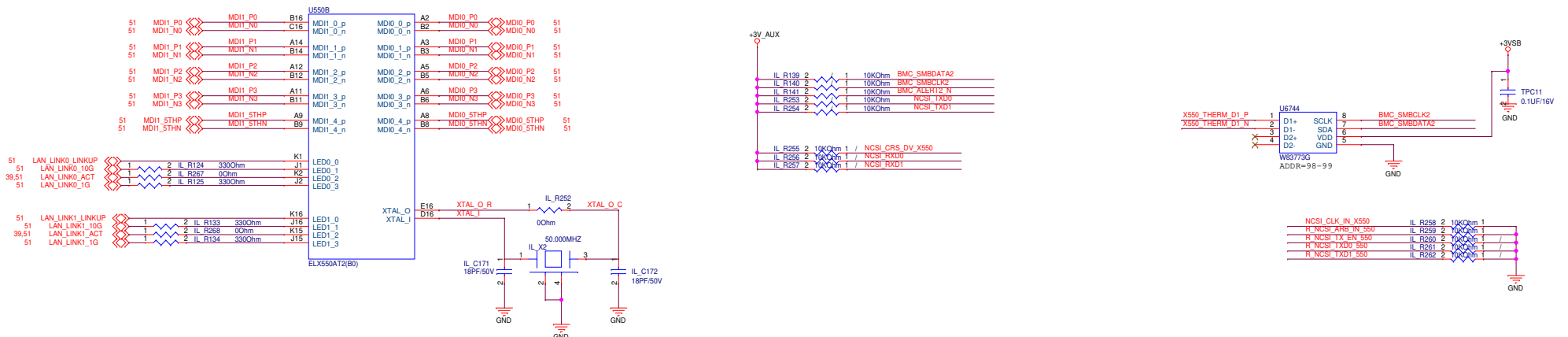
ASRock		Title : 048. MECHANICAL & Battery	
ASRock		Engineer: Rex-Chang	
Size	Project Name	Rev	
C	EPYC3000D4I-2T	R1.00	
Date: Tuesday, January 26, 2021		Sheet 48 of 82	

PAGE 1 - X550-AT2 PCIE

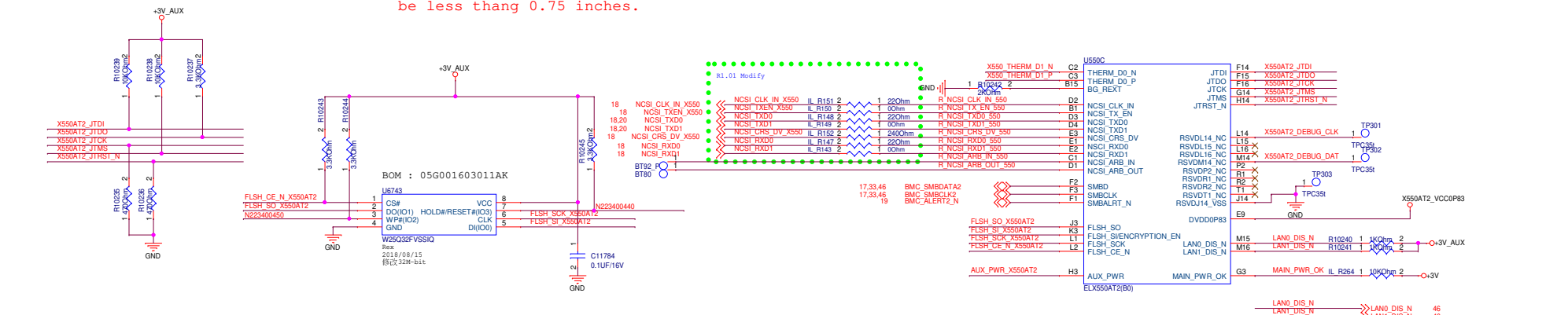


PLACE CAPACITORS CLOSE TO PCIE TRANSMITTER.

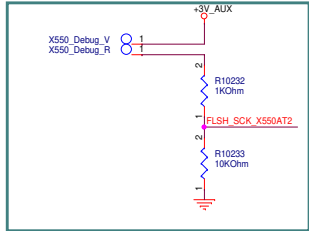
<Variant Name>



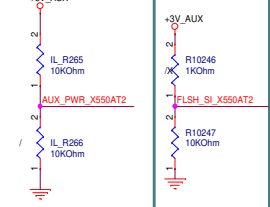
Trace length should be less than 0.75 inches.



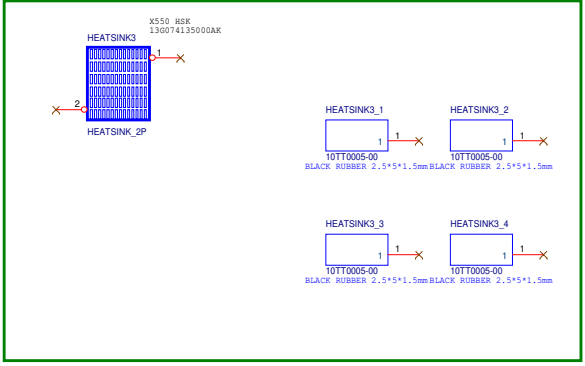
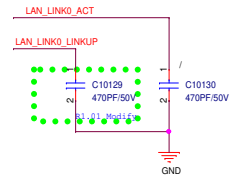
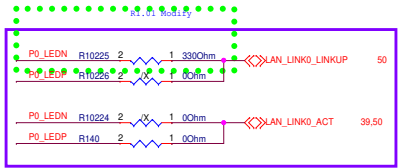
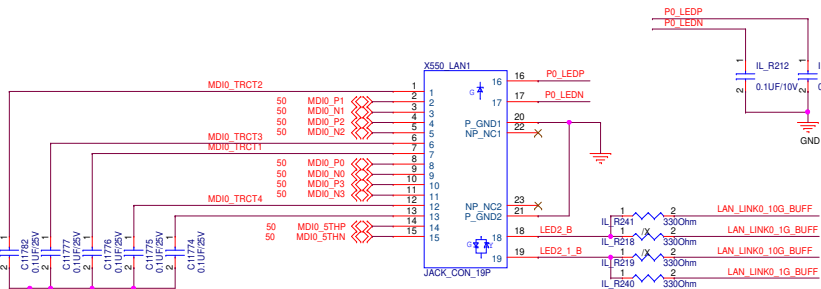
X550AT2 debug mode



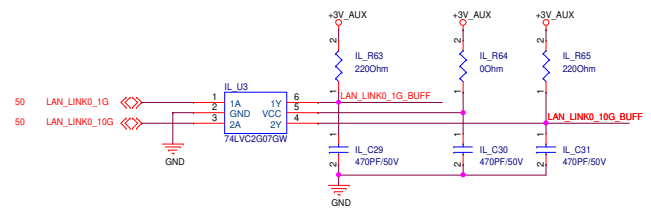
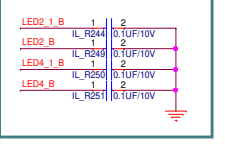
X550AT2 IPSEC Strapping Option



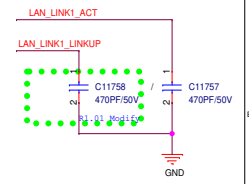
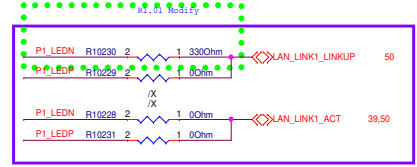
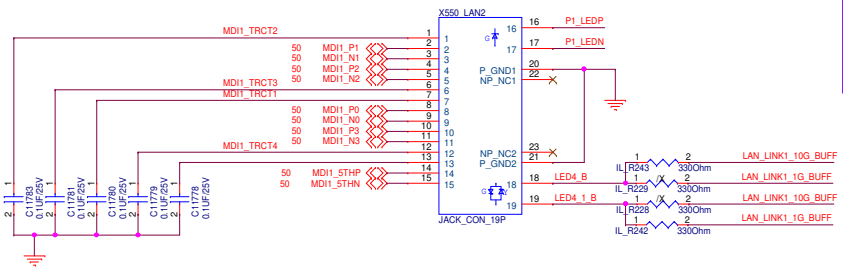
DISCRETE - PORT 0



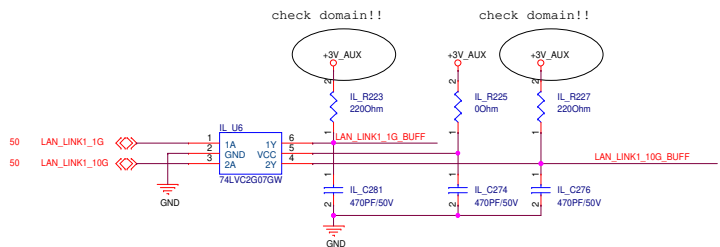
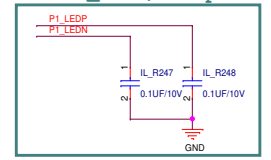
EP2C621D16GM R1.02
Add Speed LED Cap



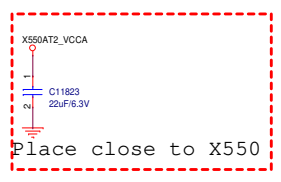
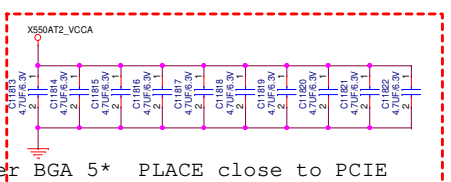
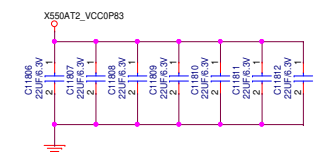
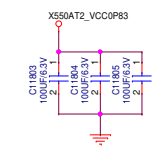
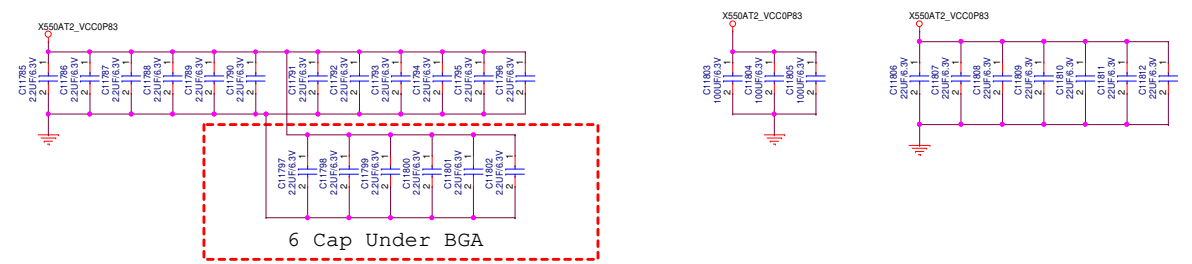
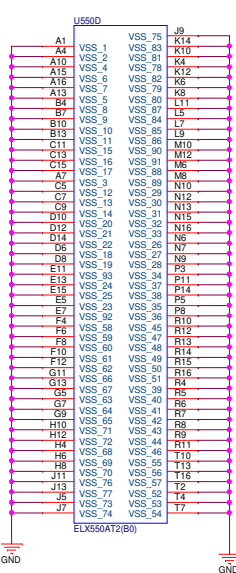
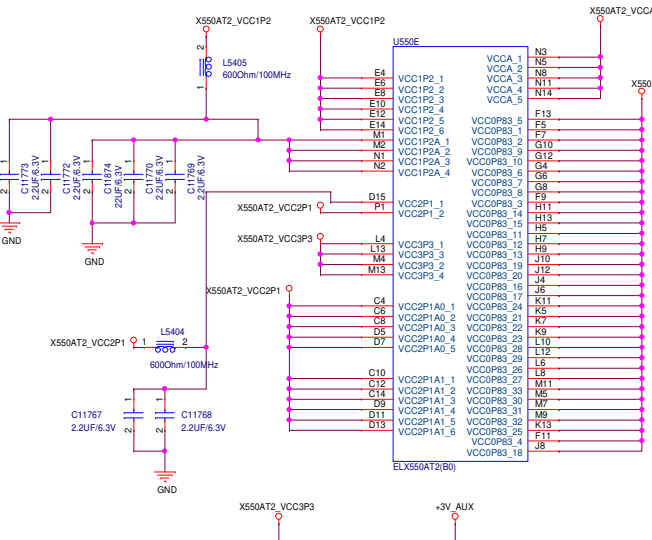
DISCRETE - PORT 1



EP2C621D16GM R1.02
Add P1_LEDP/N Cap



X550-AT2 POWER SUPPLIES:
 X550AT2_VCC1P2,
 X550AT2_VCC0P83,
 X550AT2_VCCA,
 X550AT2_VCC2P1,
 X550AT2_VCC3P3



Under BGA 5* PLACE close to PCIe

