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AMD Serial VID Interface Version 3 (SVI3) Specification

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Revision History

Date	Revision	Description
October 2022	2.00	Updated the following: • Included IL (Inclusive Language) master->controller/slave->target • Section 1.2. Added bullet for SVI3_RESET_L and SVI3_VDDIO information. • Section 3.5. Updated Figure 2 and Figure 3 with correct reference points for setup and hold parameters. • Updated Figure 1. SVI3 Interface Topology, Figure 2, SVC/SVD Timing, and Figure 3. SVC/SVT Timing. • Table 6, SVI3 Interface Timing Requirements. Changed SVI3_RESET_L assertion time min from 10 to 100. • Section 4.4.1. Bus Initialization. Updated item 3. • Section 4.4.2, Target Enumeration and Addressing. Added "3-bit CRC" to list item number 5. • Section 4.8.6, Acknowledgement Example. Changed to “with CRC verification." • Updated Table 10, Type 1 Target Required Signals and Table 11, Type 1 Target Electrical Requirements, • Updated Figure 10. Telemetry Pipeline Example (Part 1), Figure 11. Telemetry Pipeline Example (Part 2), and Figure 12. Telemetry Pipeline Example (Part 3). • Table 14. Power-up Sequencing Requirements. Updated $T_{VCC\text{-}EN}$, and $T_{STARTUP}$, and removed note 1. • Table 23, Type 1 Power States. Updated PSI 1, 2, and 4. • Added Section 5.7.1, Fault Avoidance During Power States PSI1-PSI4. • Section 5.8, Output Voltage Regulation Disabled States. • Table 24, Voltage Regulation Disabled States. Added “VID = OFF” mode. • Figure 20, Current Sensing Topology Example. • Added Table 26, Type 1 Output Current Scaling Selections. • Updated Table 32, Input Current Scaling Selections, Table 33, Input Voltage Scaling Selection, Table 36, Read-Only Registers. • Added Section 5.10.7, System Power (Telemetry Reg. Index 110b) *Optional*. • Added Table 36, System Power Scaling Selection. • Updated Table 37, Read-Only Registers and Table 39, Read/Write Registers. • Added P_SYS_SCALE to Table 37. • Updated Table 51, Type 2 Output Current Scaling Selections, Table 53, Read-Only Registers, and Table 55, Read/Write Registers. • Incorporated general edits.

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Date	Revision	Description
June 2020	1.01	-Section 4.4.2: Added clarification statement that 3-bit CRC packet is expected for initialization command. -Section 4.5.5.1: Added clarification statement that the execution of initialization procedure does not reset/modify any SVI3-defined registers. -Section 4.5.7: Added note that for all invalid commands, targets shall assume an 8-bit packet length for the purposes of framing. -Table 14: T_Startup definition is now referenced from PWR_ENABLE assertion, not VCC. -Section 5.9: Added clarification that the toggling of PWR_ENABLE does not clear sticky FAULT_STATUS bits. -Sections 5.12.2 and 6.12.2: Added clarification that FAULT_STATUS bits cannot be cleared if the fault condition still exists. -Section 6.6: Added load-line section for Type 2 targets to maintain numbering consistency. -Appendix A: Updated URC, condition 5. Added command "000b". -Appendix A: Updated NENS, condition 19, "Every target that reports error". -Section 5.9.2: Added statement that OCP_L pin will latch asserted following an OCP fault. -Miscellaneous edits.
July 2019	1.00	-Section 5.5.2: Added content. -Table 19: TVOT parameter updated to TVOTF. -Table 21 and Table 30: Added the word “Controller “to the heading of second column. -Section 5.9.5.1: Added OVP: VOTF and Pre Bias Voltage section. -Section 5.9.6.1: Added UVP During VOTF section. -Table 36: Added additional bits for Addr 02. Changed Addr 02 [7:0] to Addr 02 [4:0]. -Chapter 6: Added new chapter. -t_{low} (min) changed to 12 ns. -Added timing parameter $T_{rise/fall\_SVT}$ + $t_{launch-Target}$ = 6 ns (max). -Separated $T_{VCC-SVC\_START}$ and $T_{VDDIO-SVC\_START}$. -Changed $T_{VDDIO-SVC\_START}$ to 1 ms (max). -Added new timing parameter $T_{VDDIO-SVI3\_POR}$ to clarify power-on reset timing requirements. -Added comments to 5.5.2 regarding Negative VOTF undershoot and VOTF commands while voltage is transitioning. -Added "It is not required that SVI3 controllers support the entire temperature range from -40°C to 125°C." to Table 21.
March 2019	0.94	-Added new timing constraint t_{RESET_L} in Table 6 -CRC is now enabled by default -Added Figure 9 which depicts the SVTI/SVTO pipeline latency -Changed terminology of "BOOT" Voltage and "BOOT slew rate to "Default" Voltage and "Default" slew rate -Modified Table 14 for consistency and clarity

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Date	Revision	Description
		-Fixed error: The reaction time delay to assert the OCP_L pin after the inductor current exceeds the OCP_WARN_THRESH is equal to OCP_WARN propagation delay. -Corrected Figure 18 to show that OCP_L pin should be driven by latched OCP fault. -Added Appendix of NACK conditions.
January 2019	0.93	-Changed “VIO” to VDDIO in Table 5 -Added note 7 in Table 6 -Added rule 6 in 4.4.2 -Fixed Figure 7 -Added notes to 4.5.5.3 and 4.5.5.4: “However, if a target receives a CRC enable/disable command after a Telemetry Request packet and before it reports its telemetry, the target shall enqueue the command until reporting is complete.” -Added additional communication error conditions in 4.8.1.3: Command before ACK -Added section 4.8.2: NACK and Command Execution -Added clarification in 4.8.4.1 that terminal target will finish reporting it packet (including start and header packets) before sending an incomplete acknowledge -Added note in 4.8.4.2: *Note: If the reporting target is also an ACK Target, it will modify the buffered acknowledgment packet, as per section 4.8.3.3.* -Changed items 2 and 3 for 5.4 -Removed VID_MAX and VID_MIN as values that are modified by an offset change in Section 5.5.4 -Change Input Voltage Scale 1 to Scale 2 in Table 33 -Added Note 3 in Table 34: For temperatures below -40°C, the regulator shall report –40°C. -Added Richtek in MFG_ID register description in Table 36 -Added that CRC_ENABLED is disabled by default in Table 36 -Restructured register 20 in Table 36 -Changed default description for register 28 and 29 in Table 36
November 2018	0.92	Initial Preliminary NDA release.

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Chapter 1 Overview

The Serial VID Interface Version 3 (SVI3) is designed to provide a scalable single-controller, multi-target communication bus for power management on Advanced Micro Devices (AMD) platforms. The purpose of this specification is to describe the interface's physical and protocol layers. In addition, the specification provides design criteria for the various classes of power management devices that may be present on the interface.

The interface can be applied to various power management devices such as multi-phase Buck converters, single-phase point of load (POL) devices, integrated on-package micro converters, boost converters, intermediate bus resonant converters, system power monitoring devices, etc. To facilitate future expansion and to provide clarity, the specification is split into two main sections:

1. **Physical layer and protocol layer (Chapters 1-4):** This section only pertains to the communication between the controller and various target devices. Pin and I/O requirements will only pertain to those relevant to the SVI3 interface.
2. **Device class specific (Chapter 5 and beyond):** This section provides criteria pertaining to specific device classes. Examples of device specific information include VID tables, regulation requirements, telemetry accuracy, etc. Pin and I/O requirements only pertain to those relevant to the specific device class.

1.1 What is Included

The specification includes minimum design criteria for the controller and all target devices on the SVI3 bus. It also provides a complete description of the physical and protocol layer of the bus.

1.2 What is Not Included

The specification covers all of AMD's business sectors including, but not limited to, client, server and graphics. As such, this specification does not include system-level application-specific design criteria.

For example:

- The specification stipulates that each voltage regulator has a PWR_ENABLE pin but does not specify the proper system-level connection of this signal.
- The specification does not indicate the correct system-level connection of SVI3_RESET_L or SVI3_VDDIO signals/nets.
- The specification stipulates several power states for some regulator classes but does not describe the current threshold mapping of these power states.
- The specification does not specify current/power capability criteria for any specific platform or device-class.

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Such application-specific information can be found in ASIC data books, design guideline/checklist documents and infrastructure roadmaps.

1.3 Deviations from SVI2

SVI3 represents a major deviation from SVI2 and all previous AMD power management interfaces.

Similarities include:

- Single-controller interface
- 3-wire push-pull signaling (from the controller)
- Dedicated telemetry bus

Major differences include (but are not limited to):

- Multi-target interface with explicit addressing
- Daisy-chain telemetry topology
- Direct register read/write functionality

SVI3 is not designed to be backwards compatible with SVI2. It is not required for SVI3 devices to be able to function on an SVI2 bus. However, advanced target devices may include the ability to function in SVI2 mode.

1.4 Mandatory vs. Optional

Unless explicitly stated with the notation *optional*, it’s assumed that the enablement of all features described within the specification is mandatory for all SVI3-compliant devices.

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Chapter 2 Reference Information

2.1 Numerical Formats

All numbers are decimal unless otherwise specified with a suffix. Numbers with the suffix “b” are binary. Numbers with the suffix “h” are hexadecimal.

2.2 Bit Ordering

All SVI3 transmitted data is transmitted MSB first.

2.3 Glossary

This section describes the units of measure, acronyms, and SVI3 Specific Terminology

2.3.1 Units

Table 1 describes the units of measure and the abbreviations used in this document.

Table 1. Unit Description

Units	Description
°C	degrees Celsius
A	Ampere
Hz	Hertz
kHz	kilohertz
kSamp	kilo Samples
ms	millisecond
mV	millivolt
mΩ	milliohm
ns	nanosecond
pF	picofarad
µA	microampere
µs	microsecond
V	Volt

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2.3.2 Acronyms

Table 2 describes acronyms that are not otherwise described in the specification. Signal name and parameter acronyms are not located in this section.

Table 2. Acronym Descriptions

Acronym	Description
ACK	Acknowledgement
AMD	Advanced Micro Devices
ASIC	Application Specific Integrated Circuit
CRC	Cyclic Redundancy Check
DC	Direct Current
DCR	Direct Current Resistance
FIFO	First In First Out
I/O	Input/Output
IC	Integrated Circuit
MSB	Most Significant Bit
NACK	Negative Acknowledgement
NVM	Non-Volatile Memory
OCP	Over-Current Protection
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
POL	Point of Load
POR	Power-on Reset
PSI	Power State Indicator
SVI2	Serial Voltage Identification Interface Version 2
SVI3	Serial Voltage Identification Interface Version 3
UVP	Under-Voltage Protection
VID	Voltage Identification
VOTF	Voltage-on-the-Fly
VRHOT	Voltage Regulator Hot

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2.3.3 SVI3 Specific Terminology

Table 3 lists the Specific Terminology Definitions for SVI3.

Table 3. SVI3-Specific Terminology Definitions

Term	Definition
ACK Target	A target that is required to return an ACK or NACK.
Acknowledgement Packet	A packet that contains an ACK or NACK code.
Command Packet	Any packet initiated by the controller on the SVD bus.
Command Packet Streams	A sequence of back-to-back command packets which occur without returning the SVD bus to idle. Only one acknowledgement packet is required per command packet stream.
Idle Transmit Mode	The terminal target transmits 1b on its telemetry output.
Incomplete Acknowledgement	An acknowledgement packet that was created by the terminal target, which has not been modified by an ACK target.
Controller	The device which drives SVC and SVD.
Pipeline Mode	A target pipelines data from its telemetry input to its telemetry output.
Reporting Target	The target that is presently reporting telemetry in the daisy-chain.
Selected Target	The target that was last selected by an Address packet or a VID packet.
Target	An addressable entity on the SVI3 interface. For voltage regulators, a target corresponds to a voltage rail.
Start Packet	The two-bit packet which precedes command packets and telemetry packet streams.
SVI3 Interface	The communication interface composed of SVC, SVD and SVT signals.
Telemetry Packet	A packet created by a reporting target containing telemetry or register data.
Telemetry Packet Stream	The expanding set of data that is pipelined on the telemetry daisy-chain as each target reports its respective telemetry.
Terminal Target	The target that is located the furthest away from the controller on the telemetry daisy-chain. The target with the highest address.
Transmit Mode	The reporting target is transmitting its telemetry on its telemetry output.

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Chapter 3 Serial VID Interface Version 3 (SVI3) Overview

3.1 Required Signals and Descriptions

As previously noted, this section only describes signals that are pertinent to the SVI3 communication bus. Additional required signals specific to device types can be found in their appropriate sub-sections.

Table 4. SVI3 Interface Signals

Signal	Controller I/O	Target I/O	Description
VCC	N/A	Input (Power)	VCC serves as the core logic power for SVI3 targets.
SVI3_VDDIO	Input (Power)	Input (Power)	SVI3_VDDIO serves as the reference for SVC, SVD, SVTI and SVTO.
SVC	Output	Input	Serial VID Clock is a push-pull signal which acts as a clock for SVD, SVTI and SVTO.
SVD	Output	Input	Serial VID Data is a push-pull signal which transmits commands from the controller to the targets.
SVTI	Input	Input	Serial VID Telemetry Input is driven by the next-furthest target (from the controller) on the telemetry daisy-chain. It carries telemetry and acknowledge packets.
SVTO	N/A	Output	Serial VID Telemetry Output is a push-pull output driven by each target. It carries telemetry and acknowledge packets.
SVI3_RESET_L	Input	Input	Active low signal causing all SVI3 state machines and SVI3-defined registers to reset to default states.

3.2 Interface Topology

The SVI3 topology is a 3-wire serial bus designed to support bi-directional data transfer between a single controller and up to 63 targets. From the controller's interface, the three wires consist of SVD (Serial VID Data), SVC (Serial VID Clock) and SVTI (Serial Telemetry VID Input).

As stated in Table 4, all signals in the SVI3 bus are unidirectional.

As shown in Figure 1, to facilitate the single-controller, multi-target topology, the SVC and SVD are connected from the controller to each target. Telemetry is connected in a daisy-chain pattern

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from the controller to Target N (also known as the “terminal target”). To enable daisy-chaining, each target has two telemetry I/Os: SVTI (Serial VID Telemetry Input) and SVTO (Serial VID Telemetry Output).

The terminal target plays a unique role in enumeration, telemetry and acknowledgement procedures. The SVTI pin of the terminal target is always grounded, allowing the target to be aware of its position in the daisy-chain.

It is important to note that multiple targets may reside in a single discrete integrated circuit. For example, a single voltage regulator controller IC may regulate 2 independent voltage rails meaning that 2 targets reside in the device. This is depicted in Figure 1 (refer to Target 1 and Target 2). As shown, for the case that 2 targets reside in a single physical device, only a single SVC, SVD, SVTI and SVTO physical pin is required. Internal to the IC, SVC and SVD are routed to each target. The daisy chain link between Target 1 and Target 2 exists internal to the IC.

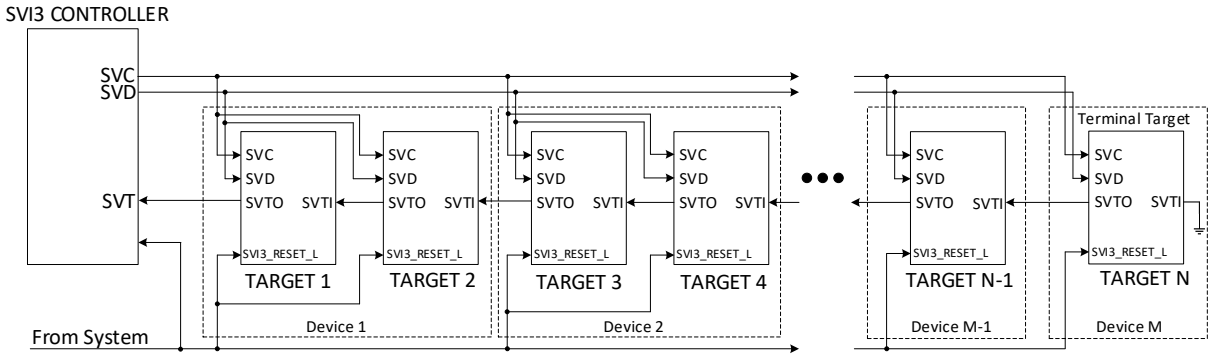

Figure 1. SVI3 Interface Topology

3.3 Addressing Convention

The SVI3 protocol can support up to 63 independent targets. Valid target addresses range from 01h to 3Fh. Address 00h is a reserved address designation. Addressing is not arbitrary. As shown in Figure 1, targets are addressed by their position in the SVI3 telemetry daisy chain, with the furthest target from the controller (the terminal target) having the greatest address. If multiple targets are present in a single device, the device shall consume multiple consecutive addresses.

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3.4 Electrical Requirements

The electrical requirements of the SVI3 interface are described in Table 5.

Table 5. SVI3 Interface Electrical Requirements

Parameter	Description	Min.	Typ.	Max.	Units	Notes
SVI3_VDDIO	SVI3 bus voltage	1.08		1.98	V	1
V_{IL}	SVC, SVD, SVTI input low voltage			0.35 * SVI3_VDDIO	V	
V_{IH}	SVC, SVD, SVTI input high voltage	0.65 * SVI3_VDDIO			V	
V_{HYST}	Hysteresis Voltage	0.1			V	
V_{OL}	SVC, SVD, SVTO output low voltage @ 8 mA			0.45	V	
	SVC, SVD, SVTO output low voltage @ 4 mA			0.22	V	
V_{OH}	SVC, SVD, SVTO output high voltage @ -8 mA	SVI3_VDDIO – 0.45			V	
	SVC, SVD, SVTO output high voltage @ -4 mA	SVI3_VDDIO – 0.22			V	
$V_{IL\_SVI3\_RESET\_L}$	SVI3_RESET_L input low voltage			0.63	V	2, 3
$V_{IH\_SVI3\_RESET\_L}$	SVI3_RESET_L input high voltage	1.17			V	2, 3
$I_{leak-Pin}$	Input leakage per SVC/SVD/SVT pin	-10		10	µA	
C_{Pin}	Input capacitance per physical pin (SVC, SVD, SVTI)			2	pF	

Notes:

1. *Nominal voltages 1.2V to 1.8V ± 10%*
2. *SVI3_RESET_L is not referenced to SVI3_VDDIO. SVI3_RESET_L must function normally when SVI3_VDDIO is not powered.*
3. *SVI3_RESET_L must be operable at 3.3V + 10%*

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3.5 Interface Timing Requirements

The SVI3 interface timing requirements are described in Table 6, Figure 2 and Figure 3. All setup and hold timing requirements are referring to signals observed at the physical device pins. There are no specified setup and hold requirements for telemetry signals that are only present within a physical device (for example, Target 1 and Target 2 in Figure 1). It is the responsibility of the device designer to ensure that all internal setup and hold timing constraints are met.

Table 6. SVI3 Interface Timing Requirements

Parameter	Description	Min.	Typ.	Max.	Units	Notes
t_p	Clock period	20		200	ns	1, 2, 3
f_{clock}	Clock frequency		$1/t_p$		Hz	1, 2, 3
$t_{SVC\_timeout}$	SVC high time that results in target's SVI3-interface being disabled (see Section 4.9)	400	500	600	ns	
t_{low}	Duration of low portion of clock	12	0.6 * t_p	0.65 * t_p	ns	
t_{high}	Duration of high portion of clock	0.35 * t_p	0.4 * t_p	0.45 * t_p	ns	
$t_{rise\_SVC\_SVD\_SYS}$	System Rise time for SVC, SVD: from V_{IL} to V_{IH}		0.1 * t_p	0.15 * t_p	ns	4, 7
$t_{fall\_SVC\_SVD\_SYS}$	System Fall time for SVC, SVD: from V_{IH} to V_{IL}		0.1 * t_p	0.15 * t_p	ns	4, 7
t_{rise_SVT}	Rise time for SVT: from V_{IL} to V_{IH}			2	ns	4, 7
t_{fall_SVT}	Fall time for SVT: from V_{IH} to V_{IL}			2	ns	4, 7
t_{delay}	Time for SVC/SVD/SVT to propagate from one device to another			2	ns	9
$t_{SVI3\_RESET\_L}$	SVI3_RESET_L assertion time	100			µs	8

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Table 6. SVI3 Interface Timing Requirements (Continued)

Parameter	Description	Min.	Typ.	Max.	Units	Notes
Controller-to-Target Path						
$t_{launch\text{-}Controller}$	Time from falling SVC edge at Controller to SVD transition at Controller		2		ns	5
$t_{setup\text{-}Target}$	Time from SVD valid at Target to rising clock edge at Target	2			ns	5
$t_{hold\text{-}Target}$	Time from rising SVC edge at Target to next SVD transition	2			ns	5
Target 1-to-Controller Path / Target-to-Target Path						
$t_{launch\text{-}Target}$	Time from falling SVC edge at Target to beginning of SVT transition at Target	0			ns	5, 6
$t_{rise/fall\_SVT} + t_{launch\text{-}Target}$	Time from falling SVC edge at Target to end of SVT transition at Target			6	ns	5, 6
$t_{setup\text{-}Controller}$	Time from SVT valid at Controller to rising SVC edge at Controller	2			ns	5, 6
$t_{hold\text{-}Controller}$	Time from rising SVC edge at Controller to next SVT transition	2			ns	5, 6

Notes:

1. *Clock frequency/period may change in flight*
2. *A period-to-period frequency tolerance of less than ± 500ps (above/below the max/min) is considered acceptable*
3. *Targets must be capable of supporting the entire frequency range*
4. *Measured at receiver*
5. *Measured at external pins*
6. *Timing also applies to target SVTI for target-to-target path*
7. *Timing refers to VOH/VOL with +/-8mA load (see Table 5)*
8. *Targets shall reset all SVI3-defined registers and the SVI3 communication bus within $t_{SVI3\_RESET\_L}$ relative to SVI3_RESET_L assertion*
9. *T_delay max is for 50MHz SVC operation. For systems limited to below 50MHz, t_delay must be less than ½ [0.55*t_p – (rise/fall_SVT + $t_{launch\text{-}Target}$) – $t_{setup\text{-}Controller}$].*

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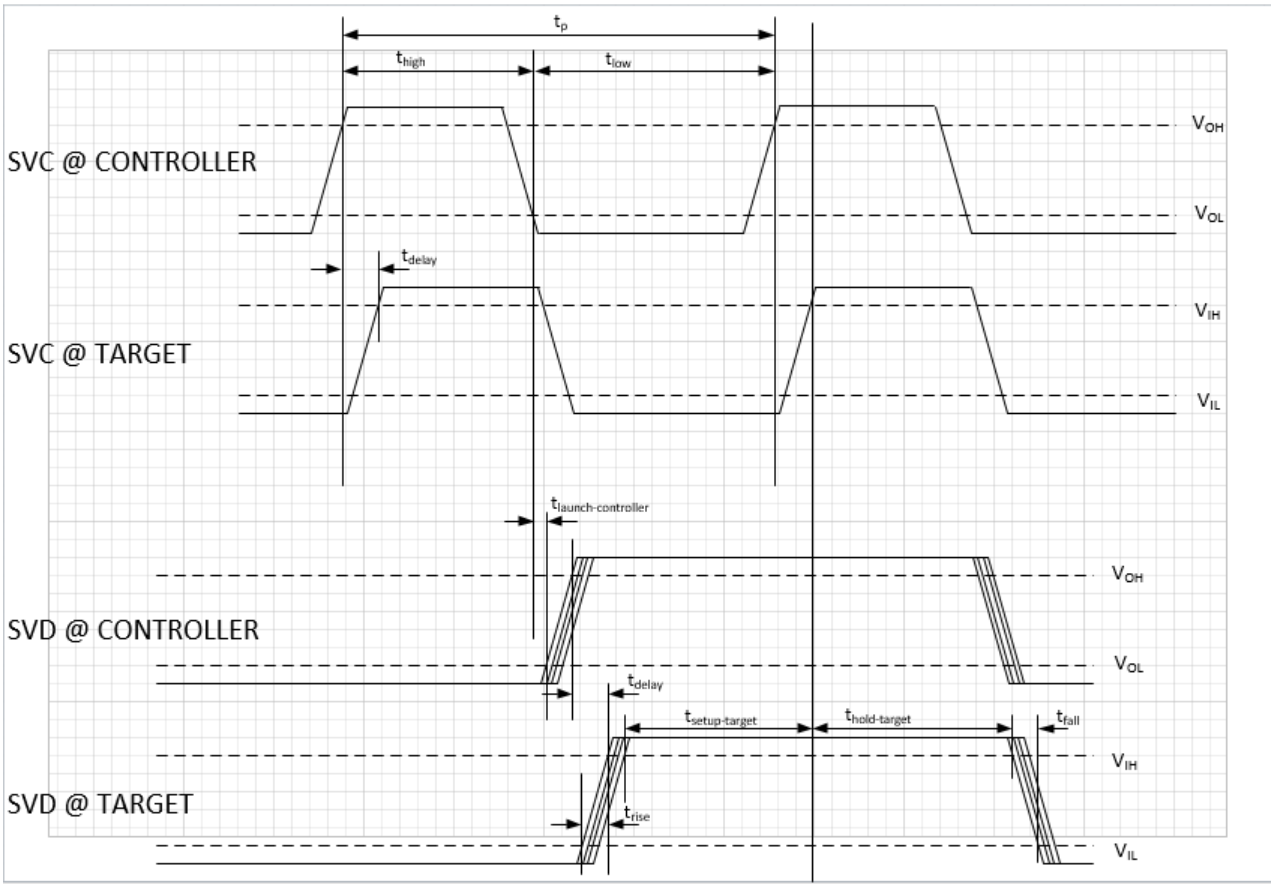

Figure 2. SVC/SVD Timing

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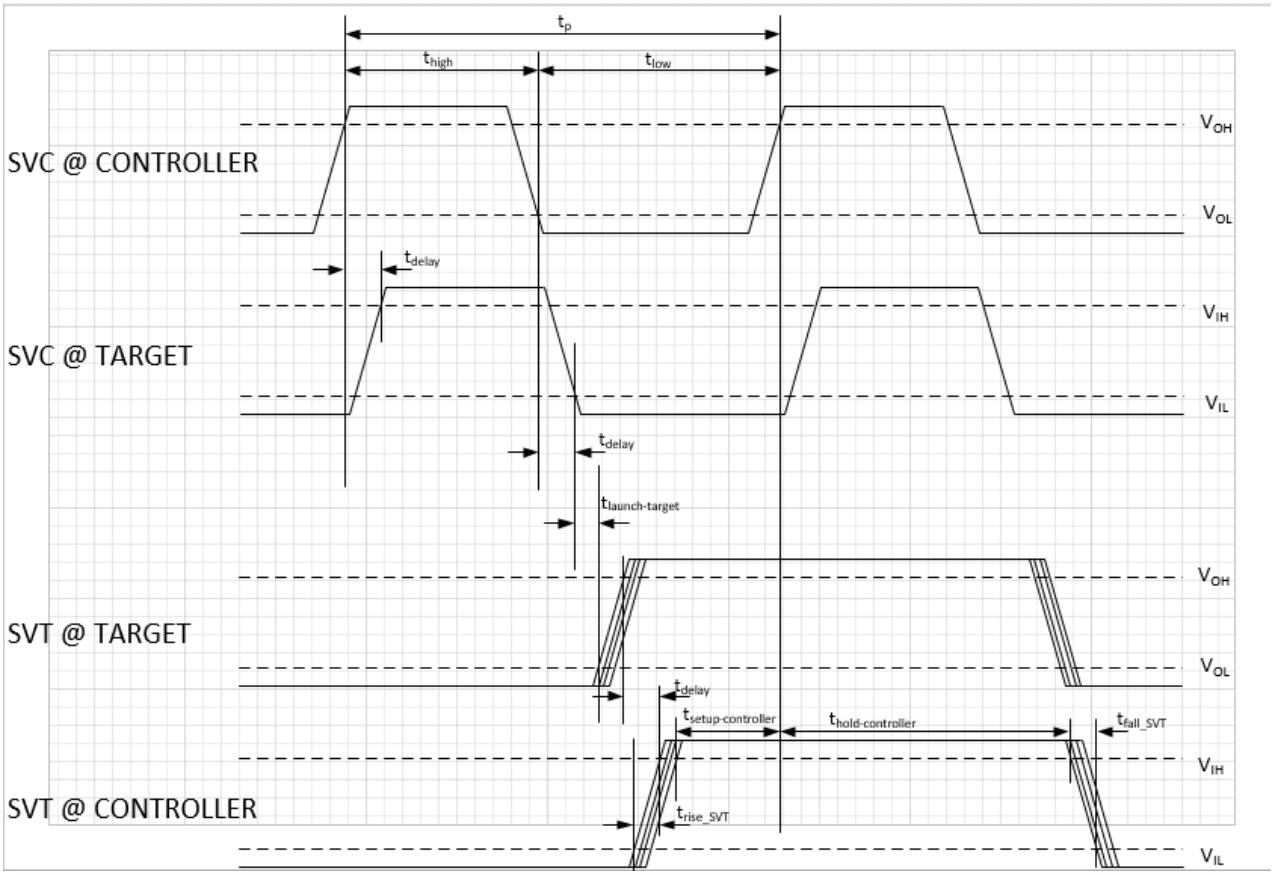

Figure 3. SVC/SVT Timing

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Chapter 4 Protocol Rules

4.1 Clocking, Data Launch and Capture

The SVC clock either operates continuously or is shut down completely (see Section 4.9).

SVD and SVTO are launched on the falling edge of SVC. SVD and SVTI are captured on the rising edge of SVC.

4.2 Daisy-Chain Pipelining

For the purposes of target enumeration, telemetry reporting and command acknowledgement, targets pipeline data on the daisy-chain, toward the controller. All targets have a pipelining latency of two clock cycles. In other words, if a target is pipelining, it captures a SVTI bit on a rising SVC edge and launchs the bit on SVTO immediately following two SVC falling edges.

4.3 Command Packet Framing

4.3.1 Start Packet

A 2-bit Start packet consisting of 01b precedes all commands. All command packets follow immediately after a Start packet.

4.3.2 CRC Verification

All SVI3 target devices must support 3-bit CRC verification for command packets and telemetry. The requirement of CRC verification is programmable (enabled/disabled) through an SVI3-defined global command (see Section 4.5.5.3 and Section 4.5.5.4). CRC is enabled by default.

If CRC is enabled, the controller generates a 3-bit CRC code based on the 8-, 16- or 24-bits of the packet. The target confirms the packet and CRC code using the CRC-3 polynomial, shown below:

$CRC(x) = x^3 + x + 1$

The initial value of the CRC shift register is set to all zeroes. It will reset to the initial value for every packet.

4.3.3 Packet Completion

Depending on the type of packet, lengths vary from 8, 16 and 24 bits. The target must decode the packet type and count the appropriate number of bits to determine the end of a packet. Packet length is detailed in Section 4.5.7.

Following every packet, the controller transmits a 2-bit End packet consisting of 10b.

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4.3.4 Packet Completion and Execution

When a packet is preceded by a Start packet, has the expected number of bits, passes CRC verification (if enabled) and is succeeded by an End packet, the packet is considered valid. Only after all these conditions are confirmed, will a target execute the command and return an ACK (provided the command is executable).

4.3.5 Packet Mis-Communication

If the communication verification conditions are not met (i.e., CRC verification fails, or an End packet is not observed after the expected number of bits), the target will not execute the command. Every target on the SVI3 interface verifies framing and CRC (if enabled) for every command packet sent (regardless of the selected target). If any target detects a framing error or CRC error (if enabled), it returns a NACK: Communication Error (see Section 4.8.) The SVI3 interface then undergoes the re-synchronization procedure detailed in Section 4.11.

4.4 Initialization

The SVI3 bus initialization procedure is designed to ensure that all SVI3 signals are connected properly and stable before communication can occur. The initialization procedure also automatically addresses each target based on its position in the telemetry daisy-chain. Bus initialization and target enumeration must be completed before any subsequent commands or telemetry can be transmitted.

Initialization Requirement Rules:

1. Bus initialization and target addressing is only required when the power source of VCC is cycled.
2. Assertion of SVI3_RESET_L does not reset the target addresses (additional target enumeration is not required).
3. SVI3_VDDIO power cycling does not reset the target addresses (additional target enumeration is not required).
4. For voltage regulator targets, it is not required that the target be initialized before voltage regulation is enabled.
5. After VCC power-on, the initialization procedure must occur before any non-initialization commands can be sent or telemetry received (i.e., Before initialization, any non-initialization commands are ignored by the targets).

4.4.1 Bus Initialization

Referring to Figure 7 and Table 7, the bus initialization procedure is as follows:

1. VCC is powered and within regulation. All SVI3-defined registers are initialized to their respective default values.
2. SVI3_VDDIO is powered and within regulation.

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3. The detection of SVI3_VDDIO entering regulation triggers a POR (power-on reset) by the targets of the communication bus. The communication bus is held in reset, by the targets for $T_{SVI3\_VDDIO-SVI3\_POR}$.
4. SVC, SVD and all instances of SVTO transition high and are stable before a maximum of $T_{SVI3\_VDDIO-SVC\_SVD\_SVTO}$ after VCC and SVI3_VDDIO are within regulation.
5. SVI3_RESET_L is guaranteed high for a minimum of $T_{SVI3\_RESET\_L-SVC\_START}$ before SVC begins toggling.
6. SVI3_VDDIO is within regulation a minimum of $T_{SVI3\_VDDIO-SVC\_START}$ before SVC begins toggling.
7. SVD remains high for at least $T_{SVC\_START-INIT\_START}$ after SVC begins toggling. The controller initiates the target enumeration sequence. Any SVD transitions which occur before $T_{SVC\_START-INIT\_START}$ is ignored by the target (i.e., the SVD line is not observed until $T_{SVC\_START-INIT\_START}$ is complete).

4.4.2 Target Enumeration and Addressing

The SVI3 protocol requires that each target be addressed based on their position in the telemetry daisy-chain. After bus initialization, the controller begins enumerating and addressing the targets. The process is as follows:

1. The controller transmits a Start packet, global Initialization packet (see Section 4.5.5.1 for packet details), 3-bit CRC packet (if enabled) and an End packet via SVC/SVD. All targets listen to this packet. Non-terminal targets enter pipelining mode.

   Note: *All un-initialized targets listen to the SVC/SVD bus but ignore all command packets except the Initialization command packet.*

2. The terminal target immediately begins transmitting a Start packet, followed by a single 0b, on the telemetry bus. Following this, the terminal target begins transmitting 1b's.
3. The next closest target (N-1) will pipeline through the Start packet and begin counting 0b's
   a. For every 0b observed, the target increments its address offset register.
   b. When the target observes its first 1b on its input, it discards it and replace it with a single 0b in the pipeline.
   c. Following the above-mentioned bit flip, the target resumes pipelining.
4. All non-terminal targets follow the behavior described in Step 3. This pattern continues until Target 1 pipelines a packet to the controller that consists of a Start packet followed by N 0b's.
5. The controller confirms that the number of 0b's is as expected and transmits a Start packet, Address packet, 3-bit CRC, and End packet. The data payload of the Address packet is equal to the number of targets (number of 0b's) (see Section 0 for packet details).

   Note: *The controller ensures that only an Address packet is sent following an Initialization command. No other command type is valid until the enumeration procedure is complete.*

6. Every target listens to the Address packet. Each target is addressed as the Address packet payload minus their respective "address offset". All targets exit initialization mode and follow standard protocol rules.

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7. All targets transmit a completed ACK in response to the Address packet (as per Section 4.8).

The target enumeration procedure allows for automatic addressing of each target on the SVI3 bus as well as confirming that the SVI3 bus is functioning and connected correctly.

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4.4.2.1 Target Enumeration Example

The following figures (Figure 4, Figure 5 and Figure 6) illustrate a target enumeration process for a bus with six targets.

Controller (Input Only)		Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed
Pipeline Mode		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
Transmit Mode			Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
Idle Transmit (1b's only)		1	1 1	1 1	1 1	1 1	1 1	1
	Clock 0	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 0
The terminal Target initiates telemetry stream by placing start packet on bus	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 1	0
	Clock 1	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 0
	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 0	1
	Clock 2	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 0
The terminal Target adds a single 0b to the stream and sets its own offset = 0	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]	0b
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	0 1	0
	Clock 3	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 0
	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]	0b	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]	Idle (1b)
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 0	1 0	1
	Clock 4	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 1	Offset = 0
The N-1 Target detects the 0b and increments its offset register	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]	0b	Idle (1b)
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	0 1	0 1	1
	Clock 5	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 1	Offset = 0
The N-1 Target detects a 1b on its input. It discards the 1b and transmits a single 0b	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]	0b	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]	Out: Transmit 0b	Idle (1b)
	SVTO | SVTI Reg:	1	1 1	1 1	1 0	1 0	0 1	1
	Clock 6	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 1	Offset = 1	Offset = 0
The N- 1 Target switches to pipeline mode	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]	0b	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Start Packet [1]	0b	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	1 1	1 1	0 1	0 0	1 1	1

Figure 4. Target Enumeration Example (Part 1)

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Controller (Input Only)	Clock 7	Controller	Non-Addressed	Non-Addressed	Non-Addressed	Offset = 2	Offset = 1	Offset = 0
Pipeline Mode	SVTI Reg:	Idle (1b)	Idle (1b)	Start Packet [1]	0b	Idle (1b)	Idle (1b)	
Transmit Mode	SVTO Reg:		Idle (1b)	Idle (1b)	Start Packet [0]	0b	Idle (1b)	Idle (1b)
Idle Transmit (1b's only)	SVTO | SVTI Reg:	1	1 1	1 0	1 0	0 1	1 1	1
	Clock 8	Controller	Non-Addressed	Non-Addressed	Offset = 1	Offset = 2	Offset = 1	Offset = 0
The N-2 Target detects 1b on it	SVTI Reg:	Idle (1b)	Idle (1b)	Start Packet [0]	0b	Idle (1b)	Idle (1b)	
input. It discards the 1b and	SVTO Reg:		Idle (1b)	Start Packet [1]	0b	Transmit 0b	Idle (1b)	Idle (1b)
transmits a single 0b	SVTO | SVTI Reg:	1	1 1	0 1	0 0	0 1	1 1	1
	Clock 9	Controller	Non-Addressed	Non-Addressed	Offset = 2	Offset = 2	Offset =1	Offset = 0
	SVTI Reg:	Idle (1b)	Start Packet [1]	0b	0b	Idle (1b)	Idle (1b)	
The N-2 Target switches to	SVTO Reg:		Idle (1b)	Start Packet [0]	0b	Idle (1b)	Idle (1b)	Idle (1b)
pipeline mode	SVTO | SVTI Reg:	1	1 0	1 0	0 0	1 1	1 1	1
	Clock 10	Controller	Non-Addressed	Offset = 1	Offset = 3	Offset = 2	Offset =1	Offset = 0
	SVTI Reg:	Idle (1b)	Start Packet [0]	0b	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Start Packet [1]	0b	0b	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	0 1	0 0	0 1	1 1	1 1	1
	Clock 11	Controller	Non-Addressed	Offset = 2	Offset = 3	Offset = 2	Offset =1	Offset = 0
The N-3 Target detects 1b on it	SVTI Reg:	Start Packet [1]	0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	
input. It discards the 1b and	SVTO Reg:		Start Packet [0]	0b	Transmit 0b	Idle (1b)	Idle (1b)	Idle (1b)
transmits a single 0b	SVTO | SVTI Reg:	0	1 0	0 0	0 1	1 1	1 1	1
	Clock 12	Controller	Offset = 1	Offset = 3	Offset = 3	Offset = 2	Offset =1	Offset = 0
	SVTI Reg:	Start Packet [0]	0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	
The N-3 Target switches to	SVTO Reg:		0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
pipeline mode	SVTO | SVTI Reg:	1	0 0	0 0	1 1	1 1	1 1	1
	Clock 13	Controller	Offset = 2	Offset = 4	Offset = 3	Offset = 2	Offset =1	Offset = 0
	SVTI Reg:	0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle
	SVTO Reg:		0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO | SVTI Reg:	0	0 0	0 1	1 1	1 1	1 1	1
	Clock 14	Controller	Offset = 3	Offset = 4	Offset = 3	Offset = 2	Offset =1	Offset = 0
The N-4 Target detects 1b on it	SVTI Reg:	0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle
input. It discards the 1b and	SVTO Reg:		0b	Transmit 0b	Idle (1b)	Idle (1b)	Idle (1b)	
transmits a single 0b	SVTO | SVTI Reg:	0	0 0	0 1	1 1	1 1	1 1	1

Figure 5. Target Enumeration Example (Part 2)

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Controller (Input Only)	**Clock 15**	**Controller**	**Offset = 4**	**Offset = 4**	**Offset = 3**	**Offset = 2**	**Offset =1**	**Offset = 0**	
Pipeline Mode	SVTI Reg:	0b	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle	
Transmit Mode	SVTO Reg:		0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)		
Idle Transmit (1b's only)	SVTO | SVTI Reg:	0	0 0	1 1	1 1	1 1	1 1	1	
	Clock 16	**Controller**	**Offset = 5**	**Offset = 4**	**Offset = 3**	**Offset = 2**	**Offset =1**	**Offset = 0**	
	SVTI Reg:	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)		
	SVTO Reg:		0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO | SVTI Reg:	0	0 1	1 1	1 1	1 1	1 1	1	
	Clock 17	**Controller**	**Offset = 5**	**Offset = 4**	**Offset = 3**	**Offset = 2**	**Offset =1**	**Offset = 0**	
The N-5 Target detects 1b on it input. It discards the 1b and transmits a single 0b	SVTI Reg:	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)		
	SVTO Reg:		Transmit 0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO | SVTI Reg:	0	0 1	1 1	1 1	1 1	1 1	1	
	Clock 18	**Controller**	**Offset = 5**	**Offset = 4**	**Offset = 3**	**Offset = 2**	**Offset =1**	**Offset = 0**	
The N-5 Target switches to pipeline mode and Controller counts its 6th 0	SVTI Reg:	0b	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)		
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO | SVTI Reg:	0	1 1	1 1	1 1	1 1	1 1	1	
The Controller detects a 1b. The Controller begins to send a start packet + address packet + CRC	**Clock 19**	**Controller**	**Offset = 5**	**Offset = 4**	**Offset = 3**	**Offset = 2**	**Offset =1**	**Offset = 0**	
	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)		
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 1	1	
	Clock 32	**Controller**	**Address = 1**	**Address = 2**	**Address = 3**	**Address = 4**	**Address = 5**	**Address = 6**	
All Targets receive the address packet and set their respective addresses	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)		
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 1	1	

Figure 6. Target Enumeration Example (Part 3)

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4.4.3 Initialization Timing

The initialization timing is described in Figure 7 and Table 7.

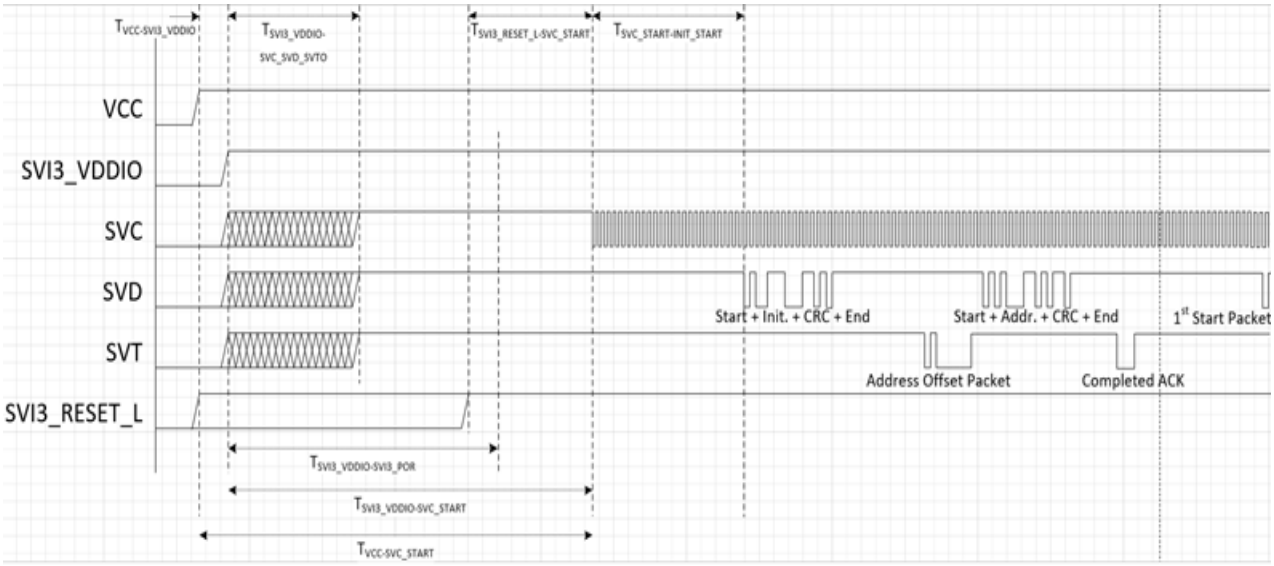

Figure 7. SVI3 Bus Initialization Timing

Table 7. SVI3 Initialization Timing Requirements

Parameter	Description	Min	Max	Unit
$T_{VCC-SVI3\_VDDIO}$	Time that SVI3_VDDIO must be powered and stable relative to VCC being powered and stable	0		µs
$T_{SVI3\_VDDIO - SVC\_SVD\_SVTO}$	Time that SVC, SVD and SVTO must be high and stable relative to SVI3_VDDIO power		10	µs
$T_{SVI3\_RESET\_L-SVC\_START}$	Time that SVI3_RESET_L is guaranteed high before SVC begins toggling	10		µs
$T_{VCC-SVC\_START}$	Time that controller must wait before beginning to toggle SVC relative to VCC power	10		ms
$T_{SVI3\_VDDIO-SVC\_START}$	Time that controller must wait before beginning to toggle SVC relative to SVI3_VDDIO power	1		ms

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Table 7. SVI3 Initialization Timing Requirements (Continued)

Parameter	Description	Min	Max	Unit
$T_{SVI3\_VDDIO-SVI3\_POR}$	Time that a target must hold the SVI3 interface in reset relative to SVI3_VDDIO power	$T_{SVI3\_VDDIO-SVC\_SVD\_SVTO}$ (max)	$T_{SVI3\_VDDIO-SVC\_START}$ (min)	
N_{SVC_INIT}	Number of clock cycles that SVD must remain high relative to the first SVC falling edge	8		
$T_{SVC\_START-INIT\_START}$	Time that SVD must remain high relative to the first SVC falling edge	$N_{SVC\_INIT}*t_P$		ns

4.5 Command Operation

4.5.1 Addressing Rules

1. The Address packet and Address/VID packet are responsible for changing the selected target.
2. After being selected, only the selected target executes all following commands until another target is selected (i.e., Address packets are not required for every subsequent command).
3. If the controller attempts to point to a target with a target address greater than the terminal target's address, the terminal target returns a NACK: Invalid Command. If any subsequent commands/command streams are sent without first pointing to a valid address, the terminal target returns a NACK: Invalid Command.
4. The Address packet sent during enumeration is a special case and does not change/set the selected target.
5. The assertion of SVI3_RESET_L removes selected target status from all targets.
6. If a non-global command is requested while no targets are selected, the terminal target returns a NACK: Invalid Command.

4.5.2 Acknowledgements

The SVI3 protocol mandates that a target returns an acknowledgement on the SVT bus after it receives an individual SVD command (if only one command is to be sent) or a stream of SVD commands (see Section 4.5.3). There are three types of acknowledgements that a target can return:

ACK: Valid and executable command; no communication errors

NACK: Invalid Command: Invalid/unsupported command; non-executable command; address/register offset/data out of range

NACK: Communication Error: Incorrect bit count (end packet not observed when expected), unexpected bit value (invalid start packet), CRC error (if enabled)

The mechanism to return acknowledgements is covered in detail in Section 4.8.

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4.5.3 Back-to-Back Command Packets

SVI3 command packets may be communicated individually or as a continuous stream of commands.

To send an individual packet, the controller returns the SVD line high after the packet is completed. (i.e., when an individual packet is sent, the first bit received by the target after the End packet is 1b).

To send a back-to-back stream of packets, the controller sends the Start packet (01b) immediately following the previous End packet. (i.e., when a back-to-back command is sent, the first bit received by the target after an End packet is 0b). The back-to-back stream of packets are terminated when the SVD line is returned high following an End packet.

4.5.3.1 Back-to-Back Command Packet Rules:

1. A target begins executing each command immediately following the End packet (i.e., the target doesn't wait until the packet stream is complete.)
2. Each target effected by the command packet stream returns a single acknowledgement when the stream is complete.
3. If the target has multiple types of acknowledgements to return for a single command packet stream, the target returns a single acknowledgment based on the following priority:
   a. NACK: Communication Error (highest priority; overwrites all previous NACKs and ACKs)
   b. NACK: Invalid Command (mid priority; overwrites all previous ACKs)
   c. ACK (lowest priority; does not overwrite previous NACKs)
4. If a target requires a NACK return for any command in the stream, the target doesn't execute the NACK'd command packet or any subsequent packets in the stream.

4.5.4 Packet Types

The SVI3 protocol contains several packet types which range in bit lengths from 8, 16 and 24 bits.

4.5.4.1 Address Packet

The Address packet is used to point to the target to which all following commands are directed. This target is known as the selected target.

Bit length: 8

Packet structure:

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Address Packet							
VIDSEL (0b)	ADRSEL (1b)	Address (5:0)					
7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packet, 0b for non-VID packets
ADRSEL: 1b for Address packets, 0b for all other packets
Address (5:0): The address of the selected target

4.5.4.2 VID Packets (for Voltage Regulator Devices)

VID packets are used only for target devices that output a programmed voltage and require a VID target (such as voltage regulators.) This is a special packet which changes the selected target and sets the target VID for that target. The selected target executes all subsequent commands.

Bit length: 16
Packet Structure:

VID															
VIDSEL (1b)	Address (5:0)						VID (8:0)								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packet, 0b for non-VID packets
Address (5:0): The address of the selected target
VID (8:0): The target VID of the selected target

4.5.4.3 Change Power State (for Voltage Regulator Devices)

Change Power State packets are used only for voltage regulator target devices that have different power modes ranging from max power capacity to max efficiency.

Bit length: 8
Packet Structure:

Change Power State							
VIDSEL (0b)	ADRSEL (0b)	Command Type (001b)			PSI (2:0)		
7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packet, 0b for non-VID packets
ADRSEL: 1b for Address packets, 0b for all other packets
Command Type: 001b for Change Power State
PSI (2:0): Power state indicator (encoded power states 0-7)

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4.5.4.4 Register Write

The Register Write packet is used to write to an SVI3-defined register or a manufacturer-specific register (if supported).

Bit length: 24

Packet Structure:

Register Write																							
VIDSEL (0b)	ADRSEL (0b)	Command type (010b)			Mfg.	Reserved (11b)		Register Offset (7:0)								Data (7:0)							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packet, 0b for non-VID packets
ADRSEL: 1b for Address packets, 0b for all other packets
Command Type: 010b for Register Write
Mfg.: 1b for manufacturer specific registers, 0b for SVI3 specific registers
Reserved: Always 11b
Register Offset (7:0): 8-bit offset value of register to be written
Data (7:0): Data to be written to register

4.5.4.5 Register Read

The Register Read packet is used to read an SVI3-specified register or a manufacturer-specific register (if supported). The return data is read during the next requested telemetry round. If an additional Register Read command is received before the next requested telemetry round, the target only returns the most recent request (i.e., The target only needs to store one Register Read request.).

Bit length: 16

Packet Structure:

Register Read															
VIDSEL (0b)	ADRSEL (0b)	Command type (011b)			Mfg.	Reserved (11b)		Register Offset (7:0)							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packet, 0b for non-VID packets
ADRSEL: 1b for Address packets, 0b for all other packets
Command Type: 011b for Register Read
Mfg.: 1b for manufacturer specific registers, 0b for SVI3 specific registers
Reserved: Always 11b
Register Offset (7:0): 8-bit offset value of register to be read

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4.5.4.6 Register Reset

The Register Reset packet is used to reset registers to their respective default values.

Bit length: 8

Packet Structure:

Register Reset							
VIDSEL (0b)	ADRSEL (0b)	Command Type (100b)			Register Type (2:0)		
7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packet, 0b for non-VID packets
ADRSEL: 1b for Address packets, 0b for all other packets
Command Type: 100b for Register Reset
Register Type (2:0): [2] Mfg. Register (not SVI3-defined) *optional* (if supported)
[1] SVI3-defined registers excluding VID and PSI
[0] VID and PSI

4.5.5 Global Commands

Global Command Rules:

1. Global commands only exist as a single command. Back-to-back command streams do not contain a global command.
2. Global commands are executed by all applicable targets immediately and simultaneously.
3. Except for the Initialization command, the controller expects an acknowledgement packet for every global command. Each target modifies the acknowledgement packet based on the rules detailed in Section 4.8.4.3.
4. Global commands do not require any addressing. Issuing a global command does not change the selected target that responds to subsequent non-global commands.

Bit length: 8

Packet Structure:

Global Command							
VIDSEL (0b)	ADRSEL (0b)	Command Type (111b)			Global Command Type (2:0)		
7	6	5	4	3	2	1	0

VIDSEL: 1b for VID packets, 0b for non-VID packets
ADRSEL: 1b for Address packets, 0b for all other packets
Command Type: 111b for Global commands
Global Command Type: Global command action code

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4.5.5.1 Initialization (Global Command Type 000b)

As discussed in Section 4.4, the Initialization packet is used for target enumeration.

If target enumeration has already occurred, the initialization procedure still occurs (as per Section 4.4) and the most recent enumeration overwrites previously determined addresses. The execution of the initialization procedure does not reset/modify any SVI3 registers, defined in Section 5.12 or Section 6.11.

4.5.5.2 Telemetry Request (Global Command Type 001b)

Issued to alert all targets to store the most recently acquired telemetry and to prepare for reporting to a telemetry stream. This command also indicates to the terminal target to initiate a telemetry stream. The function of this packet is discussed further in Section 4.6.

4.5.5.3 Enable CRC Verification (Global Command Type 010b)

All targets expect a 3-bit CRC packet after all subsequent command packets. Commands are only executed after successful CRC verification.

All targets add a 3-bit CRC packet following their respective telemetry transmission.

It is the controller's responsibility to ensure that no telemetry streams are being transmitted while the CRC verification feature is being enabled/disabled.

4.5.5.4 Disable CRC Verification (Global Command Type 011b)

All targets do not expect a 3-bit CRC packet after all subsequent command packets.

All targets do not add a 3-bit CRC packet following their respective telemetry transmission.

It is the controller's responsibility to ensure that no telemetry streams are being transmitted while the CRC verification feature is being enabled/disabled.

4.5.5.5 Return VID/PSI to Default – Voltage Regulator Targets (Global Command Type 110b)

Commands each voltage regulator target to set its VID value to its respective default VID. The default VID is defined as the voltage set, at the platform level, in a non-volatile fashion (non-volatile memory, resistor strap, etc.). The command also sets the PSI to its default value.

4.5.5.6 Return All SVI3 Registers to Default – (Global Command Type 111b)

Commands each target to set all of its SVI3-specified registers (including VID and PSI) to their respective default values (defined in Section 5.12). The command does not affect any registers that are not defined in the SVI3 specification (i.e., the command does not affect any manufacturer specific registers). All targets retain their previously assigned address. i.e., Target enumeration and addressing is not required after this command.

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4.5.6 Command Syntax

The command syntax is described in Figure 8. The figure illustrates the syntax branches depending on the type of packet. The figure also illustrates the path for back-to-back commands.

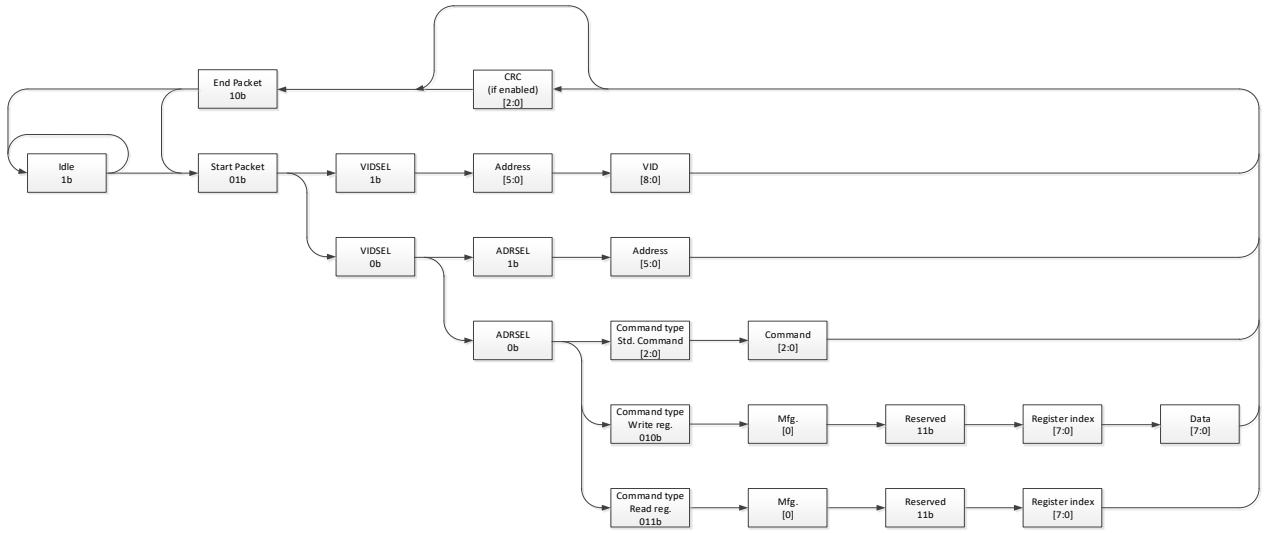

Figure 8. SVI3 Command Syntax

Note: *When CRC is disabled, the End packet 10b shall be transmitted immediately following the command packet.*

4.5.7 Packet Length

For all command packets, the total packet length is determined from decoding the first 5 bits of the packet, as illustrated in Figure 8 and shown in Table 8. For 5-bit combinations not listed in Table 8 (invalid commands), targets assume an 8-bit packet length.

Table 8. Packet Length Decoding

MSB				LSB	Packet Length	
1	X	X	X	X	16	bits
0	1	X	X	X	8	bits
0	0	0	0	1	8	bits
0	0	0	1	0	24	bits
0	0	0	1	1	16	bits
0	0	1	0	0	8	bits
0	0	1	1	1	8	bits

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4.6 Telemetry

The SVI3 protocol allows each target to report an arbitrary amount of telemetry information to the controller. This enables system flexibility since some types of information may not be useful from all targets (example: There may be limited value of continuously reporting temperature of a low-power auxiliary point-of-load converter).

SVI3-defined registers control which types of telemetry each target is to report. These registers are programmed through Register Write commands.

4.6.1 Telemetry Operation

As shown in Figure 1, the telemetry bus is daisy chained. The important points of the telemetry operation are:

1. Data is always flowing toward the controller.
2. Telemetry for the entire system is reported through the daisy-chain, in long, continuous streams.
3. Each target pipelines data with a two-bit primary buffer (see Figure 9). As mentioned in Section 4.8.4.2, a 4-bit secondary buffer is also required for enqueueing/dequeuing acknowledgement packets.
4. When idle (or between streams), the terminal target transmits 1b's and all other targets pipeline the 1b's toward the controller.
5. Each target contributes to the stream, starting with the terminal target and ending with Target 1 (closest to the controller).
6. The frequency at which the telemetry streams begin (report rate) is dictated by the controller's frequency of issuing Telemetry Request packets.
7. The controller ensures that Telemetry Request command packets are only issued when no telemetry stream exists on the daisy-chain.

4.6.1.1 Telemetry Stream Creation

The step-by-step creation of a telemetry stream is as follows:

1. The controller sends a Telemetry Request command packet, indicating to all targets to prepare for reporting telemetry (capture and store latest acquisition).
2. Following the receipt of a Telemetry Request packet, the terminal target transmits an ACK (as described in Section 4.8) and then waits eight SVC clock cycles.
3. After the terminal target has waited eight clock cycles, the terminal target transmits:
   a. A Start packet (01b)
   b. A telemetry header packet with the terminal target address (N) (see Section 4.6.4.1)
   c. All telemetry packets enabled for the terminal target (back-to-back, without interruption, in any order)
   d. Header packet with the N-1 target address (see Section 4.6.4.1)

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e. If CRC verification is enabled, transmit the 3-bit CRC packet (as defined in Section 4.3.2) based on the combination of the Target N header packet, all Target N telemetry packets, and the Target N-1 header packet
f. Continuous 1b's (switches to "idle transmit mode")

4. While the terminal target is transmitting, the N-1 target is pipelining bits while listening for its own header packet. Immediately after the N-1 target pipelines and reads its own header packet (and passes through the following 3-bit CRC, if enabled) it will:
   a. Transmit all telemetry packets enabled for the N-1 target (back-to-back, without interruption, in any order)
   b. Transmit the header packet with N-2 target address (see Section 4.6.4.1)
   c. If CRC verification is enabled, transmit the 3-bit CRC packet (as defined in Section 4.3.2) based on the combination of all Target N-1 telemetry packets and the Target N-2 header packet
   d. Switch to pipeline mode
5. The above pattern continues with each target reporting its own telemetry in descending order of address.
6. Immediately after the Target 1 pipelines and reads its own header packet (and passes through the following 3-bit CRC, if enabled), it completes the following:
   a. Transmit all telemetry packets enabled for Target 1 (back-to-back, without interruption, in any order)
   b. Transmit the header packet with Target 0 address (see Section 4.6.4.1), indicating the end of the telemetry stream
   c. If CRC is enabled, transmit the 3-bit CRC packet (as defined in Section 4.3.2) based on the combination of all Target 1 telemetry packets and the Target 0 header packet
   d. Switch to pipeline mode

The bus remains idle (with the terminal target transmitting 1b and all non-terminal targets pipelining 1b until the controller sends another Telemetry Request packet or an acknowledgement is required to be returned (see Section 4.8).

4.6.2 Telemetry Stream Framing

4.6.2.1 Start Packet

Like the command packet, the entire telemetry stream is preceded by a single 2-bit Start packet (01b). Individual telemetry packets within the stream are not preceded by a Start packet.

4.6.2.2 Header Packet with Address 0

The receipt of a header packet with address 0 (and 3-bit CRC packet, if enabled) signifies to the controller that the telemetry stream is complete.

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4.6.3 Telemetry Packet Framing

4.6.3.1 Header Packet

Each header packet indicates to the controller from which target the following telemetry packets were reported. It signifies the beginning of a series of telemetry packets from the respective target.

4.6.3.2 Telemetry Packet Length

Like command packets, individual telemetry packets are framed by counting bits. Depending on the type of telemetry packet, the bit length can vary from 8, 16, 24 bits.

4.6.4 Packet Types

4.6.4.1 Header Packets

Specifies the address of the target from which the following telemetry packets were reported.

Bit length: 8

Packet Structure:

Header Packet							
Packet Type (11b)		Address (5:0)					
7	6	5	4	3	2	1	0

Packet Type: 00b Acknowledge, 10b: Telemetry, 11b: Header packet

Address (5:0): Target address of following telemetry

4.6.4.2 Standard 10-bit Telemetry

The most common streaming telemetry packet. Contains 10-bit data payload.

Bit length: 16

Packet Structure:

Standard 10-bit Telemetry															
Packet Type (10b)		Exp. (0b)	Telemetry Reg. Index (2:0)			Telemetry Data (9:0)									
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Packet Type: 00b Acknowledge, 10b: Telemetry, 11b: Header packet

Exp: 0b for standard 10-bit telemetry, 1b for expanded set of telemetry

Telemetry Reg Index: Indicates type of telemetry (for application specific telemetry mapping, see Section 5.10)

Telemetry Data: Telemetry data payload

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4.6.4.3 16-bit Telemetry

Used for transmitting 16-bit telemetry (if applicable).

Bit length: 24

Packet Structure:

16-bit Telemetry																								
Packet Type (10b)		Exp. (1b)	Exp. Tel Type (00b)		Telemetry Reg. Index (2:0)			Telemetry Data (15:0)																
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Packet Type: 00b Acknowledge, 10b: Telemetry, 11b: Header packet

Exp: 0b for standard 10-bit telemetry, 1b for expanded set of telemetry

Exp. Tel Type: 00b for 16-bit telemetry, 01b reserved, 10b reserved, 11b Register Readback

Telemetry Reg Index: Indicates type of telemetry (for application specific telemetry mapping, see Section 5.10)

Telemetry Data: Telemetry data payload

4.6.4.4 Register Readback

Register Readback data is related to the most recent Register Read command sent to the target. If no Register Read command is received since the last Telemetry Request, no packet is sent.

To prevent race conditions, the target only reports Register Readback packets pertaining to a Register Read command sent prior to the most recent Telemetry Request. In other words, if a target receives a Register Read command after receiving a Telemetry Request, but before reporting its own telemetry, it waits until a subsequent Telemetry Request.

Bit length: 24

Packet Structure:

Register Readback																								
Packet Type (10b)		Exp. (1b)	Exp. Tel Type (11b)		Mfg.	Reserved (11b)		Register Offset (7:0)								Register Data (7:0)							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Packet Type: 00b Acknowledge, 10b: Telemetry, 11b: Header packet

Exp: 0b for standard 10-bit telemetry, 1b for expanded set of telemetry

Exp. Tel Type: 00b for 16-bit telemetry, 01b reserved, 10b reserved, 11b Register Readback

Mfg: 0b for SVI3-defined registers, 1b for Mfg. specific registers

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Register Offset: The register offset of the requested data
Register Data: Register data payload

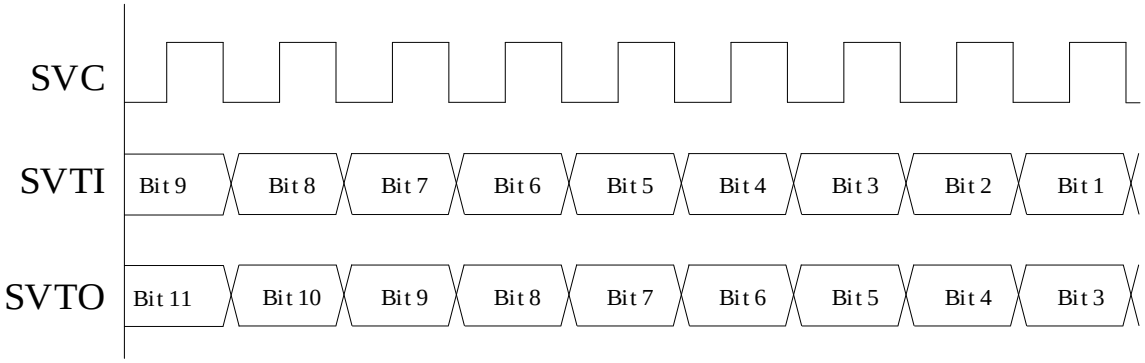

Figure 9. SVTI to SVTO Pipeline Latency

4.7 Telemetry Example

Figure 10, Figure 11, and Figure 12 illustrate a 6-target example of telemetry operation with CRC verification.

Controller (Input Only)		Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
Pipeline Mode		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
Transmit Mode			Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
Idle Transmit (1b's only)		1	1 1	1 1	1 1	1 1	1 1	1
	Clock 0	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
Target 6 initiates telemetry stream by placing start packet on bus	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 1	0
	Clock 2	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [0]	
Target 6 places Target 6 header on telemetry bus	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Start Packet [1]	Target 6 Header [7]
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	0 1	1
	Clock 10	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
	SVTI Reg:	Idle (1b)	Start Packet [0]	Target 6 Header [6]	Target 6 Header [4]	Target 6 Header [2]	Target 6 Header [0]	
Target 6 begins transmitting first telemetry packet	SVTO Reg:		Start Packet [1]	Target 6 Header [7]	Target 6 Header [5]	Target 6 Header [3]	Target 6 Header [1]	Target 6 1st Tel [15]
	SVTO | SVTI Reg:	1	0 1	1 1	0 0	0 1	1 0	X
	Clock 26	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
	SVTI Reg:	Target 6 1st Tel [10]	Target 6 1st Tel [8]	Target 6 1st Tel [6]	Target 6 1st Tel [4]	Target 6 1st Tel [2]	Target 6 1st Tel [0]	
Target 6 begins transmitting second telemetry packet	SVTO Reg:		Target 6 1st Tel [9]	Target 6 1st Tel [7]	Target 6 1st Tel [5]	Target 6 1st Tel [3]	Target 6 1st Tel [1]	Target 6 2nd Tel [15]
	SVTO | SVTI Reg:	X	X X	X X	X X	X X	X X	X
	Clock 74	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
Target 6 finishes transmitting its telemetry packet and begins transmitting Target 5 header packet	SVTI Reg:	Target 6 4th Tel [10]	Target 6 4th Tel [8]	Target 6 4th Tel [6]	Target 6 4th Tel [4]	Target 6 4th Tel [2]	Target 6 4th Tel [0]	
	SVTO Reg:		Target 6 4th Tel [9]	Target 6 4th Tel [7]	Target 6 4th Tel [5]	Target 6 4th Tel [3]	Target 6 4th Tel [1]	Target 5 Header [7]
	SVTO | SVTI Reg:	X	X X	X X	X X	X X	X X	1
	Clock 88	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
While pipelining, Target 5 reads Target 5 header & 3-bit CRC and begins transmitting its first telemetry packet	SVTI Reg:	Target 6 4th Tel [0]	Target 5 Header [2]	Target 5 Header [0]	Target 6 CRC [1]	Target 5 1st Tel [15]	Idle (1b)	
	SVTO Reg:		Target 5 Header [3]	Target 5 Header [1]	Target 6 CRC [2]	Target 6 CRC [0]	Target 5 1st Tel [14]	Idle (1b)
	SVTO | SVTI Reg:	X	0 1	0 1	X X	X X	X 1	1
	Clock 151	Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
Target 5 finishes transmitting its telemetry packet & begins transmitting Target 4 header packet	SVTI Reg:	Target 5 4th Tel [8]	Target 5 4th Tel [6]	Target 5 4th Tel [4]	Target 5 4th Tel [2]	Target 5 4th Tel [0]	Idle (1b)	
	SVTO Reg:		Target 5 4th Tel [7]	Target 5 4th Tel [5]	Target 5 4th Tel [3]	Target 5 4th Tel [1]	Target 4 Header [7]	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X X	X X	X X	1 1	1

Figure 10. Telemetry Pipeline Example (Part 1)

While pipelining, Target 4 reads Target 4 header & 3-bit CRC and begins transmitting its first telemetry packet	**Clock 165**	**Controller**	**Target 1**	**Target 2**	**Target 3**	**Target 4**	**Target 5**	**Target 6**
	SVTI Reg:	Target 4 Header [6]	Target 4 Header [0]	Target 5 CRC [1]	Target 4 1st Tel [15]	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 4 Header [1]	Target 5 CRC [2]	Target 5 CRC [0]	Target 4 1st Tel [14]	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	0 0	X X	X X	X 1	1 1	1
While pipelining, Target 1 reads Target 1 header and begins transmitting its first telemetry packet	**Clock 380**	**Controller**	**Target 1**	**Target 2**	**Target 3**	**Target 4**	**Target 5**	**Target 6**
	SVTI Reg:	Target 1 Header [0]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 1 1st Tel [15]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	X 1	1 1	1 1	1 1	1 1	1
Target 1 finishes transmitting its telemetry packet and begins transmitting Target 0 header packet	**Clock 459**	**Controller**	**Target 1**	**Target 2**	**Target 3**	**Target 4**	**Target 5**	**Target 6**
	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 0 Header [7]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 1	1
Target 1 finishes transmitting 3-bit CRC and returns to pipeline mode. Controller reads Target 0 header & 3-bit CRC, indicating end of telemetry stream	**Clock 470**	**Controller**	**Target 1**	**Target 2**	**Target 3**	**Target 4**	**Target 5**	**Target 6**
	SVTI Reg:	Target 1 CRC [0]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	0	1 1	1 1	1 1	1 1	1 1	1
	Clock 471	**Controller**	**Target 1**	**Target 2**	**Target 3**	**Target 4**	**Target 5**	**Target 6**
	SVTI Reg:	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	1 1	1 1	1 1	1 1	1 1	1

Controller (Input Only)
Pipeline Mode
Transmit Mode
Idle Transmit (1b's only)

Figure 11. Telemetry Pipeline Example (Part 2)

The controller will receive the telemetry stream shown in Figure 12.

Clock	12	20	36	52	68	84	92	95	111	127	143	159	167	170	186	202	218	234	242	245	261	277	293	309	317	320	336	352	368	384	392	395	411	427	443	459	467	470
Packet	Start	6.H	6.1	6.2	6.3	6.4	5.H	6.CRC	5.1	5.2	5.3	5.4	4.H	5.CRC	4.1	4.2	4.3	4.4	3.H	4.CRC	3.1	3.2	3.3	3.4	2.H	3.CRC	2.1	2.2	2.3	2.4	1.H	2.CRC	1.1	1.2	1.3	1.4	0.H	1.CRC

Figure 12. Telemetry Pipeline Example (Part 3) Controller

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4.8 Acknowledgements

Each target that is affected by a command (or command stream) is required to return an acknowledgement. All command types, except the global Initialization command, are expected to trigger an acknowledgement. The purpose of the acknowledgement is to confirm to the controller that a valid command was received without error by all commanded targets and that all commands are executed.

After sending a command (or stream of commands), the controller waits until receiving an acknowledgement before sending another command (stream). Acknowledgments are placed on the telemetry bus and are given priority over telemetry streaming.

4.8.1 Acknowledgement Types

There are four types of acknowledgment packets. The acknowledgement packet structure is shown below.

Packet length: 4 bits

Packet Structure:

Acknowledge			
Packet Type (00b)		ACK Response [1:0]	
3	2	1	0

Packet Type: 00b Acknowledge, 10b: Telemetry, 11b: Header packet

ACK Response: The response code of the acknowledgement

4.8.1.1 Completed ACK (01b)

A target is required to return a completed ACK if all commands were valid and executable and there were no detected communication errors.

When a completed ACK is received, it signifies to the controller that all targets can execute all commands in the previous command (stream).

4.8.1.2 NACK: Invalid Command (10b)

A target is required to return a NACK: Invalid Command packet if any command is invalid or not executable and there were no detected communication errors.

When the controller receives a NACK: Invalid Command, it indicates that at least one command from at least one target is invalid or not executable. It does not indicate a communication error.

In addition to returning a NACK packet, the target also asserts the appropriate flag in the NACK_STATUS register. Invalid Command NACKs are broken down into following sub-groups:

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Undefined Register / Command: This occurs when either the "command type" is not defined or when the register offset to be written/read is not defined. Examples: Attempting to use command type 101b; Attempting to read Register 98h (see Section 5.12).

Undefined Register / Command Payload: This occurs when the command type is valid, but the payload is undefined. It is also asserted if a Register Write command points to a valid register but the payload of that Register Write is undefined or out of the defined range. Examples: Attempting to set PSI5 (see Section 5.7); Attempting to set 0x21[4:0] LL_ADJUST greater than 10101b.

Not Executable / Not Supported: This occurs when the command, register (if applicable) and data payload are all defined but the command cannot be executed because it is logically incorrect or not supported by the target. Examples: Attempting to enable telemetry that isn't supported; Attempting to increase VID_MIN greater than VID_MAX; Attempting to write to a read-only register; Attempting to set the voltage offset such that the resultant voltage would be outside the target's supported voltage range.

4.8.1.3 NACK: Communication Error (11b)

Targets are required to return a NACK: Communication Error if any communication errors are detected, regardless of the selected target. A communication error includes a non-successful CRC verification or the absence of a proper End packet after counting the packet length.

When the controller receives a NACK: Communication Error, it indicates at least one target reported a communication error. This triggers the communication recovery procedure (see Section 4.11).

In addition to returning a NACK packet, the target also asserts the appropriate flag in the NACK_STATUS register (see Section 5.12.2). Communication Error NACKs are broken down into following sub-groups:

Framing Error: This occurs when the target perceives that the bit length of a packet is incorrect. Example: End packet not received after counted number of bits.

CRC Error: This occurs when the packet is framed properly however the CRC code (if enabled) is not correct.

Command before ACK: This occurs when the target perceives the beginning of a command before it has returned an ACK in response to a previous command or command stream.

4.8.1.4 Incomplete ACK (00b)

When the terminal target is not an ACK target, it returns an Incomplete ACK. The Incomplete ACK should be modified by one or more of the ACK targets in the daisy chain before reaching the controller.

If the controller receives an Incomplete ACK, it indicates a communication error and triggers a re-sync procedure (see Section 4.11).

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4.8.2 NACK and Command Execution

If a command causes a NACK due to any of the conditions, the command is not executed.

If an Address packet or Address/VID packet causes a NACK due to any of the conditions, the selected target doesn't change.

4.8.3 Acknowledgement Framing

Unlike command packets and telemetry packet streams, the acknowledgement packet does not require a 01b Start packet preceding it. The 00b indicates to the controller and all targets in the daisy-chain that an acknowledgement is incoming.

The end of the acknowledgement is indicated by counting a total of 4 bits.

4.8.4 Acknowledgement Operation

The acknowledgment operation rules can be split into three sections:

Terminal Target Rules: Rules for the last target in the daisy-chain

Non-Terminal Reporting Target Rules: Rules for the target presently reporting telemetry on the daisy-chain (if any)

ACK Target: Rules for any target that requires an ACK to be reported

4.8.4.1 Terminal Target Acknowledgement Operation

1. The terminal target always monitors the SVC/SVD bus for completed commands (or completed command streams) addressed to any target(s)
2. Following a stream of command packets (or an individual command), the terminal target waits two SVC clock cycles and then completes one the following cases:

Case 1: The terminal target is not the reporting target and is not an ACK target

The terminal target transmits an incomplete acknowledge packet.

Case 2: The terminal target is not the reporting target and is an ACK target.

The terminal target transmits the appropriate ACK (or NACK) packet.

Case 3: The terminal target is the reporting target and is not an ACK target.

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The terminal target finishes reporting its present start/header/telemetry packet,[1] immediately transmits an incomplete acknowledge, and immediately resumes reporting the next scheduled packet.

Case 4: The terminal target is the reporting target and is an ACK target.

The terminal target finishes reporting its present start/header/telemetry packet,[1] immediately transmits the appropriate ACK/NACK, and immediately resumes reporting the next scheduled packet

4.8.4.2 Non-Terminal Reporting Target Acknowledgement Operation

When a non-terminal reporting target detects an incoming acknowledge packet on the SVTI input, while reporting on the SVTO output, it completes the following:

1. Begins queuing acknowledge packet bits into a separate 4-bit FIFO buffer
2. Finishes transmitting the present packet[2]
3. Immediately begins de-queuing and transmitting the buffered acknowledge packet until the buffer is empty[3]
4. Immediately continues transmitting its next telemetry packet[3]

[1] If the terminal target is reporting the N-1 header packet and CRC verification is enabled, the terminal target waits until the 3-bit CRC packet is transmitted before transmitting the incomplete acknowledge packet.

[2] If the target is reporting a header packet and CRC verification is enabled, the target waits until the 3-bit CRC packet is transmitted before dequeuing and transmitting the buffered acknowledgement packet.

[3] If the reporting target is also an ACK Target it modifies the buffered acknowledgment packet, as described in Section 4.8.4.3.

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4.8.4.3 ACK Target Rules

When an ACK target is not the terminal target, the ACK target pipelines any incoming ACK packets while modifying the outgoing packet bits based on truth as shown in Table 9.

Table 9. ACK Truth Table

Input				Output	
ACK Type (Target)		**Pipeline In ACK**		**Pipeline Out ACK**	
Bit 1	Bit 0	Bit 1	Bit 0	Bit 1	Bit 0
0	1	0	X	0	1
0	1	1	0	1	0
1	0	0	X	1	0
1	1	X	X	1	1
1	0	1	0	1	0
X	X	1	1	1	1

The truth table ensures that the following priority is maintained:

1. NACK: Communication Error (highest priority)
2. NACK: Invalid Command
3. Completed ACK
4. Incomplete ACK (lowest priority)

If the ACK target is reporting when an ACK/NACK is required, the target finishes reporting its present packet before transmitting the appropriate ACK/NACK.[4]

4.8.5 CRC Verification and Acknowledgements

As mentioned in Section 4.3.2, each target transmits a 3-bit CRC code (if enabled) based on the packets it reported (including header packets). Regardless of where acknowledgement packets are inserted in the telemetry stream, CRC codes do not consider the bits of acknowledgement packets.

4.8.6 Acknowledgement Example

Figure 13 -Figure 16 illustrates an acknowledgement example with 6 targets with CRC verification. Target 2 is in the process of reporting its telemetry and target 4 requires an Acknowledgement.

[4] If the target is reporting a header packet and CRC verification is enabled, the target waits until the 3-bit CRC packet is transmitted before transmitting the acknowledgement packet.

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Controller (Input Only)	Clock 318	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
Pipeline Mode	SVTI Reg:	Target 3 CRC [2]		Salve 3 CRC [0]		Idle (1b)		Idle (1b)		Idle (1b)		Idle (1b)			
Report / Transmit Mode	SVTO Reg:			Target 3 CRC [1]		Target 2 1st Tel [15]		Idle (1b)		Idle (1b)		Idle (1b)		Idle (1b)	
Idle Transmit (1b's only)	SVTO | SVTI Reg:		X	X	X	X	1	1	1	1	1	1	1	1	
Ack Required															
	Clock 319	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
Target 4 ACK required; Target 6 begins transmitting Incomplete ACK on SVT bus	SVTI Reg:	Target 2 Header [1]		Target 2 1st Tel [15]		Idle (1b)		Idle (1b)		Idle (1b)		Idle (1b)			
	SVTO Reg:			Target 2 Header [0]		Target 2 1st Tel [14]		Idle (1b)		Idle (1b)		Idle (1b)		Acknowledge [3]	
	SVTO | SVTI Reg:		1	0	X	X	1	1	1	1	1	1	1	0	
	Clock 320	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
	SVTI Reg:	Target 2 Header [0]		Target 2 1st Tel [14]		Idle (1b)		Idle (1b)		Idle (1b)		Acknowledge [3]			
	SVTO Reg:			Target 2 1st Tel [15]		Target 2 1st Tel [13]		Idle (1b)		Idle (1b)		Idle (1b)		Acknowledge [2]	
	SVTO | SVTI Reg:		0	X	X	X	1	1	1	1	1	1	0	0	
	Clock 321	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
	SVTI Reg:	Target 2 1st Tel [15]		Target 2 1st Tel [13]		Idle (1b)		Idle (1b)		Idle (1b)		Acknowledge [2]			
	SVTO Reg:			Target 2 1st Tel [14]		Target 2 1st Tel [12]		Idle (1b)		Idle (1b)		Acknowledge [3]		Acknowledge [1]	
	SVTO | SVTI Reg:		X	X	X	X	1	1	1	1	1	0	0	0	
	Clock 322	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
	SVTI Reg:	Target 2 1st Tel [14]		Target 2 1st Tel [12]		Idle (1b)		Idle (1b)		Acknowledge [3]		Acknowledge [1]			
	SVTO Reg:			Target 2 1st Tel [13]		Target 2 1st Tel [12]		Idle (1b)		Idle (1b)		Acknowledge [2]		Acknowledge [0]	
	SVTO | SVTI Reg:		X	X	X	X	1	1	1	0	0	0	0	0	
	Clock 323	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
	SVTI Reg:	Target 2 1st Tel [13]		Target 2 1st Tel [11]		Idle (1b)		Idle (1b)		Acknowledge [2]		Acknowledge [0]			
	SVTO Reg:			Target 2 1st Tel [12]		Target 2 1st Tel [10]		Idle (1b)		Acknowledge [3]		Acknowledge [1]		Idle (1b)	
	SVTO | SVTI Reg:		X	X	X	X	1	1	1	0	0	0	0	1	
	Clock 324	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
	SVTI Reg:	Target 2 1st Tel [12]		Target 2 1st Tel [10]		Idle (1b)		Acknowledge [3]		Acknowledge [1]		Idle (1b)			
	SVTO Reg:			Target 2 1st Tel [11]		Target 2 1st Tel [9]		Idle (1b)		Acknowledge [2]		Acknowledge [0]		Idle (1b)	
	SVTO | SVTI Reg:		X	X	X	X	1	1	0	0	0	0	1	1	
	Clock 325	Controller		Target 1		Target 2		Target 3		Target 4		Target 5		Target 6	
	SVTI Reg:	Target 2 1st Tel [11]		Target 2 1st Tel [9]		Idle (1b)		Acknowledge [2]		Acknowledge [0]		Idle (1b)			
Target 4 detects incomplete ACK packet	SVTO Reg:			Target 2 1st Tel [10]		Target 2 1st Tel [8]		Acknowledge [3]		Acknowledge [1]		Idle (1b)		Idle (1b)	
	SVTO | SVTI Reg:		X	X	X	X	1	0	0	0	0	1	1	1	

Figure 13. Acknowledgement Example (Part 1)

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		Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
Target 4 converts ACK Response [0] from 0b to 1b, indicating "Completed ACK"; Target 2 begins enqueuing ACK	Clock 326							
	SVTI Reg:	Target 2 1st Tel [10]	Target 2 1st Tel [8]	Acknowledge [3]	Acknowledge [1]	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [9]	Target 2 1st Tel [7]	Acknowledge [2]	Acknowledge [0]	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X 0	0 0	1 1	1 1	1
	Clock 327							
	SVTI Reg:	Target 2 1st Tel [9]	Target 2 1st Tel [7]	Acknowledge [2]	Acknowledge [0]	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [8]	Target 2 1st Tel [6]	Acknowledge [1]	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X 0	0 1	1 1	1 1	1
	Clock 328							
	SVTI Reg:	Target 2 1st Tel [8]	Target 2 1st Tel [6]	Acknowledge [1]	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [7]	Target 2 1st Tel [5]	Acknowledge [0]	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X 0	1 1	1 1	1 1	1
	Clock 329							
	SVTI Reg:	Target 2 1st Tel [7]	Target 2 1st Tel [5]	Acknowledge [0]	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [6]	Target 2 1st Tel [4]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X 1	1 1	1 1	1 1	1
	Clock 330							
	SVTI Reg:	Target 2 1st Tel [6]	Target 2 1st Tel [4]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [5]	Target 2 1st Tel [3]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X 1	1 1	1 1	1 1	1
Target 2 finishes transmitting its present packet and begins de-queuing acknowledge packet	Clock 331							
	SVTI Reg:	Target 2 1st Tel [2]	Target 2 1st Tel [0]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [1]	Acknowledge [3]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	0 1	1 1	1 1	1 1	1
	Clock 332							
	SVTI Reg:	Target 2 1st Tel [1]	Acknowledge [3]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 1st Tel [0]	Acknowledge [2]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X 0	0 1	1 1	1 1	1 1	1
	Clock 333							
	SVTI Reg:	Target 2 1st Tel [0]	Acknowledge [2]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Acknowledge [3]	Acknowledge [1]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	0 0	0 1	1 1	1 1	1 1	1

Figure 14. Acknowledgement Example (Part 2)

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		Controller	Target 1	Target 2	Target 3	Target 4	Target 5	Target 6
Target 2 finishes de-queuing acknowledge packet	Clock 334							
	SVTI Reg:	Acknowledge [3]	Acknowledge [1]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Acknowledge [2]	Acknowledge [0]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	0	0 0	1 1	1 1	1 1	1 1	1
Target 2 begins transmitting next telemetry packet	Clock 335							
	SVTI Reg:	Acknowledge [2]	Acknowledge [0]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Acknowledge [1]	Target 2 2nd Tel [15]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	0	0 1	X 1	1 1	1 1	1 1	1
	Clock 336							
	SVTI Reg:	Acknowledge [1]	Target 2 2nd Tel [15]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Acknowledge [0]	Target 2 2nd Tel [14]	Acknowledge [0]	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	0	1 X	X 1	1 1	1 1	1 1	1
Controller accepts acknowledgement	Clock 337							
	SVTI Reg:	Acknowledge [0]	Target 2 2nd Tel [14]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 2nd Tel [15]	Target 2 2nd Tel [13]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	1	X X	X 1	1 1	1 1	1 1	1
	Clock 338							
	SVTI Reg:	Target 2 2nd Tel [15]	Target 2 2nd Tel [13]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)	
	SVTO Reg:		Target 2 2nd Tel [14]	Target 2 2nd Tel [12]	Idle (1b)	Idle (1b)	Idle (1b)	Idle (1b)
	SVTO | SVTI Reg:	X	X X	X 1	1 1	1 1	1 1	1

Controller (Input Only)
Pipeline Mode
Report / Transmit Mode
Idle Transmit (1b's only)
Ack Required

Figure 15. Acknowledgement Example (Part 3)

The controller receives the telemetry stream with the ACK inserted as shown in Figure 16.

Clock	12	20	36	52	68	84	92	95	111	127	143	159	167	170	186	202	218	234	242	245	261	277	293	309	317	320	336	340	356	372	388	396	399	415	431	447	463	471	474
Packet	Start	6.H	6.1	6.2	6.3	6.4	5.H	6.CRC	5.1	5.2	5.3	5.4	4.H	5.CRC	4.1	4.2	4.3	4.4	3.H	4.CRC	3.1	3.2	3.3	3.4	2.H	3.CRC	2.1	4.ACK	2.2	2.3	2.4	1.H	2.CRC	1.1	1.2	1.3	1.4	0.H	1.CRC

Figure 16. Acknowledgement Example (Part 4)

4.9 SVI3 Interface Disabled State

To save power or to prevent against glitching during certain power state transitions, the entire SVI3 interface may be placed into a disabled state by holding SVC high. For voltage regulators, disabling/enabling the SVI3 interface does not have any effect on voltage regulation.

4.9.1 SVI3 Interface Disable Procedure

The step-by-step SVI3 interface disable procedure is as follows:

1. The controller holds SVC high for at least $t_{SVC\_timeout\ (max)}$ (see Table 6), causing all SVI3 targets to timeout.
   ***Note**: Holding SVC high for more than $th_{igh\ (max)}$ and less then $t_{SVC\_timeout\ (max)}$ is invalid.*
2. Upon registering a time out, the target disables all SVI3 decoder logic. All SVTO signals are pulled high.
   a. Any command packet that was in the process of being transmitted is discarded
   b. Any telemetry that was in the process of being reported/pipelined is immediately discarded
   c. All pending Register Read requests are cleared
   d. All pending ACKs/NACKs are cleared
   e. Any ongoing initialization is aborted

4.9.2 SVI3 Interface Enable Procedure

The step-by-step SVI3 interface enable procedure is as follows:

1. The controller toggles the SVC clock for at least N_{INIT} clock cycles (see Table 7).
2. Each target only listens to SVD after registering N_{INIT} consecutive valid clock cycles. Clock timeouts ($t_{SVC\_timeout}$) resets this count.
3. Following N_{INIT} consecutive valid clock cycles, the SVI3 interface is considered enabled:
   a. Command packets can be decoded and executed.
   b. Telemetry is available to request.

4.10 SVI3_VDDIO Power-down/Power-up

Following the SVI3 interface being disabled (see Section 4.9.1), SVI3_VDDIO may be powered down.

While SVI3_VDDIO is powered down:

- SVI3 communication is disabled.
- For voltage regulation devices, voltage regulation is unaffected by powering down SVI3_VDDIO.

- Provided that SVI3_RESET_L remains de-asserted, the state of SVI3-defined registers is unaffected by powering down SVI3_VDDIO.
- If SVI3_RESET_L becomes asserted, all SVI3-defined registers return to their respective default state.

The power-up sequence of SVI3_VDDIO is identical to steps 2-6 of the Bus Initialization Sequence (see Section 4.4.1).

Figure 17 shows an example of a system powering-down and powering-up SVI3_VDDIO while keeping SVI3_RESET_L de-asserted.

As shown in Figure 17, the sequence of events is as follows:

1. SVC is held high for $t_{SVC\_timeout}$ causing the SVI3 interface to be disabled.
2. SVI3_VDDIO is powered down. SVC, SVD, SVTO go low. VCC remains powered. SVI3_RESET_L remains de-asserted. Voltage regulation operation is unaffected.
3. SVI3_VDDIO is powered up and within regulation.
4. The detection of SVI3_VDDIO entering regulation triggers a POR (power-on reset) of the communication bus by the targets. The communication bus holds in reset for $T_{SVI3\_VDDIO\text{-}SVI3\_POR}$. The POR affects the state of the SVI3-defined registers.
5. SVC, SVD and all instances of SVTO are high and stable within a maximum of $T_{SVI3\_VDDIO\text{-}SVC\_SVD\_SVTO}$ after SVI3_VDDIO is within regulation.
6. SVC begins toggling after a minimum of $T_{SVI3\_VDDIO\text{-}SVC\_START}$ after SVI3_VDDIO enters regulation.
7. SVD remains high for at least $T_{SVC\_START\text{-}INIT\_START}$. Following this, the SVI3 Interface is enabled, and the controller may initiate SVD commands after this time.

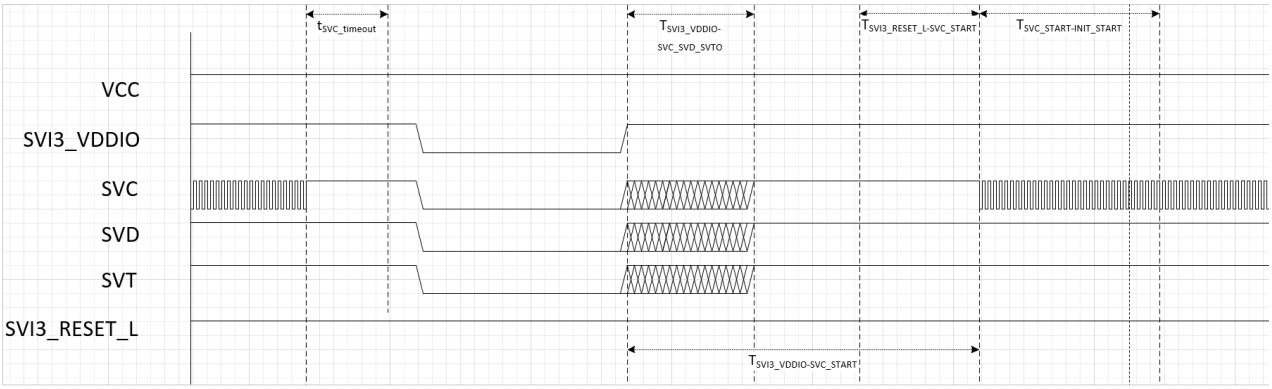

Figure 17. Example of SVI3_VDDIO Power-Down and Power-Up

4.11 Communication Error Catching and Recovery

A target detects a communication error if any of the following conditions occur:

1. A packet starts with any combination of bits other than the two-bit Start packet (01b).
2. After the expected number of packet bits, the target observes any combination of bits other than the two-bit End packet (10b).
3. CRC verification does not match (if enabled).

Following the detection of a communication error, the following sequence occurs:

1. The target does not execute the mis-communicated command packet.
2. Every target that detects the communication error immediately returns a NACK: Communication Error
3. When the controller receives a NACK: Communication Error, it immediately ceases issuing any further command packets and holds SVC high for $t_{SVC\_timeout}$. As described in Section 4.9.1, this action puts the SVI3 bus in disabled state and resets all target decoding state machines.
4. Following $t_{SVC\_timeout}$, the controller performs the SVI3 interface enable procedure described in Section 4.9.2.
5. Following the SVI3 interface enable procedure, command packets may be sent from the controller.

Chapter 5 Design Criteria for Type 1 Devices: Multi-Phase Step-Down Switching Voltage Regulators

5.1 Definition of Type 1 Device

For clarity, packaged ICs for the purpose of controlling voltage regulation (i.e. voltage regulator controllers) are referred to as *voltage regulator devices* or *devices*. To be classified as a Type 1 device, all of the following criteria must be true:

- The regulator must be a switching step-down DC-DC converter topology
- The device may regulate one or more rails
- At least one rail must have more than one phase

5.2 Required Signals and Descriptions

The required signals for Type 1 devices are listed in Table 10. These signals are in addition to signals defined in Section 3.1.

Table 10. Type 1 Target Required Signals

Signal	I/O	Description
OCP_L	Output	One required per device; open-drain, active-low output; Asserted when current is greater than I_IN_WARN_THRESH *optional*, OCP_THRESH or OCP_WARN_THRESH
P_SYS *optional on non-mobile controllers*	Input	One per device; Analog input; signal from battery charger or system power monitor representing total system power; resistor from pin to ground sets gain
PWR_ENABLE	Input	One required per rail; Active high signal to enable voltage regulation
PWRGD	Output	One required per rail; Active high, open-drain signal to indicate to system that rail is enabled, within regulation and has no faults
VCC	Input (Power)	One required per device; Device logic voltage
VDD_SENSE	Input	One required per rail; Analog input; Positive remote voltage sense of rail
VSS_SENSE	Input	Minimum one required per device; Analog input; Negative remote voltage sense of rail; One input may be shared for multiple rails

5.3 Electrical Requirements

Table 11. Type 1 Device Electrical Requirements

Parameter	Description	Min.	Typ.	Max.	Units	Note
$I_{leak\text{-}Pin}$	Leakage ENABLE/PWRGD/OCP_L pin	-10		10	µA	
PWR_ENABLE V_{IH}	Enable input high voltage	1.17			V	1
PWR_ENABLE V_{IL}	Enable input low voltage			0.63	V	1
PWRGD / OCP_L V_{OL}	PWRGD and OCP_L output low voltage, I_{OL}= 8 mA			0.2	V	
P_SYS Max Voltage	Full scale voltage of system power (P_SYS) ADC		1.2		V	

Notes:

1. *The PWR_ENABLE pin must be operable at 3.3V + 10%.*

5.4 Power-Up Sequencing

The power up sequence of a regulated rail is as follows:

1. VCC voltage is powered on and in regulation.
2. The target copies the default voltage and the default slew rate to the target VID and slew rate registers respectively. As described in Section 5.12.3, VID is set by VID_DEFAULT_VOLTAGE and UP_SLEW_RATE is set by DEFAULT_SLEW_RATE.
   a. If SVI3 interface is initialized, the target VID and slew rate may be over-written before the PWR_ENABLE pin is asserted.
3. The PWR_ENABLE pin is asserted.
4. The output voltage begins ramping up to the target VID at the UP_SLEW_RATE.
5. PWRGD is asserted after the output voltage is within tolerance and start-up ramping is complete.

   Note: *It is not required that SVI3_VDDIO be within regulation or the SVI3 bus be initialized to initiate the power-up sequence.*

5.4.1 Default Voltage

The Default Voltage is used as the target's initial VID value. At first VCC power-on, targets copy the Default Voltage's effective 9-bit VID value to the target's VID register. When SVI3_RESET_L is asserted, targets copy the Default Voltage's effective 9-bit value to the target's VID register.

The Default Voltage is programmed at the platform level (through NVM, board-level resistor strapping). The required programmable Default Voltage set is shown in Table 12.

Table 12. Type 1 Default Voltages

Value	Default Voltage (V)
0h	Off (Wait for SVI3 cmd.)
1h	0.500
2h	0.600
3h	0.700
4h	0.800
5h	0.900
6h	1.000
7h	1.100
8h	1.200
9h	1.300
Ah	1.400
Bh	1.500
Ch	1.800
Dh	2.000
Eh	2.500
Fh	2.800

5.4.2 Default Slew Rate

The Default Slew Rate is used as the default value for the target's programmable slew rate value UP_SLEW_RATE (see Section 5.12.3). At first VCC power-on, targets copy the Default Slew Rate's effective value to the target's slew rate register UP_SLEW_RATE. When SVI3_RESET_L is asserted, targets copies the Default Slew Rate's effective value to the target's slew rate register.

The Default Slew Rate is programmed at the platform level (through NVM, board-level resistor strapping). The required programmable Default Voltage Slew Rate set is shown in Table 13.

Table 13. Default Slew Rate

Value	Default Slew Rate (mV/µs)
00b	2.5
01b	10
10b	20
11b	40

5.4.3 Power-Up Timing Requirements

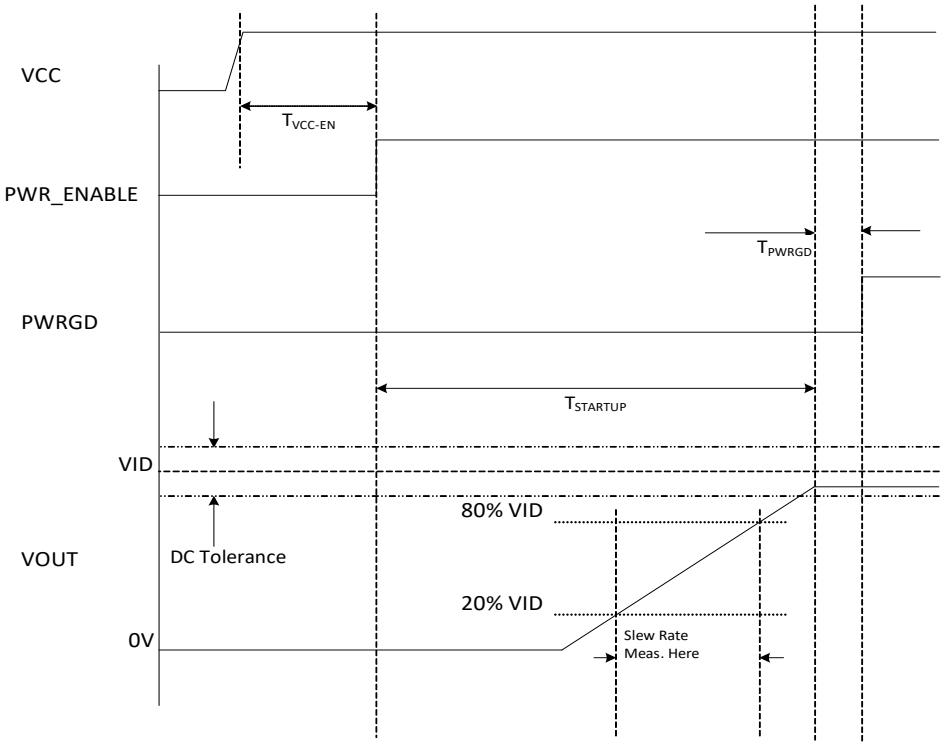

Figure 18. Power Up Sequencing

Table 14. Power-up Sequencing Requirements

Parameter	Description	Min.	Typ.	Max.	Units
T_{VCC-EN}	Time from VCC stable to assertion of PWR_ENABLE	5			ms
Slew Rate	Measured slew rate during power up sequencing	Typ. – 10%	Programmed (UP_SLEW_RATE)	Typ. + 10%	mV/µs
$T_{STARTUP}$	Time from PWR_ENABLE assertion to instant that output voltage is within regulation and is finished slewing			VID / Min. Slew Rate + Max of [500, (10000 - T_{VCC-EN})]	µs
T_{PWRGD}	Time from instant that output voltage is within regulation and is finished slewing to PWRGD assertion			5	µs

5.5 Output Voltage

It is required that all Type 1 voltage regulators be capable of supporting the entire range of the VID table (see Table 15 through Table 18) within the accuracy specifications described in Section 5.5.5.

Voltage regulators may support lower/higher voltages than those described in the table. Setting target voltages beyond the VID table is supported using a programmable offset described in Section 5.5.4.

5.5.1 VID Table

Table 15. Type 1 Target VID Table (Part 1)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
000000000	000	OFF	000100000	020	0.405	001000000	040	0.565	001100000	060	0.725
000000001	001	0.250	000100001	021	0.410	001000001	041	0.570	001100001	061	0.730
000000010	002	0.255	000100010	022	0.415	001000010	042	0.575	001100010	062	0.735
000000011	003	0.260	000100011	023	0.420	001000011	043	0.580	001100011	063	0.740
000000100	004	0.265	000100100	024	0.425	001000100	044	0.585	001100100	064	0.745
000000101	005	0.270	000100101	025	0.430	001000101	045	0.590	001100101	065	0.750
000000110	006	0.275	000100110	026	0.435	001000110	046	0.595	001100110	066	0.755
000000111	007	0.280	000100111	027	0.440	001000111	047	0.600	001100111	067	0.760
000001000	008	0.285	000101000	028	0.445	001001000	048	0.605	001101000	068	0.765
000001001	009	0.290	000101001	029	0.450	001001001	049	0.610	001101001	069	0.770
000001010	00A	0.295	000101010	02A	0.455	001001010	04A	0.615	001101010	06A	0.775
000001011	00B	0.300	000101011	02B	0.460	001001011	04B	0.620	001101011	06B	0.780
000001100	00C	0.305	000101100	02C	0.465	001001100	04C	0.625	001101100	06C	0.785
000001101	00D	0.310	000101101	02D	0.470	001001101	04D	0.630	001101101	06D	0.790
000001110	00E	0.315	000101110	02E	0.475	001001110	04E	0.635	001101110	06E	0.795
000001111	00F	0.320	000101111	02F	0.480	001001111	04F	0.640	001101111	06F	0.800
000010000	010	0.325	000110000	030	0.485	001010000	050	0.645	001110000	070	0.805
000010001	011	0.330	000110001	031	0.490	001010001	051	0.650	001110001	071	0.810
000010010	012	0.335	000110010	032	0.495	001010010	052	0.655	001110010	072	0.815
000010011	013	0.340	000110011	033	0.500	001010011	053	0.660	001110011	073	0.820
000010100	014	0.345	000110100	034	0.505	001010100	054	0.665	001110100	074	0.825
000010101	015	0.350	000110101	035	0.510	001010101	055	0.670	001110101	075	0.830
000010110	016	0.355	000110110	036	0.515	001010110	056	0.675	001110110	076	0.835
000010111	017	0.360	000110111	037	0.520	001010111	057	0.680	001110111	077	0.840
000011000	018	0.365	000111000	038	0.525	001011000	058	0.685	001111000	078	0.845
000011001	019	0.370	000111001	039	0.530	001011001	059	0.690	001111001	079	0.850
000011010	01A	0.375	000111010	03A	0.535	001011010	05A	0.695	001111010	07A	0.855
000011011	01B	0.380	000111011	03B	0.540	001011011	05B	0.700	001111011	07B	0.860
000011100	01C	0.385	000111100	03C	0.545	001011100	05C	0.705	001111100	07C	0.865
000011101	01D	0.390	000111101	03D	0.550	001011101	05D	0.710	001111101	07D	0.870
000011110	01E	0.395	000111110	03E	0.555	001011110	05E	0.715	001111110	07E	0.875
000011111	01F	0.400	000111111	03F	0.560	001011111	05F	0.720	001111111	07F	0.880

Table 16. Type 1 Target VID Table (Part 2)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
010000000	080	0.885	010100000	0A0	1.045	011000000	0C0	1.205	011100000	0E0	1.365
010000001	081	0.890	010100001	0A1	1.050	011000001	0C1	1.210	011100001	0E1	1.370
010000010	082	0.895	010100010	0A2	1.055	011000010	0C2	1.215	011100010	0E2	1.375
010000011	083	0.900	010100011	0A3	1.060	011000011	0C3	1.220	011100011	0E3	1.380
010000100	084	0.905	010100100	0A4	1.065	011000100	0C4	1.225	011100100	0E4	1.385
010000101	085	0.910	010100101	0A5	1.070	011000101	0C5	1.230	011100101	0E5	1.390
010000110	086	0.915	010100110	0A6	1.075	011000110	0C6	1.235	011100110	0E6	1.395
010000111	087	0.920	010100111	0A7	1.080	011000111	0C7	1.240	011100111	0E7	1.400
010001000	088	0.925	010101000	0A8	1.085	011001000	0C8	1.245	011101000	0E8	1.405
010001001	089	0.930	010101001	0A9	1.090	011001001	0C9	1.250	011101001	0E9	1.410
010001010	08A	0.935	010101010	0AA	1.095	011001010	0CA	1.255	011101010	0EA	1.415
010001011	08B	0.940	010101011	0AB	1.100	011001011	0CB	1.260	011101011	0EB	1.420
010001100	08C	0.945	010101100	0AC	1.105	011001100	0CC	1.265	011101100	0EC	1.425
010001101	08D	0.950	010101101	0AD	1.110	011001101	0CD	1.270	011101101	0ED	1.430
010001110	08E	0.955	010101110	0AE	1.115	011001110	0CE	1.275	011101110	0EE	1.435
010001111	08F	0.960	010101111	0AF	1.120	011001111	0CF	1.280	011101111	0EF	1.440
010010000	090	0.965	010110000	0B0	1.125	011010000	0D0	1.285	011110000	0F0	1.445
010010001	091	0.970	010110001	0B1	1.130	011010001	0D1	1.290	011110001	0F1	1.450
010010010	092	0.975	010110010	0B2	1.135	011010010	0D2	1.295	011110010	0F2	1.455
010010011	093	0.980	010110011	0B3	1.140	011010011	0D3	1.300	011110011	0F3	1.460
010010100	094	0.985	010110100	0B4	1.145	011010100	0D4	1.305	011110100	0F4	1.465
010010101	095	0.990	010110101	0B5	1.150	011010101	0D5	1.310	011110101	0F5	1.470
010010110	096	0.995	010110110	0B6	1.155	011010110	0D6	1.315	011110110	0F6	1.475
010010111	097	1.000	010110111	0B7	1.160	011010111	0D7	1.320	011110111	0F7	1.480
010011000	098	1.005	010111000	0B8	1.165	011011000	0D8	1.325	011111000	0F8	1.485
010011001	099	1.010	010111001	0B9	1.170	011011001	0D9	1.330	011111001	0F9	1.490
010011010	09A	1.015	010111010	0BA	1.175	011011010	0DA	1.335	011111010	0FA	1.495
010011011	09B	1.020	010111011	0BB	1.180	011011011	0DB	1.340	011111011	0FB	1.500
010011100	09C	1.025	010111100	0BC	1.185	011011100	0DC	1.345	011111100	0FC	1.505
010011101	09D	1.030	010111101	0BD	1.190	011011101	0DD	1.350	011111101	0FD	1.510
010011110	09E	1.035	010111110	0BE	1.195	011011110	0DE	1.355	011111110	0FE	1.515
010011111	09F	1.040	010111111	0BF	1.200	011011111	0DF	1.360	011111111	0FF	1.520

Table 17. Type 1 Target VID Table (Part 3)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
100000000	100	1.525	100100000	120	1.685	101000000	140	1.845	101100000	160	2.005
100000001	101	1.530	100100001	121	1.690	101000001	141	1.850	101100001	161	2.010
100000010	102	1.535	100100010	122	1.695	101000010	142	1.855	101100010	162	2.015
100000011	103	1.540	100100011	123	1.700	101000011	143	1.860	101100011	163	2.020
100000100	104	1.545	100100100	124	1.705	101000100	144	1.865	101100100	164	2.025
100000101	105	1.550	100100101	125	1.710	101000101	145	1.870	101100101	165	2.030
100000110	106	1.555	100100110	126	1.715	101000110	146	1.875	101100110	166	2.035
100000111	107	1.560	100100111	127	1.720	101000111	147	1.880	101100111	167	2.040
100001000	108	1.565	100101000	128	1.725	101001000	148	1.885	101101000	168	2.045
100001001	109	1.570	100101001	129	1.730	101001001	149	1.890	101101001	169	2.050
100001010	10A	1.575	100101010	12A	1.735	101001010	14A	1.895	101101010	16A	2.055
100001011	10B	1.580	100101011	12B	1.740	101001011	14B	1.900	101101011	16B	2.060
100001100	10C	1.585	100101100	12C	1.745	101001100	14C	1.905	101101100	16C	2.065
100001101	10D	1.590	100101101	12D	1.750	101001101	14D	1.910	101101101	16D	2.070
100001110	10E	1.595	100101110	12E	1.755	101001110	14E	1.915	101101110	16E	2.075
100001111	10F	1.600	100101111	12F	1.760	101001111	14F	1.920	101101111	16F	2.080
100010000	110	1.605	100110000	130	1.765	101010000	150	1.925	101110000	170	2.085
100010001	111	1.610	100110001	131	1.770	101010001	151	1.930	101110001	171	2.090
100010010	112	1.615	100110010	132	1.775	101010010	152	1.935	101110010	172	2.095
100010011	113	1.620	100110011	133	1.780	101010011	153	1.940	101110011	173	2.100
100010100	114	1.625	100110100	134	1.785	101010100	154	1.945	101110100	174	2.105
100010101	115	1.630	100110101	135	1.790	101010101	155	1.950	101110101	175	2.110
100010110	116	1.635	100110110	136	1.795	101010110	156	1.955	101110110	176	2.115
100010111	117	1.640	100110111	137	1.800	101010111	157	1.960	101110111	177	2.120
100011000	118	1.645	100111000	138	1.805	101011000	158	1.965	101111000	178	2.125
100011001	119	1.650	100111001	139	1.810	101011001	159	1.970	101111001	179	2.130
100011010	11A	1.655	100111010	13A	1.815	101011010	15A	1.975	101111010	17A	2.135
100011011	11B	1.660	100111011	13B	1.820	101011011	15B	1.980	101111011	17B	2.140
100011100	11C	1.665	100111100	13C	1.825	101011100	15C	1.985	101111100	17C	2.145
100011101	11D	1.670	100111101	13D	1.830	101011101	15D	1.990	101111101	17D	2.150
100011110	11E	1.675	100111110	13E	1.835	101011110	15E	1.995	101111110	17E	2.155
100011111	11F	1.680	100111111	13F	1.840	101011111	15F	2.000	101111111	17F	2.160

Table 18. Type 1 Target VID Table (Part 4)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
110000000	180	2.165	110100000	1A0	2.325	111000000	1C0	2.485	111100000	1E0	2.645
110000001	181	2.170	110100001	1A1	2.330	111000001	1C1	2.490	111100001	1E1	2.650
110000010	182	2.175	110100010	1A2	2.335	111000010	1C2	2.495	111100010	1E2	2.655
110000011	183	2.180	110100011	1A3	2.340	111000011	1C3	2.500	111100011	1E3	2.660
110000100	184	2.185	110100100	1A4	2.345	111000100	1C4	2.505	111100100	1E4	2.665
110000101	185	2.190	110100101	1A5	2.350	111000101	1C5	2.510	111100101	1E5	2.670
110000110	186	2.195	110100110	1A6	2.355	111000110	1C6	2.515	111100110	1E6	2.675
110000111	187	2.200	110100111	1A7	2.360	111000111	1C7	2.520	111100111	1E7	2.680
110001000	188	2.205	110101000	1A8	2.365	111001000	1C8	2.525	111101000	1E8	2.685
110001001	189	2.210	110101001	1A9	2.370	111001001	1C9	2.530	111101001	1E9	2.690
110001010	18A	2.215	110101010	1AA	2.375	111001010	1CA	2.535	111101010	1EA	2.695
110001011	18B	2.220	110101011	1AB	2.380	111001011	1CB	2.540	111101011	1EB	2.700
110001100	18C	2.225	110101100	1AC	2.385	111001100	1CC	2.545	111101100	1EC	2.705
110001101	18D	2.230	110101101	1AD	2.390	111001101	1CD	2.550	111101101	1ED	2.710
110001110	18E	2.235	110101110	1AE	2.395	111001110	1CE	2.555	111101110	1EE	2.715
110001111	18F	2.240	110101111	1AF	2.400	111001111	1CF	2.560	111101111	1EF	2.720
110010000	190	2.245	110110000	1B0	2.405	111010000	1D0	2.565	111110000	1F0	2.725
110010001	191	2.250	110110001	1B1	2.410	111010001	1D1	2.570	111110001	1F1	2.730
110010010	192	2.255	110110010	1B2	2.415	111010010	1D2	2.575	111110010	1F2	2.735
110010011	193	2.260	110110011	1B3	2.420	111010011	1D3	2.580	111110011	1F3	2.740
110010100	194	2.265	110110100	1B4	2.425	111010100	1D4	2.585	111110100	1F4	2.745
110010101	195	2.270	110110101	1B5	2.430	111010101	1D5	2.590	111110101	1F5	2.750
110010110	196	2.275	110110110	1B6	2.435	111010110	1D6	2.595	111110110	1F6	2.755
110010111	197	2.280	110110111	1B7	2.440	111010111	1D7	2.600	111110111	1F7	2.760
110011000	198	2.285	110111000	1B8	2.445	111011000	1D8	2.605	111111000	1F8	2.765
110011001	199	2.290	110111001	1B9	2.450	111011001	1D9	2.610	111111001	1F9	2.770
110011010	19A	2.295	110111010	1BA	2.455	111011010	1DA	2.615	111111010	1FA	2.775
110011011	19B	2.300	110111011	1BB	2.460	111011011	1DB	2.620	111111011	1FB	2.780
110011100	19C	2.305	110111100	1BC	2.465	111011100	1DC	2.625	111111100	1FC	2.785
110011101	19D	2.310	110111101	1BD	2.470	111011101	1DD	2.630	111111101	1FD	2.790
110011110	19E	2.315	110111110	1BE	2.475	111011110	1DE	2.635	111111110	1FE	2.795
110011111	19F	2.320	110111111	1BF	2.480	111011111	1DF	2.640	111111111	1FF	2.800

5.5.2 Voltage-on-the-Fly (VOTF) Timing

The SVI3 interface can command voltage rails to change voltage while in regulation by programming the target VID.

Positive VID transitions (transitioning from a lower voltage to a higher voltage) results in the output voltage increasing at a programmable slew rate. One register controls the slew rate for both start-up sequencing and VID transitions.

The VOTF timing and slew rate accuracy requirements are described in Figure 19 and Table 19.

Negative VID transitions do not have a specified slew rate tolerance. However, when VID decay is disabled (see Section 5.5.2.1), the negative slew rate target should be that of the positive voltage slew rate or 1/4 that of the positive slew rate, dependent on the register setting. Negative VID transitions shall not result in the output voltage undershooting the target VID beyond the specified DC tolerance.

If a new VID is commanded while the voltage is already transitioning from a previous VID command, the voltage regulator ACKs the command and transitions toward the most recent commanded voltage.

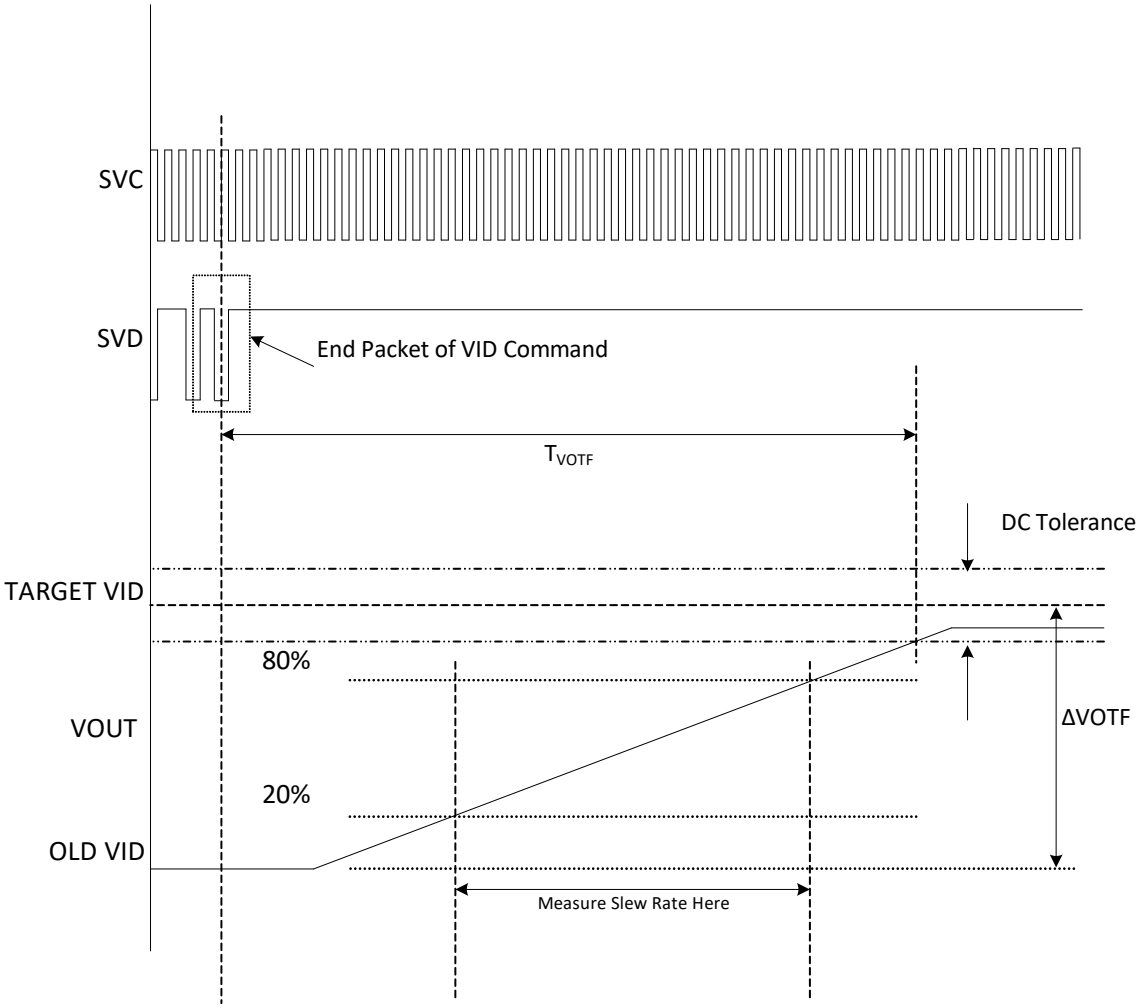

Figure 19. Voltage on the Fly Transition

Table 19. Voltage on the Fly Transition Timing Requirements

Parameter	Description	Min.	Typ.	Max.	Units	Note
Slew Rate	Measured slew rate during positive transition	Typ. – 10%	Programmed (UP_SLEW_RATE)	Typ. + 10%	mV/µs	1, 2, 3
T_{VOTF}	Total time of positive voltage transition			(ΔVOTF / Min. Slew Rate) + 10	µs	1, 3

Notes:

1. *The above slew rate and VOTF timing parameters are applicable when transitioning from the "OFF" VID.*
2. *For testing purposes, the slew rate shall be measured when ΔVOTF is greater than 100 mV.*
3. *Specified timing assumes that the output voltage is equal to the VID voltage at the moment that the voltage change is commanded.*

5.5.2.1 VID Decay Mode

There are no specified slew rate requirements for negative VID transitions (transitioning from a higher voltage to a lower voltage).

To save power in certain applications, targets are capable of supporting VID Decay Mode (output capacitors discharge through load only). The activation of VID Decay Mode is programmable through an SVI3-defined register DECAY_CONDITIONS (see Section 5.12.3).

When VID Decay Mode is not enabled, targets actively transition from a higher voltage to a lower voltage.

5.5.3 Programmable Maximum / Minimum VID

Programmable maximum and minimum values can be set through registers (VID_MAX, VID_MIN) defined in Section 5.12.3. If a VID packet is received by a target which is outside the maximum/minimum VID range, the target doesn't change the target voltage and returns a NACK: Invalid Command.

Conversely, if the controller attempts to set the maximum VID below the present target VID, the target doesn't change the VID_MAX register and returns a NACK: Invalid Command.

If the controller attempts to set the minimum VID above the present target VID, the target doesn't change the VID_MIN register and returns a NACK: Invalid Command.

5.5.4 Programmable Voltage Offset / Trim

A programmable voltage offset VOUT_OFFSET can be applied to the VID for margining purposes and to allow for regulation of voltages beyond the VID table (dependent on regulator capability).

The offset is programmed through the register described in Section 5.12.3. If the resultant VID request is beyond the capabilities of the regulator (VID + VOUT_OFFSET > MAX_VOUT_SUPPORTED or VID + VOUT_OFFSET < MIN_VOUT_SUPPORTED), the regulator returns a NACK: Invalid Command.

VOUT_OFFSET shifts OVP_THRESH and UVP_THRESH.

Table 20. Type 1 Extended Voltage Range

Parameter	Min	Max	Unit
Extended voltage range using offset	0.005	3.825	V

5.5.5 Output Voltage Accuracy

The specifications shown in Table 21 refer to the zero-load DC accuracy requirements of the voltage regulator's output. There are no specifications for accuracy outside the below VID and temperature range.

Table 21. Type 1 Output Voltage Accuracy

VID (V)	Controller T_j °C[1]	Min	Max	Unit
0.250 to 0.995	-40 to 0	-10	+10	mV
1.000 to 2.800	-40 to 0	-1	+1	%
0.250 to 0.995	0 to 85	-5	+5	mV
1.000 to 2.800	0 to 85	-0.5	+0.5	%
0.250 to 0.995	85 to 125	-7.5	+7.5	mV
1.000 to 2.800	85 to 125	-0.75	+0.75	%

Note:

1. *It is not required that SVI3 devices/targets support the entire temperature range from -40°C to 125°C.*

5.6 Load-Line

Table 22. Load-line Capability and Programmability

Parameter	Min	Typ.	Max	Unit
Load-Line Slope Capability	0		5	mΩ
Default Load-Line Slope Increment			0.05	mΩ
SVI3 Load-Line Gain Adjustment (of default)	0 (Off)		200	%
SVI3 Load-Line Gain Adj. Increment		10		%

5.7 Power States

The regulator is capable of transitioning from any PSI state to any PSI state.

Table 23. Type 1 Power States

PSI	Action
0	Full phase count (default)
1	Phase count 1st level (minimum phase count dictated by 4-bit register)
2	Phase count 2nd level (minimum phase count dictated by 4-bit register)
3	Single phase operation + active diode emulation (low-side actively driven when I_ind is positive)
4	Manufacturer-specific power-saving mode. *optional*
5	Reserved
6	Power down to 0V (voltage regulation disabled). PWRGD pin remains asserted. All non-essential systems are shutdown. No telemetry is measured by target. However, targets must still pass through telemetry packets and add its header packet for proper framing (if SVI3 interface is enabled)
7	Automated phase shedding and diode emulation

5.7.1 Fault Avoidance During Power States PSI1-PSI4

The voltage regulator takes actions to ensure that faults such as over-current protection are avoided while in PSI1-PSI4. These actions include:

1. Temporarily enabling full phase count during VID transitions.
2. Increasing phase count above register-indicated level when current level exceeds supported threshold.

5.7.2 PWR_ENABLE Effect on Power States

If PWR_ENABLE is de-asserted while in any PSI state, the voltage decreases in a manner dictated by the DECAY_CONDITIONS register (see Section 5.12.3).

The assertion of PWR_ENABLE always causes the voltage regulator to enter PSI0 state. For example, if the voltage regulator enters PSI6 state (disabling voltage regulation), and the PWR_ENABLE pin is de-asserted and then re-asserted, voltage regulation resumes in PSI0 mode.

5.8 Output Voltage Regulation Disabled States

There are three methods of disabling output voltage regulation: PWR_ENABLE pin low, PSI6 power state, VID command (VID = OFF). Table 24 summarizes the requirements of functionality, feature availability and exit latency during these states.

Table 24. Voltage Regulation Disabled States

Mode	SVI3 SVD Cmd.	Telemetry	PWRGD	Quiescent Power1,2	Exit time
PWR_ENABLE Low	Accessible	Disabled	Low	Mobile: < 1 mW / target Non-mobile: < 20 mW/target	VID/Slew_RATE + 100 µs
PSI6	Accessible	Disabled	High	Mobile: < 1 mW / target Non-mobile: < 20 mW/target	VID/Slew_RATE + 100 µs
VID = OFF	Accessible	Full-capability	High	Undefined	VID/Slew_RATE + 10 µs

Notes:

1. *During $T_{VCC\text{-}EN}$ (see Section 5.4.3), the controller quiescent power is not restricted.*
2. *Quiescent power requirements assume that the SVI3 interface has been disabled (see Section 4.9). Quiescent power requirements refer to that of the controller device only.*

PWR_ENABLE de-assertion or entering PSI6 shuts down output voltage regulation but does not affect the VID register. Upon PWR_ENABLE assertion or exiting PSI6, the voltage regulator returns to the value present in the VID register. During PWR_ENABLE de-assertion or PSI6 power states, all non-essential (power regulation) systems are shutdown, and telemetry is not measured by the target. During PSI6 or PWR_ENABLE de-assertion, no telemetry data packets are added by the target. However, if the SVI3 interface is still enabled, each target must pass through telemetry packets and add its header packet for proper framing. If a Register Read command is issued, the selected target still issues a Register Readback packet. Other SVI3 functionality (such as register writing) are accessible.

5.9 Faults / Warning / Lock-Outs

All SVI3 target/rails have individual fault, warning and protection mechanisms.

Faults: All faults result in the immediate de-assertion of PWRGD and a latched shut-down of the effected voltage regulator rail. The shut-down of the voltage regulator must not result in negative voltage undershoots. After a fault, voltage regulation can not resume until PWR_ENABLE has toggled low then high. The toggling of PWR_ENABLE has no effect on the sticky FAULT_STATUS bits defined in Section 5.12.2 and Section 6.11.2.

Note: *The above fault behavior may be modifiable by manufacturer-specific settings. However, the default behavior shall be immediate shutdown, latch off (as described above).*

Warning: Warnings are defined as a condition that alerts the controller in some fashion to make a corrective action to prevent a fault condition. During a warning condition, the PWRGD remains asserted and voltage regulation behavior is unaffected.

Lock-Outs: A lock-out is defined as a condition (or conditions) that must occur before the voltage regulator can enter a specified state.

5.9.1 Under Voltage Lockout (UVLO)

5.9.1.1 Voltage Regulator Device VCC / Driver Voltage / Input Voltage

The voltage regulator device ensures that its VCC voltage is within minimum specification before enabling voltage regulation. VCC should never fall below minimum specification in normal operation. If VCC falls below specification, the device disables voltage regulation until a full VCC power cycle occurs.

If the voltage regulator device uses integrated drivers, the device ensures that the drive voltage is within minimum specification before enabling voltage regulation.

If the voltage regulator device measures input voltage for telemetry purposes, the device ensures that the input voltage is within minimum specification before enabling voltage regulation.

If driver voltage or input voltage falls below specification, the controller disables voltage regulation. This is not considered a latched fault condition. If voltages return to specification, the controller enables voltage regulation.

5.9.1.2 SVI3 SVI3_VDDIO

The device allows voltage regulation while the SVI3 interface voltage (SVI3_VDDIO) is below minimum specification.

5.9.2 Over Current Protection (OCP) Fault

Voltage regulator devices must support OCP for all rails. The detection of an OCP fault results in the fault shut-down as described in Section 5.9.

The detection of an OCP fault latches the assertion of the OCP_L pin. Only when the OCP fault is cleared, through PWR_ENABLE de-assertion and re-assertion or VCC power cycling, will the OCP_L pin de-assert.

OCP is based on the summation of all inductor currents. The analog/digital signal representing the summed inductor current meets the parameters listed in Table 25. The current sense network must have a minimum bandwidth I_{IND}_BW and must be able to track current slew rates up to I_{IND}_SR. The maximum delay between the summed inductor current exceeding the OCP threshold and the regulator initiating power-down is listed in Table 25.

Table 25. Type 1 Current Sensing Requirements

Parameter	Min	Typ	Max	Unit
I_{IND}_BW (-3dB Bandwidth: output/inductor current)	250			kHz
I_{IND}_SR (slew rate referenced to inductor current)	-1000		1000	A/µs
OCP propagation delay (OCP_THRESH exceeded to shut down), OCP_FAULT_DELAY = 000b			1	µs
OCP_WARN propagation delay (OCP_WARN_THRESH exceeded to OCP_WARN assertion)			1	µs

5.9.2.1 OCP Threshold Programmability

The over current protection threshold (OCP_THRESH) is programmable through an SVI3-specified register (see Section 5.12.3). The voltage regulator device must have a platform-level programmable default threshold applied (either through NVM or resistor settings).

5.9.2.2 OCP Delay

A programmable delay may be applied to the over-current protection fault. If the delay is enabled, the inductor current must exceed OCP_ THRESH continuously for a programmable amount of

time OCP_FAULT_DELAY before an OCP fault occurs. The register description of OCP_FAULT_DELAY is described in Section 5.12.3.

5.9.3 OCP Warning aka PCC (Peak Current Control)

The OCP warning function uses a second programmable threshold OCP_WARN_THRESH to trigger the assertion of OCP_L and the OCP_WARN bit in the TEMP1/WARN telemetry packet (see Section 5.10.5). The OCP warning function is based on the same summed inductor current signal used for OCP fault detection. As shown in Figure 20, the OCP_L pin is also triggered by the input current (optional). The threshold for the input current triggered OCP_L is set by the I_IN_WARN_THRESH register (see Section 5.12.3).

The reaction time delay to assert the OCP_L pin after the inductor current exceeds the OCP_WARN_THRESH is equal to the OCP_WARN propagation delay (see Table 25).

OCP_L asserts for a minimum programmable time of OCP_WARN_MIN_PULSE. The register description of OCP_WARN_MIN_PULSE is described in Section 5.12.3.

5.9.3.1 OCP_L Pin Functionality

Each physical SVI3 device is required to have a minimum of one OCP_L pin. If a controller has one OCP_L pin and controls multiple targets/rails, the device internally “ORs” individual OCP_L assertions from individual rails.

5.9.3.2 OCP Warning Programmability

OCP_WARN_THRESH and OCP_FAULT_DELAY is programmable through SVI3-specified registers (see Section 5.12.3). The device can set the default values through NVM. If NVM is not available on the device, OCP Warning functionality is disabled by default.

5.9.4 Current Sensing and OCP Block Diagram

An example of a high-level block diagram detailing the current sensing and OCP functionality is shown in Figure 20. The figure also details the current sensing telemetry path.

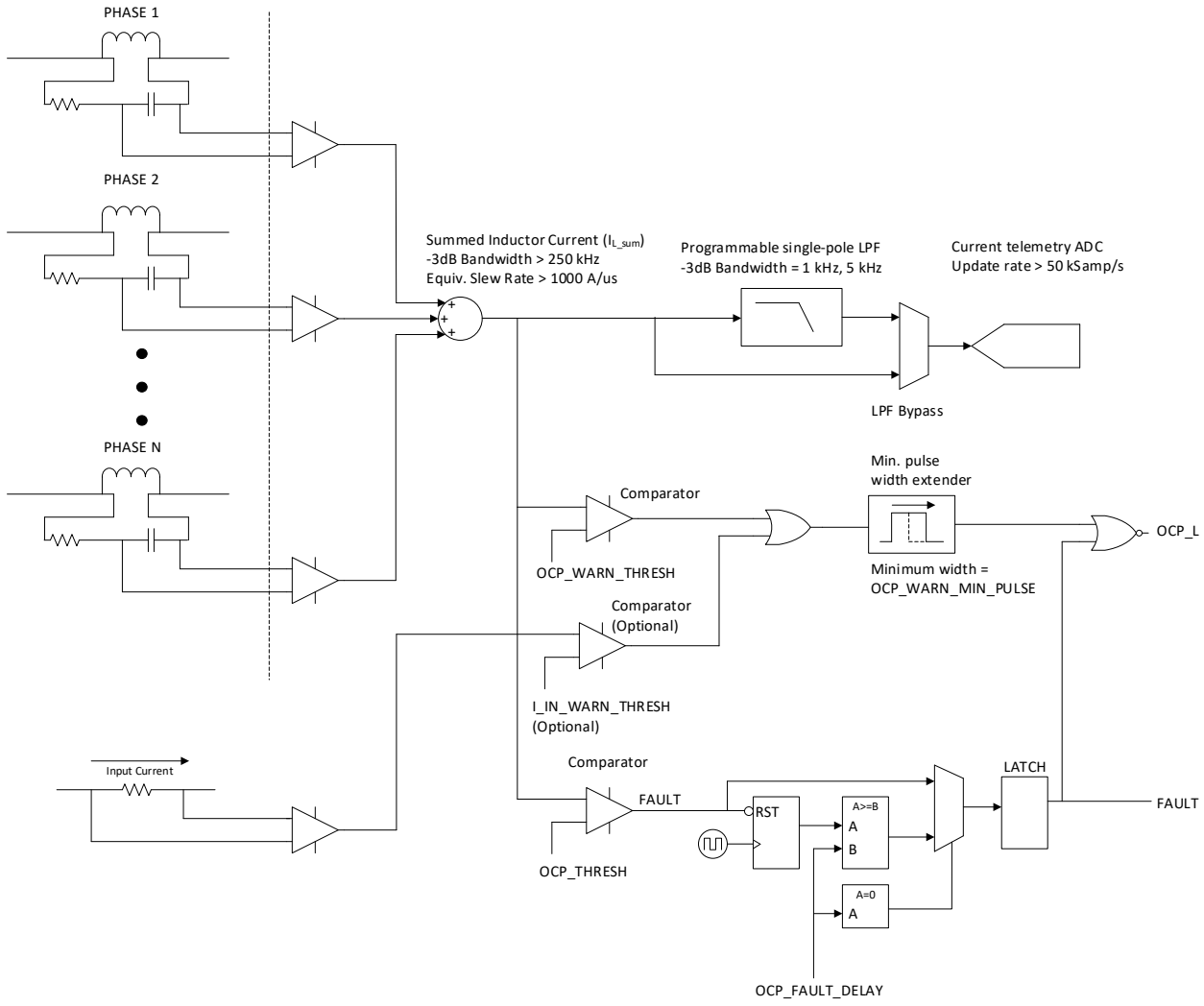

Figure 20. Current Sensing Topology Example

5.9.5 Over Voltage Protection (OVP) Fault

Voltage regulator devices must support OVP for all rails. If the output voltage exceeds the OVP threshold OVP_THRESH, the device initiates the fault shut-down described in Section 5.9. OVP_THRESH may be programmed to be a positive delta OVP_DELTA relative to the VID (not including load-line) or VID_MAX (as described in Section 5.12.3).

Note: *The voltage regulator must ensure that a Negative VID transition does not result in a OVP fault.*

```
OVP_THRESH   = VID + OVP_DELTA + VOUT_OFFSET
```

or

```
OVP_THRESH   = VID_MAX + OVP_DELTA + VOUT_OFFSET
```

5.9.5.1 Over Voltage Protection (OVP): Voltage-on-the-Fly (VOTF) and Pre-bias Voltage

The following conditions don't result in an OVP fault:

1. The instantaneous voltage being greater than `VID + OVP_DELTA + VOUT_OFFSET` because of a negative VOTF transition.
2. Starting voltage regulation where a pre-bias output voltage exists and OVP thresholds have not been exceeded.

5.9.5.2 Over Voltage Protection (OVP) Programmability

OVP_DELTA and its reference (VID or VID_MAX) are programmable through SVI3-specified registers (see Section 5.12.3). The device may set the default values through NVM. If NVM is not available on the device, the default values are described in Section 5.12.3.

5.9.6 Under Voltage Protection (UVP) Fault

Voltage regulator device must support UVP for all rails. If the output voltage decreases below the UVP threshold UVP_THRESH, the device initiates the fault shut-down described in section 5.9. UVP_THRESH may be programmed to be a negative delta UVP_DELTA relative to the VID (not including load-line) or VID_MIN (as described in Section 5.12.3).

```
UVP_THRESH   = VID - UVP_DELTA + VOUT_OFFSET
```

or

```
UVP_THRESH   = VID_MIN - UVP_DELTA + VOUT_OFFSET
```

5.9.6.1 UVP During VOTF

During positive VOTF transitions, it is expected that the output voltage can reasonably track the transitioning reference voltage. Therefore, during a positive VOTF transition, the reference voltage is used as the UVP reference, if the UVP reference is set to VID.

5.9.6.2 Under Voltage Protection (UVP) Programmability

UVP_DELTA and its reference (VID or VID_MIN) is programmable through SVI3-specified registers (see Section 5.12.3). The device may set the default values through NVM. If NVM is not available on the device, the default values are described in Section 5.12.3.

5.9.7 Temperature Protection

5.9.7.1 VR-Hot Warning

Each rail has independent VR-HOT warning functionality. The device measures the "hot-spot" of the rail and assert the VR_HOT bit in the temperature telemetry packet (see Section 5.10.5) when the temperature exceeds a programmable threshold VRHOT_THRESH. Temperature measurement accuracy and range is described in Table 34.

5.9.7.2 Over Temperature Protection (OTP) Fault

Each rail has independent over-temperature protection control. If the measured temperature exceeds the OTP threshold OTP_THRESH, the device initiates the fault shut-down described in Section 5.9.

5.10 Telemetry

Voltage regulator devices must be capable of providing telemetry information for each rail.

5.10.1 Output Current (Telemetry Reg. Index 000b)

Output current telemetry consists of a 10-bit encoding that is mapped to eight user-selectable scales.

The device must have the capability for the designer to select the appropriate current scale at the platform level (either by NVM or resistor selection). During start-up, the device sets the output current scale register (see Section 5.12.1). The controller reads back this register to determine the appropriate decoding scale.

The output current ADC must maintain 10-bit resolution across all current scales and have no missing codes.

Table 26. Type 1 Output Current Scaling Selections

		Current (A)							
		CUSTOM	**32A**	**64A**	**128A**	**256A**	**512A**	**1024A**	**2048A**
Decimal	**Binary**	**(000b)**	**(001b)**	**(010b)**	**(011b)**	**(100b)**	**(101b)**	**(110b)**	**(111b)**
0	0000000000	0	0	0	0	0	0	0	0
1	0000000001	CUSTOM	0.03125	0.0625	0.125	0.25	0.5	1	2
2	0000000010	CUSTOM	0.0625	0.125	0.25	0.5	1	2	4
3	0000000011	CUSTOM	0.09375	0.1875	0.375	0.75	1.5	3	6
4	0000000100	CUSTOM	0.125	0.25	0.5	1	2	4	8
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1020	1111111100	CUSTOM	31.875	63.75	127.5	255	510	1020	2040
1021	1111111101	CUSTOM	31.90625	63.8125	127.625	255.25	510.5	1021	2042
1022	1111111110	CUSTOM	31.9375	63.875	127.75	255.5	511	1022	2044
1023	1111111111	CUSTOM	31.96875	63.9375	127.875	255.75	511.5	1023	2046

5.10.1.1 DCR Current Sensing Accuracy

If the voltage regulator device uses DCR current sensing for the purposes of telemetry reporting and load-line adjustment, the following accuracy requirements are met or exceeded for all operating corners (device junction temperature, VCC voltage tolerance, nominal output voltage, etc.) The accuracy limits must be met for single-phase and multi-phase operation (i.e., tolerance cannot be exceeded when operating in singe-phase power saving mode).

Table 27. DCR Current Sensing Accuracy Requirements

	Min	Max	Unit
Maximum gain error introduced by device	-2	+2	%
Total offset of DCR voltage sensing (referred to input)	-0.5	+0.5	mV

For the purposes of defining device current accuracy, the following assumptions can be made:

- No error is introduced by DCR current sensing element
- No error is introduced by NTC tolerance or placement (i.e., temperature compensation is perfect)
- Any resistors required by the device have ±1% tolerance. The resistance tolerance counts toward “gain error introduced by the device”

5.10.1.2 Integrated Power-Stage Current Sensing Accuracy

If the voltage regulator device uses integrated power-stage current sensing for the purposes of telemetry reporting and load-line adjustment, the following accuracy requirements is met or exceeded for all operating corners (device/power-stage junction temperature, VCC voltage tolerance, nominal output voltage, etc.) The accuracy limits must be met for single-phase and multi-phase operation (i.e., tolerance cannot be exceeded when operating in singe-phase power saving mode).

Table 28. Integrated Power-Stage Current Sensing Accuracy

	Min	Max	Unit
Total current sensing gain error (end-to-end)	-5	+5	%
Total current offset (end-to end)	–1	+1	A

For the purposes of defining system current accuracy, the following assumptions can be made:

- Power-stage temperature may vary within its rated operating range
- Any resistors required by the device/power-stage have ±1% tolerance. The resistance tolerance counts toward “total current sensing gain error”

5.10.1.3 Output Current Telemetry Bandwidth and Sampling Rate

The target samples the output current in a free-running fashion at the rate defined in Table 29. Following the receipt of a Telemetry Request Packet, the target copies the most recently acquired sample to a shadow register for telemetry reporting.

Telemetry requests may occur faster than the sampling rate. In this case, the target returns successive telemetry reports with unchanging data.

Output current telemetry is derived from a bandwidth-limited version of the signal used for OCP/OCP_WARN as described in Figure 20.

The telemetry is bandwidth-limited through use of a single-pole low-pass filter with a programmable -3dB corner bandwidth. The bandwidth of output current telemetry is programmable either digitally (through a manufacturer-specified register) or by the selection of an external component (e.g., capacitor to ground). The selectable bandwidth range and minimum bandwidth resolution specification are described in Table 29.

Table 29. Current Telemetry Bandwidth/Sampling Requirements

	Min	Max	Unit
Current Telemetry ADC sampling rate	50		kSamp/s
Programmable BW range	1	LPF Bypass	kHz
Minimum amount of selectable values	1, 5, LPF Bypass		kHz

5.10.2 Output Voltage (Telemetry Reg. Index 001b)

Explicit measurement of the output voltage for telemetry purposes is required for all rails.

Output voltage telemetry data payloads consist of 10 bits. The encoding formula for output voltage telemetry is shown below:

```
VOUT_TELEMETRY[9:0] = Output Voltage (V) / 5mV
```

Output voltage continues to be measured and reported when the VID is set to “OFF”. This is intended to measure pre-bias voltage or decaying voltage.

5.10.2.1 Output Voltage Telemetry Accuracy

Output voltage telemetry accuracy requirements are described in Table 30.

Table 30. Type 1 Output Voltage Telemetry Accuracy Requirements

VID (V)	Controller Tj °C	Min	Max	Unit
0.250 to 0.995	–40 to 0	–15	+15	mV
1.000 to 2.800	–40 to 0	–1.5	+1.5	%
0.250 to 0.995	0 to 85	–7.5	+7.5	mV
1.000 to 2.800	0 to 85	–0.75	+0.75	%
0.250 to 0.995	85 to 125	–10	+10	mV
1.000 to 2.800	85 to 125	–1	+1	%

Note:
1. It is not required that SVI3 devices support the entire temperature range from -40°C to 125°C.

5.10.2.2 Output Voltage Telemetry Bandwidth

The target samples the output voltage in a free-running fashion at the rate defined in Table 31. Following the receipt of a Telemetry Request packet, the target copies the most recently acquired sample to a shadow register for telemetry reporting.

Like output current telemetry, the bandwidth of output voltage telemetry is programmable either digitally (through a manufacturer-specified register) or by the selection of an external component (e.g., capacitor to ground). The selectable bandwidth range and minimum bandwidth resolution specification are described in Table 31. Output voltage telemetry bandwidth and output current telemetry bandwidth do not require independent programmability (i.e., it can be assumed that the two bandwidths are always equal).

Table 31. Output Voltage Telemetry Bandwidth/Sampling Requirements

	Min	Max	Unit
Voltage Telemetry ADC sampling rate	50		kSamp/s
Programmable BW range	1	LPF Bypass	kHz
Minimum amount of selectable values	1, 5, LPF Bypass		kHz

5.10.3 Input Current (Telemetry Reg Index 100b) *Optional*

Table 32. Input Current Scaling Selections

Current (A)									
		CUSTOM	4A	8A	16A	32A	65A	128A	256A
Decimal	Binary	(000b)	(001b)	(010b)	(011b)	(100b)	(101b)	(110b)	(111b)
0	0000000000	0	0	0	0	0	0	0	0
1	0000000001	CUSTOM	0.00390625	0.0078125	0.015625	0.03125	0.0625	0.125	0.25
2	0000000010	CUSTOM	0.0078125	0.015625	0.03125	0.0625	0.125	0.25	0.5
3	0000000011	CUSTOM	0.01171875	0.0234375	0.046875	0.09375	0.1875	0.375	0.75
4	0000000100	CUSTOM	0.015625	0.03125	0.0625	0.125	0.2	0.5	1
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1020	1111111100	CUSTOM	3.984375	7.96875	15.9375	31.875	63.75	127.5	255
1021	1111111101	CUSTOM	3.98828125	7.9765625	15.953125	31.90625	63.8125	127.625	255.25
1022	1111111110	CUSTOM	3.9921875	7.984375	15.96875	31.9375	63.875	127.75	255.5
1023	1111111111	CUSTOM	3.99609375	7.9921875	15.984375	31.96875	63.9375	127.875	255.75

5.10.4 Input Voltage (Telemetry Reg. Index 101b) *Optional*

Table 33. Input Voltage Scaling Selection

		Voltage (V)			
		CUSTOM	CUSTOM	32V	64V
Decimal	Binary	(00b)	(01b)	(10b)	(11b)
0	0000000000	CUSTOM	CUSTOM	0	32
1	0000000001	CUSTOM	CUSTOM	0.03125	32.03125
2	0000000010	CUSTOM	CUSTOM	0.0625	32.0625
3	0000000011	CUSTOM	CUSTOM	0.09375	32.09375
4	0000000100	CUSTOM	CUSTOM	0.125	32.125
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1020	1111111100	CUSTOM	CUSTOM	31.875	63.875
1021	1111111101	CUSTOM	CUSTOM	31.90625	63.90625
1022	1111111110	CUSTOM	CUSTOM	31.9375	63.9375
1023	1111111111	CUSTOM	CUSTOM	31.96875	63.96875

5.10.5 Temperature 1 / Warn Status (Telemetry Reg. Index 010b)

Each rail is capable of reporting temperature telemetry that is representative of the "hot-spot" of the rail. VRHOT/OTP fault and temperature telemetry shares the same input signal.

The formula for reporting temperature in a 10-bit encoding is:

```
Temp 1 / Warn [9] = VRHOT (active low; 1b = not asserted, 0b =
asserted)

Temp 1 / Warn [8] = OCP_WARN (active low; 1b = not asserted, 0b
= sticky asserted until after subsequent telemetry request)
```

Note: *If OCP_WARN is asserted at any time prior to the most recent Telemetry Request and after the previous Telemetry Request, the OCP_WARN bit is asserted.*

```
Temp 1 / Warn [7:0] = Roundup (Temperature °C + 40)
```

5.10.5.1 Temperature 1 / Warn Status Accuracy

The temperature reporting requirements are detailed in Table 34.

Table 34. Temperature Telemetry Requirements

	Min	Typ	Max	Unit	Note
Temperature reporting range	–40		150	°C	1, 3, 4
Temperature reporting resolution		1		°C	
Temperature reporting accuracy (between 50°C and 125°C)	–5		+5	°C	2

Notes:

1. *Temperature reporting range refers to protocol-supported range. Actual temperature reporting range may be limited to operating range of voltage regulator.*
2. *If a thermistor is required, a 1% nominal resistance (25°C) tolerance and a 1% (25/50°C) β tolerance is assumed.*
3. *For temperatures below -40°C, the regulator reports –40°C.*
4. *It is not required that SVI3 devices support the entire temperature range from -40°C to 125°C.*

5.10.5.2 Temperature 1 / Warn Status Sampling Speed

Due to the relatively slow nature of temperature transients, bandwidth limiting of the temperature measurement is not required. The sampling speed requirement is described in Table 35.

Table 35. Temperature Telemetry Sampling Requirements

	Min	Max	Unit
Temperature ADC sampling rate	1		kSamp/s

5.10.6 Temperature 2 (Telemetry Reg. Index 011b) *Optional*

Each rail may be capable of reporting a second temperature zone of the rail. Accuracy and sampling speed requirements are identical to that of Temperature 1 (see Section 5.10.5).

The formula for reporting temperature in a 10-bit encoding is:

```
Temp 2 / Warn [9:8] = 00b

Temp 2 / Warn [7:0] = Roundup (Temperature °C + 40)
```

5.10.7 System Power (Telemetry Reg. Index 110b) *Optional for Non-Mobile*

System power is measured from the P_SYS pin (see Table 10) that receives an analog signal from a battery charger or system power monitor. System power telemetry consists of a 10-bit encoding that is mapped to eight user-selectable scales.

The device must have the capability for the designer to select the appropriate power scale at the platform level (either by NVM or resistor selection). During start-up, the device sets the system power scale register (see Section 5.12.1). The controller reads back this register to determine the appropriate decoding scale.

The system power ADC must maintain 10-bit resolution across all power scales and have no missing codes.

Table 36. System Power Scaling Selection

		System Power (W)			
		CUSTOM	**32W**	**64W**	**128W**
Decimal	**Binary**	**(000b)**	**(001b)**	**(010b)**	**(011b)**
0	0000000000	0	0	0	0
1	0000000001	CUSTOM	0.03125	0.0625	0.125
2	0000000010	CUSTOM	0.0625	0.125	0.25
3	0000000011	CUSTOM	0.09375	0.1875	0.375
4	0000000100	CUSTOM	0.125	0.25	0.5
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1020	1111111100	CUSTOM	31.875	63.75	127.5
1021	1111111101	CUSTOM	31.90625	63.8125	127.625
1022	1111111110	CUSTOM	31.9375	63.875	127.75
1023	1111111111	CUSTOM	31.96875	63.9375	127.875

		256W	**512W**	**1024W**	**2048**
Decimal	**Binary**	**(100b)**	**(101b)**	**(110b)**	**(111b)**
0	0000000000	0	0	0	0
1	0000000001	0.25	0.5	1	2
2	0000000010	0.5	1	2	4
3	0000000011	0.75	1.5	3	6
4	0000000100	1	2	4	8
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
1020	1111111100	255	510	1020	2040
1021	1111111101	255.25	510.5	1021	2042
1022	1111111110	255.5	511	1022	2044
1023	1111111111	255.75	511.5	1023	2046

5.11 Debug Functions

To facilitate system debug, all SVI3 targets have the following debug features. Debug features are enabled through SVI3-defined registers (see Section 5.12.3).

5.11.1 Extend Timeout

For slow speed debug, $t_{SVC\_timeout}$ (see Table 6) can be extended by a factor of 1024. This effectively decreases the minimum clock frequency.

5.11.2 Output Flag Manual Over-Ride

When enabled, OCP_L, VR_HOT and PWRGD may be manually controlled.

5.11.3 Telemetry Test Pattern

Output current, output voltage and temperature 1 telemetry may be over-written with user-programmable data payloads. When this debug function is enabled, the effected target outputs the 10-bit user-programmable payload through the standard telemetry packets.

The corresponding telemetry packet must still be enabled by setting TEN_BIT_TEL_EN (see Section 5.12). A Telemetry Request command is still required to initiate the telemetry stream.

5.12 Registers

SVI3-defined registers are defined in the following sub-sections. Manufacturer specific registers are not defined in the SVI3 specification and should be described in respective datasheets.

All undefined register bits are considered "Don't care".

5.12.1 Read-Only Register

Read-only registers are set by the manufacturer, by platform-level programming methods (NVM, resistor strap, etc.) or by a specialized SVI3 command. Read-only registers cannot be modified directly using the Register Write command. If a Register Write command attempts to modify a read-only register, the target returns a NACK: Invalid Command.

The SVI3-specific read-only registers are described in Table 37.

Table 37. Read-Only Registers

Addr (Hex)	Bits	Register Name	Description
01	[7:0]	SVI3_VERSION	Indicates the version of SVI3 for which the target is compliant. Equal to x in Rev. x.yy of the specification.
02	[7:5]	TYPE_ID	Indicates the type of the target 000b = Type 1: Multi-Phase Step-Down 001b = Type 2: Point of Load
02	[4:0]	MFG_ID	Indicates the manufacturer of the target/controller To be defined 00h = AMD (Eval Platform) 01h = Infineon 02h = Monolithic Power Systems 03h = Renesas 04h = Richtek 05h = MaxLinear 06h = OnSemi 07h = STMicro 08h = µPI 09h = ADI/Maxim Integrated 0Ah = Texas Instruments 0Bh = Anpec 0Ch = Ferric 0Dh = Vicor 0Eh = Alpha and Omega 0Fh = Aura Semiconductor
03	[7:0]	MODEL_ID	Unique model code defined by manufacturer
04	[7:0]	TEN_BIT_TEL_AVAIL	Indicates which types of 10-bit telemetry are available (1b = available, 0b = unavailable) Bit 7 = Reserved Bit 6 = System Power Bit 5 = Input Voltage Bit 4 = Input Current Bit 3 = Temp 2 Bit 2 = Temp 1 Bit 1 = Output voltage Bit 0 = Output current

Table 37. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
05	[7:0]	SIXTEEN_BIT_TEL_AVAIL	Indicates which types of 16-bit telemetry are available (1b = enabled, 0b = disabled) Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Reserved Bit 3 = Reserved Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved
06	[7:7]	CRC_ENABLED	Indicates if CRC is enabled 1b = enabled (default) 0b = disabled *Note: CRC can only be enabled/disabled through global command*
06	[4:2]	PSI	Indicates the PSI state of the target
06	[0:0]	VID[8]	Indicates the MSB of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
07	[7:0]	VID[7:0]	Indicates the 8 LSBs of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
08	[5:4]	DEFAULT_SLEW_RATE	Default slew rate programmed at platform level (NVM, resistor strap, etc.) 00b = 2.5 mV/us 01b = 10 mV/us 10b = 20 mV/us 11b = 40 mV/us
08	[3:0]	VID_DEFAULT_VOLTAGE	Default VID, programmed at platform level (NVM, resistor strap, etc.) 0h = Off (wait for SVI3 VID command) 1h = 0.500 V 2h = 0.600 V 3h = 0.700 V 4h = 0.800 V 5h = 0.900 V 6h = 1.000 V 7h = 1.100 V 8h = 1.200 V 9h = 1.300 V Ah = 1.400 V

Table 37. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
			Bh = 1.500 V Ch = 1.800 V Dh = 2.000 V Eh = 2.500 V Fh = 2.800 V
09	[7:6]	V_IN_SCALE	Input voltage scale, programmed at platform level (NVM, resistor strap, etc.) 00b = Custom Scale / Reserved 01b = Custom Scale / Reserved 10b = 32V Scale 11b = 64A Scale
09	[5:3]	I_OUT_SCALE	Output current scale, programmed at platform level (NVM, resistor strap, etc.) 000b = Custom Scale / Reserved 001b = 32A Scale 010b = 64A Scale 011b = 128A Scale 100b = 256A Scale 101b = 512A Scale 110b = 1024A Scale 111b = 2048A Scale
09	[2:0]	I_IN_SCALE	Input current scale, programmed at platform level (NVM, resistor strap, etc.) 000b = Custom Scale / Reserved 001b = 4A Scale 010b = 8A Scale 011b = 16A Scale 100b = 32A Scale 101b = 64A Scale 110b = 128A Scale 111b = 256A Scale
0A	[7:0]	MAX_VOUT_SUPPORTED	Maximum output voltage supported by voltage regulator Max Vout = Reg[7:0] * 20 mV
0B	[7:0]	MIN_VOUT_SUPPORTED	Minimum non-zero output voltage supported by voltage regulator Min Vout = Reg[7:0] * 5 mV

Table 37. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
0C	[2:0]	P_SYS_SCALE	System power scale, programmed at platform level (NVM, resistor strap, etc.) 000b = Custom Scale / Reserved 001b = 32W Scale 010b = 64W Scale 011b = 128W Scale 100b = 256W Scale 101b = 512W Scale 110b = 1024W Scale 111b = 2048W Scale

Note: *For PSI6, AC and DC voltage limits do not apply, but the end voltage must reach OV if allowed to do so.*

5.12.2 Status Registers

Status registers record occurrences of warnings, NACKs or faults. All status bits are active high. All status bits are "sticky" and are cleared by writing 0b to the appropriate bits, provided the fault condition no longer exists. Writing 1b doesn't affect the status of the associated bit. For example, writing FEh to the FAULT_STATUS register only clears the over current protection flag.

The SVI3-specific status registers are described in Table 38.

Table 38. Status Registers

Addr (Hex)	Bits	Register Name	Description
10	[7:0]	FAULT_STATUS	Sticky flag asserted high when a fault/warning occurs Bit 7 = Reserved (0b) Bit 6 = Reserved (0b) Bit 5 = VRHOT asserted Bit 4 = OCP_WARN asserted Bit 3 = OTP fault Bit 2 = UVP fault Bit 1 = OVP fault Bit 0 = OCP fault
11	[7:0]	NACK_STATUS	Sticky flag asserted when a NACK occurs Bit 7 = Reserved (0b) Bit 6 = Reserved (0b) Bit 5 = NACK: Communication Error: Command before ACK Bit 4 = NACK: Communication Error: Framing Error Bit 3 = NACK: Communication Error: CRC Error Bit 2 = NACK: Invalid Command: Undefined Register Command Bit 1 = NACK: Invalid Command: Undefined Payload Bit 0 = NACK: Invalid Command: Not Executable / Not Supported

5.12.3 Read/Write Registers

Read/Write registers can be modified by the controller using the Register Write command. The SVI3-specific Read/Write registers are described in Table 39. For Read/Write registers, it is expected that register defaults are extracted from NVM (if available). If NVN is not available, the default is defined in Table 39.

Table 39. Read/Write Registers

Addr (Hex)	Bits	Register Name	Description	Default (if NVM not available)
20	[7:5]	DECAY_CONDITIONS	Down voltage decay enabled for following conditions 1b = enabled 0b = disabled Bit 7 Decay in PSI0, PSI1, PSI2 (or equivalent states when in PSI7). Bit 6 Decay in PSI3 (or equivalent states when in PSI7) Bit 5 Decay in PSI6 or when PWR_ENABLE is de-asserted	000b
20	[4:4]	DOWN_SLEW_RATE	Slew rate when decay conditions not met (i.e., active slew rate control) 1b: Negative slew rate = 1/4 positive slew rate 0b: Negative slew rate = positive slew rate	0b
20	[3:0]	UP_SLEW_RATE	Slew rate for positive VID change Slew rate = Reg[3:0] * 2.5 + 2.5 mV/us	Copied from DEFAULT_SLEW_RATE
21	[4:0]	LL_ADJUST	Load-line adjustment relative to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = Invalid (out of range)	01010b (100%)
22	[7:0]	VOUT_OFFSET	Voltage offset applied to VID, VID_MIN, VID_MAX, OVP_THRESH and UVP_THRESH 00h = Disabled (no offset) Offset = Reg[7:0] * 5 - 250 mV	00h

Table 39. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM not available)
23	[7:0]	VID_MAX	Maximum settable VID command 00h = Disabled Maximum VID = Reg[7:0] * 10 mV + 250mV	00h
24	[7:0]	VID_MIN	Minimum settable VID command 00h = Disabled Minimum VID = Reg[7:0] * 10 mV + 250 mV	00h
25	[7:0]	TEN_BIT_TEL_EN	Controls which types of 10-bit telemetry are enabled (1b = Enabled, 0b = Disabled) Bit 7 = Reserved Bit 6 = System Power Bit 5 = Input Voltage Bit 4 = Input Current Bit 3 = Temp 2 Bit 2 = Temp 1 Bit 1 = Output voltage Bit 0 = Output current	00h
26	[7:0]	SIXTEEN_BIT_TEL_EN	Controls which types of 16-bit telemetry are enabled (1b = Enabled, 0b = Disabled) Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Reserved Bit 3 = Reserved Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	00h
27	[7:0]	OCP_THRESH	Over current protection threshold level 00h = Disabled (no OCP protection) OCP Threshold = Reg[7:0] * 4 * I_OUT_SCALE / 512 A	Platform
28	[7:0]	OCP_WARN_THRESH	Over current warning threshold level 00h = Disabled OCP Warning Threshold = Reg[7:0] * 4 * I_OUT_SCALE / 512 A	NVM (or 00h if NVM is unavailable)

Table 39. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM not available)
29	[7:3]	OCP_WARN_MIN_PULSE	Minimum asserted pulse width of OCP_WARN signal Minimum pulse = Reg[7:3] * 500 ns	NVM (or 00000b if NVM is unavailable)
29	[2:0]	OCP_FAULT_DELAY	Continuous time that current must exceed OCP_THRESH before triggering fault 000b = Instantaneous fault Fault delay = Reg[2:0] * 5 us	NVM (or 000b if NVM is unavailable)
2A	[7:0]	VRHOT_THRESH	Voltage regulator hot warning threshold 00h = Disabled VRHOT Threshold = Reg[7:0] - 40°C	8Ch (100°C)
2B	[7:0]	OTP_THRESH	Over temperature protection threshold 00h = Disabled OTP Threshold = Reg[7:0] - 40°C	A5h (125°C)
2C	[7:7]	OVP_REF	Reference to set over-voltage protection threshold 0b = VID, 1b = VID_MAX	0b
2C	[6:4]	OVP_DELTA	Delta value to set over-voltage protection threshold 000b = Disabled OVP Delta = Reg[6:4] * 50 + 50 mV	110b (350 mV)
2C	[3:3]	UVP_REF	Reference to set under-voltage protection threshold 0b = VID, 1b = VID_MIN	0b
2C	[2:0]	UVP_DELTA	Delta value to set under-voltage protection threshold 000b = Disabled UVP Delta = Reg[6:4] * 50 + 50 mV	110b (350 mV)
2D	[7:4]	PHASE_SHED_1	Active number of phases when target is in PSI1	0001b
2D	[3:0]	PHASE_SHED_2	Active number of phases when target is in PSI2	0001b
2E	[7:0]	I_IN_WARN_THRESH	Input current warning threshold level 00h = Disabled Threshold = Reg[7:0] * 4 * I_IN_SCALE / 512 A	NVM (or 00h if NVM is unavailable)

Table 39. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM not available)
40	[7:0]	DEBUG_ENABLED	Bit 6 = Extend timeout clock by factor of 1024 Bit 5 = Overwrite Temp 1 telemetry enabled Bit 4 = Overwrite output voltage telemetry enabled Bit 3 = Overwrite output current telemetry enabled Bit 2 = Manually control PWRGD enabled Bit 1 = Manually control VRHOT enabled Bit 0 = Manually control OCP_WARN enabled	00h
41	[7:0]	DEBUG_TEMP1_OVERRIDE	Data payload for TEMP1 when bit 5 of register 40 is asserted	00h
42	[7:0]	DEBUG_VOUT_OVERRIDE	Data payload for VOUT_TELEMETRY[9:2] when bit 4 of register 40 is asserted	00h
43	[1:0]	DEBUG_VOUT_OVERRIDE	Data payload for VOUT_TELEMETRY[1:0] when bit 4 of register 40 is asserted	00b
44	[7:0]	DEBUG_IOUT_OVERRIDE	Data payload for IOUT_TELEMETRY[9:2] when bit 3 of register 40 is asserted	00h
45	[1:0]	DEBUG_IOUT_OVERRIDE	Data payload for IOUT_TELEMETRY[1:0] when bit 3 of register 40 is asserted	00b
46	[2:0]	DEBUG_OUTPUT_OVERRIDE	Bit 2 = PWRGD when bit 2 of register 40 is asserted Bit 1 = VRHOT when bit 1 of register 40 is asserted Bit 0 = OCP_WARN when bit 0 of register 40 is asserted	000b

Table 39. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM not available)
50	[7:0]	GEN_PURPOSE_0	General purpose register 0	00h
51	[7:0]	GEN_PURPOSE_1	General purpose register 1	00h
52	[7:0]	GEN_PURPOSE_2	General purpose register 2	00h
53	[7:0]	GEN_PURPOSE_3	General purpose register 3	00h
54	[7:0]	GEN_PURPOSE_4	General purpose register 4	00h
55	[7:0]	GEN_PURPOSE_5	General purpose register 5	00h
56	[7:0]	GEN_PURPOSE_6	General purpose register 6	00h
57	[7:0]	GEN_PURPOSE_7	General purpose register 7	00h

Chapter 6 Design Criteria for Type 2 Devices: Point of Load Step-Down Switching Voltage Regulators

6.1 Definition of Type 2 Device

To be classified as a Type 2 device, all of the following criteria must be true:

- The regulator must be a switching step-down DC-DC converter topology
- The device regulates one rail
- The regulator rail contains a single phase

6.2 Required Signals and Descriptions

The required signals for Type 2 targets are found in Table 40. These signals are in addition to signals defined in Section 3.1.

Table 40. Type 2 Target Required Signals

Signal	I/O	Description
VCC	Input (Power)	Device logic voltage
PWR_ENABLE	Input	Active high signal to enable voltage regulation
PWRGD	Output	Active high, open-drain signal to indicate to system that rail is enabled, within regulation and has no faults
VDD_SENSE	Input	Analog input; Positive remote voltage sense of rail
VSS_SENSE	Input	Analog input; Negative remote voltage sense of rail

6.3 Electrical Requirements

Table 41. Type 2 Target Electrical Requirements

Parameter	Description	Min.	Typ.	Max.	Units	Note
PWR_ENABLE V_{IL}	Enable input low voltage			0.63	V	1
PWR_ENABLE V_{IH}	Enable input high voltage	1.17			V	1

Table 41. Type 2 Target Electrical Requirements(Continued)

Parameter	Description	Min.	Typ.	Max.	Units	Note
$PWRGD_{VOL}$	PWRGD output low voltage, I_{OL} = 8 mA			0.2	V	
$I_{leak-Pin}$	Leakage PWR_ENABLE/PWRGD	-10		10	µA	
Notes: *1. The PWR_ENABLE pin must be operable at 3.3V + 10%.*						

6.4 Power-Up Sequencing

The power up sequence of a regulated rail is as follows:

1. VCC voltage is powered on and in regulation
2. The device sets the default voltage and the default slew rate based on NVM or platform-level component selection. (i.e., Referring to Section 6.11.1 the read-only registers DEFAULT_SLEW_RATE and VID_DEFAULT_VOLTAGE is populated).
3. The device copies the default voltage and the default slew rate to the target VID and slew rate registers respectively. (i.e., Referring to Section 6.11.3 VID is set by VID_DEFAULT_VOLTAGE and UP_SLEW_RATE is set by DEFAULT_SLEW_RATE.)
   a. If SVI3 interface is initialized, the target VID and slew rate may be over-written before the PWR_ENABLE pin is asserted
4. The PWR_ENABLE pin is asserted
5. The output voltage begins ramping up to the target VID at the slew rate
6. PWRGD is asserted after the output voltage is within tolerance and start-up ramping is complete

   Note: *It is not required that SVI3_VDDIO be within regulation or the SVI3 bus be initialized to initiate the power-up sequence.*

6.4.1 Default Voltage

The Default Voltage is used as the target's initial VID value. At first VCC power-on, targets copy the Default Voltage's effective 9-bit VID value to the target's VID register. When SVI3_RESET_L is asserted, targets copy the Default Voltage's effective 9-bit value to the target's VID register.

The Default Voltage is programmed at the platform level (through NVM, board-level resistor strapping). The required programmable Default Voltage set is shown in Table 42.

Table 42. Type 2 Default Voltages

Value	Default Voltage (V)
0h	Off (Wait for SVI3 cmd.)
1h	0.500
2h	0.600
3h	0.700
4h	0.800
5h	0.900
6h	1.000
7h	1.100
8h	1.200
9h	1.300
Ah	1.400
Bh	1.500
Ch	1.800
Dh	2.500
Eh	3.300
Fh	5.000

6.4.2 Default Slew Rate

Refer to Section 5.4.2 for additional information about the default slew rate.

6.4.3 Power-Up Timing Requirements

Refer to Section 5.4.3 for additional information about the power-up timing requirements.

6.5 Output Voltage

It is required that all voltage regulators be capable of supporting the entire range of the VID table (See Table 43 through Table 46) within the accuracy specifications described in Section 6.5.5.

Voltage regulators may support lower/higher voltages than those described in the table. Setting target voltages beyond the VID table is supported using a programmable offset described in Section 6.5.4.

6.5.1 VID Table

Table 43. Type 2 Target VID Table (Part 1)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
000000000	000	OFF	000100000	020	0.810	001000000	040	1.130	001100000	060	1.450
000000001	001	0.500	000100001	021	0.820	001000001	041	1.140	001100001	061	1.460
000000010	002	0.510	000100010	022	0.830	001000010	042	1.150	001100010	062	1.470
000000011	003	0.520	000100011	023	0.840	001000011	043	1.160	001100011	063	1.480
000000100	004	0.530	000100100	024	0.850	001000100	044	1.170	001100100	064	1.490
000000101	005	0.540	000100101	025	0.860	001000101	045	1.180	001100101	065	1.500
000000110	006	0.550	000100110	026	0.870	001000110	046	1.190	001100110	066	1.510
000000111	007	0.560	000100111	027	0.880	001000111	047	1.200	001100111	067	1.520
000001000	008	0.570	000101000	028	0.890	001001000	048	1.210	001101000	068	1.530
000001001	009	0.580	000101001	029	0.900	001001001	049	1.220	001101001	069	1.540
000001010	00A	0.590	000101010	02A	0.910	001001010	04A	1.230	001101010	06A	1.550
000001011	00B	0.600	000101011	02B	0.920	001001011	04B	1.240	001101011	06B	1.560
000001100	00C	0.610	000101100	02C	0.930	001001100	04C	1.250	001101100	06C	1.570
000001101	00D	0.620	000101101	02D	0.940	001001101	04D	1.260	001101101	06D	1.580
000001110	00E	0.630	000101110	02E	0.950	001001110	04E	1.270	001101110	06E	1.590
000001111	00F	0.640	000101111	02F	0.960	001001111	04F	1.280	001101111	06F	1.600
000010000	010	0.650	000110000	030	0.970	001010000	050	1.290	001110000	070	1.610
000010001	011	0.660	000110001	031	0.980	001010001	051	1.300	001110001	071	1.620
000010010	012	0.670	000110010	032	0.990	001010010	052	1.310	001110010	072	1.630
000010011	013	0.680	000110011	033	1.000	001010011	053	1.320	001110011	073	1.640
000010100	014	0.690	000110100	034	1.010	001010100	054	1.330	001110100	074	1.650
000010101	015	0.700	000110101	035	1.020	001010101	055	1.340	001110101	075	1.660
000010110	016	0.710	000110110	036	1.030	001010110	056	1.350	001110110	076	1.670
000010111	017	0.720	000110111	037	1.040	001010111	057	1.360	001110111	077	1.680
000011000	018	0.730	000111000	038	1.050	001011000	058	1.370	001111000	078	1.690
000011001	019	0.740	000111001	039	1.060	001011001	059	1.380	001111001	079	1.700
000011010	01A	0.750	000111010	03A	1.070	001011010	05A	1.390	001111010	07A	1.710
000011011	01B	0.760	000111011	03B	1.080	001011011	05B	1.400	001111011	07B	1.720
000011100	01C	0.770	000111100	03C	1.090	001011100	05C	1.410	001111100	07C	1.730
000011101	01D	0.780	000111101	03D	1.100	001011101	05D	1.420	001111101	07D	1.740
000011110	01E	0.790	000111110	03E	1.110	001011110	05E	1.430	001111110	07E	1.750
000011111	01F	0.800	000111111	03F	1.120	001011111	05F	1.440	001111111	07F	1.760

Table 44. Type 2 Target VID Table (Part 2)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
010000000	080	1.770	010100000	0A0	2.090	011000000	0C0	2.410	011100000	0E0	2.730
010000001	081	1.780	010100001	0A1	2.100	011000001	0C1	2.420	011100001	0E1	2.740
010000010	082	1.790	010100010	0A2	2.110	011000010	0C2	2.430	011100010	0E2	2.750
010000011	083	1.800	010100011	0A3	2.120	011000011	0C3	2.440	011100011	0E3	2.760
010000100	084	1.810	010100100	0A4	2.130	011000100	0C4	2.450	011100100	0E4	2.770
010000101	085	1.820	010100101	0A5	2.140	011000101	0C5	2.460	011100101	0E5	2.780
010000110	086	1.830	010100110	0A6	2.150	011000110	0C6	2.470	011100110	0E6	2.790
010000111	087	1.840	010100111	0A7	2.160	011000111	0C7	2.480	011100111	0E7	2.800
010001000	088	1.850	010101000	0A8	2.170	011001000	0C8	2.490	011101000	0E8	2.810
010001001	089	1.860	010101001	0A9	2.180	011001001	0C9	2.500	011101001	0E9	2.820
010001010	08A	1.870	010101010	0AA	2.190	011001010	0CA	2.510	011101010	0EA	2.830
010001011	08B	1.880	010101011	0AB	2.200	011001011	0CB	2.520	011101011	0EB	2.840
010001100	08C	1.890	010101100	0AC	2.210	011001100	0CC	2.530	011101100	0EC	2.850
010001101	08D	1.900	010101101	0AD	2.220	011001101	0CD	2.540	011101101	0ED	2.860
010001110	08E	1.910	010101110	0AE	2.230	011001110	0CE	2.550	011101110	0EE	2.870
010001111	08F	1.920	010101111	0AF	2.240	011001111	0CF	2.560	011101111	0EF	2.880
010010000	090	1.930	010110000	0B0	2.250	011010000	0D0	2.570	011110000	0F0	2.890
010010001	091	1.940	010110001	0B1	2.260	011010001	0D1	2.580	011110001	0F1	2.900
010010010	092	1.950	010110010	0B2	2.270	011010010	0D2	2.590	011110010	0F2	2.910
010010011	093	1.960	010110011	0B3	2.280	011010011	0D3	2.600	011110011	0F3	2.920
010010100	094	1.970	010110100	0B4	2.290	011010100	0D4	2.610	011110100	0F4	2.930
010010101	095	1.980	010110101	0B5	2.300	011010101	0D5	2.620	011110101	0F5	2.940
010010110	096	1.990	010110110	0B6	2.310	011010110	0D6	2.630	011110110	0F6	2.950
010010111	097	2.000	010110111	0B7	2.320	011010111	0D7	2.640	011110111	0F7	2.960
010011000	098	2.010	010111000	0B8	2.330	011011000	0D8	2.650	011111000	0F8	2.970
010011001	099	2.020	010111001	0B9	2.340	011011001	0D9	2.660	011111001	0F9	2.980
010011010	09A	2.030	010111010	0BA	2.350	011011010	0DA	2.670	011111010	0FA	2.990
010011011	09B	2.040	010111011	0BB	2.360	011011011	0DB	2.680	011111011	0FB	3.000
010011100	09C	2.050	010111100	0BC	2.370	011011100	0DC	2.690	011111100	0FC	3.010
010011101	09D	2.060	010111101	0BD	2.380	011011101	0DD	2.700	011111101	0FD	3.020
010011110	09E	2.070	010111110	0BE	2.390	011011110	0DE	2.710	011111110	0FE	3.030
010011111	09F	2.080	010111111	0BF	2.400	011011111	0DF	2.720	011111111	0FF	3.040

Table 45. Type 2 Target VID Table (Part 3)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
100000000	100	3.050	100100000	120	3.370	101000000	140	3.690	101100000	160	4.010
100000001	101	3.060	100100001	121	3.380	101000001	141	3.700	101100001	161	4.020
100000010	102	3.070	100100010	122	3.390	101000010	142	3.710	101100010	162	4.030
100000011	103	3.080	100100011	123	3.400	101000011	143	3.720	101100011	163	4.040
100000100	104	3.090	100100100	124	3.410	101000100	144	3.730	101100100	164	4.050
100000101	105	3.100	100100101	125	3.420	101000101	145	3.740	101100101	165	4.060
100000110	106	3.110	100100110	126	3.430	101000110	146	3.750	101100110	166	4.070
100000111	107	3.120	100100111	127	3.440	101000111	147	3.760	101100111	167	4.080
100001000	108	3.130	100101000	128	3.450	101001000	148	3.770	101101000	168	4.090
100001001	109	3.140	100101001	129	3.460	101001001	149	3.780	101101001	169	4.100
100001010	10A	3.150	100101010	12A	3.470	101001010	14A	3.790	101101010	16A	4.110
100001011	10B	3.160	100101011	12B	3.480	101001011	14B	3.800	101101011	16B	4.120
100001100	10C	3.170	100101100	12C	3.490	101001100	14C	3.810	101101100	16C	4.130
100001101	10D	3.180	100101101	12D	3.500	101001101	14D	3.820	101101101	16D	4.140
100001110	10E	3.190	100101110	12E	3.510	101001110	14E	3.830	101101110	16E	4.150
100001111	10F	3.200	100101111	12F	3.520	101001111	14F	3.840	101101111	16F	4.160
100010000	110	3.210	100110000	130	3.530	101010000	150	3.850	101110000	170	4.170
100010001	111	3.220	100110001	131	3.540	101010001	151	3.860	101110001	171	4.180
100010010	112	3.230	100110010	132	3.550	101010010	152	3.870	101110010	172	4.190
100010011	113	3.240	100110011	133	3.560	101010011	153	3.880	101110011	173	4.200
100010100	114	3.250	100110100	134	3.570	101010100	154	3.890	101110100	174	4.210
100010101	115	3.260	100110101	135	3.580	101010101	155	3.900	101110101	175	4.220
100010110	116	3.270	100110110	136	3.590	101010110	156	3.910	101110110	176	4.230
100010111	117	3.280	100110111	137	3.600	101010111	157	3.920	101110111	177	4.240
100011000	118	3.290	100111000	138	3.610	101011000	158	3.930	101111000	178	4.250
100011001	119	3.300	100111001	139	3.620	101011001	159	3.940	101111001	179	4.260
100011010	11A	3.310	100111010	13A	3.630	101011010	15A	3.950	101111010	17A	4.270
100011011	11B	3.320	100111011	13B	3.640	101011011	15B	3.960	101111011	17B	4.280
100011100	11C	3.330	100111100	13C	3.650	101011100	15C	3.970	101111100	17C	4.290
100011101	11D	3.340	100111101	13D	3.660	101011101	15D	3.980	101111101	17D	4.300
100011110	11E	3.350	100111110	13E	3.670	101011110	15E	3.990	101111110	17E	4.310
100011111	11F	3.360	100111111	13F	3.680	101011111	15F	4.000	101111111	17F	4.320

Table 46. Type 2 Target VID Table (Part 4)

SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage	SVID[8:0]		Voltage
Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)	Binary	Hex	(V)
110000000	180	4.330	110100000	1A0	4.650	111000000	1C0	4.970	111100000	1E0	5.290
110000001	181	4.340	110100001	1A1	4.660	111000001	1C1	4.980	111100001	1E1	5.300
110000010	182	4.350	110100010	1A2	4.670	111000010	1C2	4.990	111100010	1E2	5.310
110000011	183	4.360	110100011	1A3	4.680	111000011	1C3	5.000	111100011	1E3	5.320
110000100	184	4.370	110100100	1A4	4.690	111000100	1C4	5.010	111100100	1E4	5.330
110000101	185	4.380	110100101	1A5	4.700	111000101	1C5	5.020	111100101	1E5	5.340
110000110	186	4.390	110100110	1A6	4.710	111000110	1C6	5.030	111100110	1E6	5.350
110000111	187	4.400	110100111	1A7	4.720	111000111	1C7	5.040	111100111	1E7	5.360
110001000	188	4.410	110101000	1A8	4.730	111001000	1C8	5.050	111101000	1E8	5.370
110001001	189	4.420	110101001	1A9	4.740	111001001	1C9	5.060	111101001	1E9	5.380
110001010	18A	4.430	110101010	1AA	4.750	111001010	1CA	5.070	111101010	1EA	5.390
110001011	18B	4.440	110101011	1AB	4.760	111001011	1CB	5.080	111101011	1EB	5.400
110001100	18C	4.450	110101100	1AC	4.770	111001100	1CC	5.090	111101100	1EC	5.410
110001101	18D	4.460	110101101	1AD	4.780	111001101	1CD	5.100	111101101	1ED	5.420
110001110	18E	4.470	110101110	1AE	4.790	111001110	1CE	5.110	111101110	1EE	5.430
110001111	18F	4.480	110101111	1AF	4.800	111001111	1CF	5.120	111101111	1EF	5.440
110010000	190	4.490	110110000	1B0	4.810	111010000	1D0	5.130	111110000	1F0	5.450
110010001	191	4.500	110110001	1B1	4.820	111010001	1D1	5.140	111110001	1F1	5.460
110010010	192	4.510	110110010	1B2	4.830	111010010	1D2	5.150	111110010	1F2	5.470
110010011	193	4.520	110110011	1B3	4.840	111010011	1D3	5.160	111110011	1F3	5.480
110010100	194	4.530	110110100	1B4	4.850	111010100	1D4	5.170	111110100	1F4	5.490
110010101	195	4.540	110110101	1B5	4.860	111010101	1D5	5.180	111110101	1F5	5.500
110010110	196	4.550	110110110	1B6	4.870	111010110	1D6	5.190	111110110	1F6	5.510
110010111	197	4.560	110110111	1B7	4.880	111010111	1D7	5.200	111110111	1F7	5.520
110011000	198	4.570	110111000	1B8	4.890	111011000	1D8	5.210	111111000	1F8	5.530
110011001	199	4.580	110111001	1B9	4.900	111011001	1D9	5.220	111111001	1F9	5.540
110011010	19A	4.590	110111010	1BA	4.910	111011010	1DA	5.230	111111010	1FA	5.550
110011011	19B	4.600	110111011	1BB	4.920	111011011	1DB	5.240	111111011	1FB	5.560
110011100	19C	4.610	110111100	1BC	4.930	111011100	1DC	5.250	111111100	1FC	5.570
110011101	19D	4.620	110111101	1BD	4.940	111011101	1DD	5.260	111111101	1FD	5.580
110011110	19E	4.630	110111110	1BE	4.950	111011110	1DE	5.270	111111110	1FE	5.590
110011111	19F	4.640	110111111	1BF	4.960	111011111	1DF	5.280	111111111	1FF	5.600

6.5.2 Voltage-on-the-Fly (VOTF) Timing

Refer to Section 5.5.2 for additional information about Voltage-on-the-Fly (VOTF) Timing.

6.5.2.1 VID Decay Mode

There are no specified slew rate requirements for negative VID transitions (transitioning from a higher voltage to a lower voltage).

To save power in certain applications, targets are capable of supporting VID Decay Mode (output capacitors discharge through load only). The activation of VID Decay Mode is programmable through an SVI3-defined register DECAY_CONDITIONS (see Section 6.11.3).

When VID Decay Mode is not enabled, targets actively transition from a higher voltage to a lower voltage.

6.5.3 Programmable Maximum / Minimum VID

Programmable maximum and minimum values can be set through registers (VID_MAX, VID_MIN) defined in Section 6.11.3. If a VID packet is received by a target which is outside the maximum/minimum VID range, the target doesn't change the target voltage and returns a NACK: Invalid Command.

Conversely, if the controller attempts to set the maximum VID below the present target VID, the target doesn't change the VID_MAX register and returns a NACK: Invalid Command.

If the controller attempts to set the minimum VID above the present target VID, the target doesn't change the VID_MIN register and returns a NACK: Invalid Command.

6.5.4 Programmable Voltage Offset / Trim

A programmable voltage offset VOUT_OFFSET can be applied to the VID for margining purposes and to allow for regulation of voltages beyond the VID table (dependent on regulator capability).

The offset is programmed through the registers described in Section 6.11.3. If the resultant VID request is beyond the capabilities of the regulator (VID + VOUT_OFFSET > MAX_VOUT_SUPPORTED or VID + VOUT_OFFSET < MIN_VOUT_SUPPORTED), the regulator returns a NACK: Invalid Command.

VOUT_OFFSET will shift OVP_THRESH and UVP_THRESH.

Table 47. Extended Voltage Range

Parameter	Min	Max	Unit
Extended VID range using offset	0.02	10.200	V

6.5.5 Output Voltage Accuracy

The specification shown in Table 48. Type 2 Output Voltage Accuracy refers to the zero-load DC accuracy requirements of the voltage regulator's output.

Table 48. Type 2 Output Voltage Accuracy

VID (V)	Controller T_j °C[1]	Min	Max	Unit
0.500 to 0.995	-40 to 0	-10	+10	mV
1.000 to 5.600	-40 to 0	-1	+1	%
0.500 to 0.995	0 to 85	-5	+5	mV
1.000 to 5.600	0 to 85	-0.5	+0.5	%
0.500 to 0.995	85 to 125	-7.5	+7.5	mV
1.000 to 5.600	85 to 125	-0.75	+0.75	%
Note: *It is not required that SVI3 devices support the entire temperature range from -40°C to 125°C.*				

6.6 Load-Line

The nominal load-line slope is 0 mΩ for Type 2 devices.

6.7 Power States

The regulator is capable of transitioning from any PSI state to any PSI state.

Table 49. Type 2 Power States

PSI	Action
0	Force CCM (Continuous Conduction Mode) (default)
1	Not Supported - NACK
2	Not Supported - NACK
3	Single phase operation + active diode emulation (low-side actively driven when I_ind is positive)
4	Not Supported - NACK
5	Reserved
6	Power down to 0V (voltage regulation disabled). PWRGD pin remains asserted. All non-essential systems are shutdown. No telemetry is measured by target. However, targets must still pass-through telemetry packets and add its header packet for proper framing (if SVI3 interface is enabled)
7	Not Supported – NACK

6.7.1 PWR_ENABLE Effect on Power States

For additional information, see Section 5.7.1.

6.8 Output Voltage Regulation Disabled States

For additional information, see Section 5.8.

6.9 Faults / Warning / Lock-Outs

For additional information, see Section 5.9.

6.9.1 Under Voltage Lockout (UVLO)

6.9.1.1 Voltage Regulator Device VCC / Driver Voltage / Input Voltage

For additional information, see Section 5.9.1.1.

6.9.1.2 SVI3_VDDIO

For additional information, see Section 5.9.1.2.

6.9.2 Over Current Protection (OCP) Fault

Voltage regulator devices must support OCP for all rails. The detection of an OCP fault results in the fault shutdown described in Section 5.9.

The analog/digital signal representing the inductor current meets the parameters listed in Table 50. The current sense network must have a minimum bandwidth I_{IND}_BW and must be able to track current slew rates up to I_{IND}_SR. The maximum delay between the summed inductor current exceeding the OCP threshold and the regulator initiating power-down is listed in Table 50.

Table 50. Current Sensing Requirements

Parameter	Min	Typ.	Max	Unit
I_{IND}_BW (-3dB Bandwidth: output/inductor current)	250			kHz
I_{IND}_SR (slew rate referenced to inductor current)	-1000		1000	A/µs
OCP propagation delay (OCP_THRESH exceeded to shut down), OCP_FAULT_DELAY = 000b			1	µs

6.9.2.1 OCP Threshold Programmability

For additional information, see Section 5.9.2.1.

6.9.2.2 OCP Delay

For additional information, see Section 5.9.2.2.

6.9.3 OCP Warning/PCC (Peak Current Control)

The OCP Warning function is not required for Type 2 devices.

Note: *OCP Warning is also called PCC (Peak Current Control).*

6.9.3.1 OCP_L Pin Functionality

OCP_L is not required for Type 2 devices.

6.9.3.2 OCP Warning Programmability

OCP Warning is not required for Type 2 devices

6.9.4 Current Sensing and OCP Block Diagram

An example of a high-level block diagram detailing the current sensing and OCP functionality is shown in Figure 21. The figure also details the current sensing telemetry path.

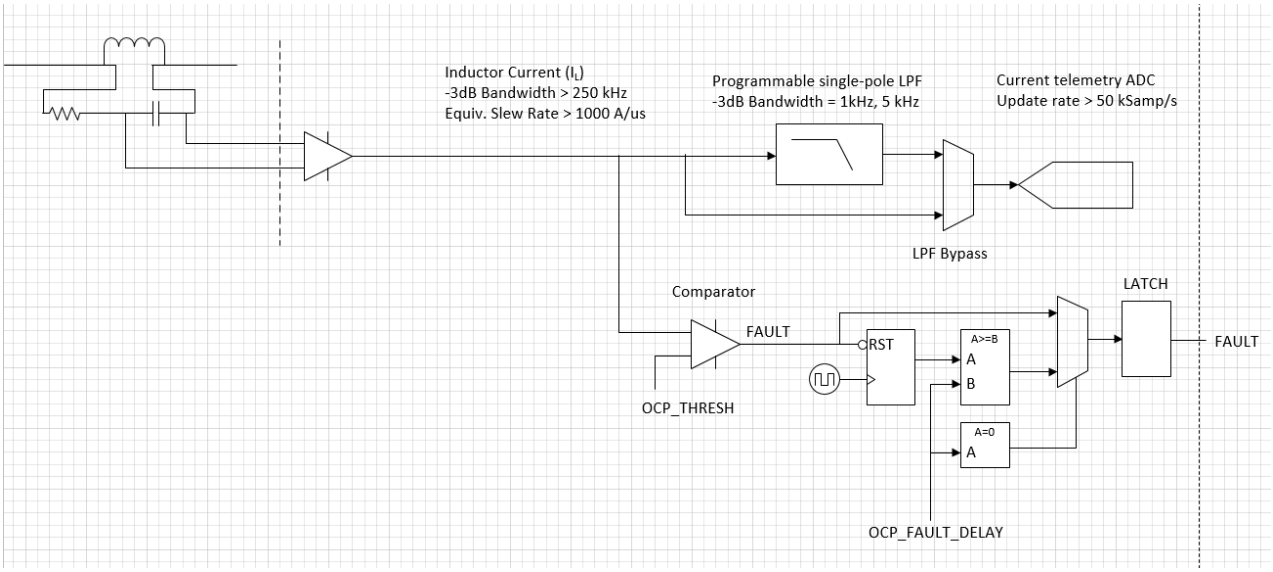

Figure 21. Current Sensing Telemetry Path

6.9.5 Over Voltage Protection (OVP) Fault

For additional information, see Section 5.9.5.

6.9.5.1 Over Voltage Protection (OVP): Voltage-on-the-Fly (VOTF) and Pre-bias Voltage

For additional information, see Section 5.9.5.1.

6.9.5.2 Over Voltage Protection (OVP) Programmability

For additional information, see Section 5.9.5.2.

6.9.6 Under Voltage Protection (UVP) Fault

For additional information, see Section 5.9.6.

6.9.6.1 UVP During VOTF

For additional information, see Section 5.9.6.1.

6.9.6.2 Under Voltage Protection (UVP) Programmability

For additional information, see Section 5.9.6.2.

6.9.7 Temperature Protection

6.9.7.1 VR-Hot Warning

For additional information, see Section 5.9.7.1.

6.9.7.2 Over Temperature Protection (OTP) Fault

For additional information, see Section 5.9.7.2.

6.9.8 Telemetry

For additional information, see Section 5.10.

6.9.9 Output Current (Telemetry Reg. Index 000b)

Output current telemetry consists of a 10-bit encoding that is mapped to three user-selectable scales.

The voltage regulator device must have the capability for the designer to select the appropriate current scale at the platform level (either by NVM or resistor selection). During start-up, the controller sets the output current scale register (see Section 6.11.1). The device reads back this register to determine the appropriate decoding scale. The output current ADC must maintain 10-bit resolution across all current scales and have no missing codes.

Table 51. Type 2 Output Current Scaling Selections

Current (A)									
		CUSTOM	32A	64A	Scale 3	Scale 4	Scale 5	Scale 6	Scale 7
Decimal	Binary	(000b)	(001b)	(010b)					
0	0000000000	0	0	0					
1	0000000001	CUSTOM	0.03125	0.0625					
2	0000000010	CUSTOM	0.0625	0.125					
3	0000000011	CUSTOM	0.09375	0.1875					
4	0000000100	CUSTOM	0.125	0.25					
.	.	.	.	.					
.	.	.	.	.					
.	.	.	.	.					
.	.	.	.	.					
1020	1111111100	CUSTOM	31.875	63.75					
1021	1111111101	CUSTOM	31.90625	63.8125					
1022	1111111110	CUSTOM	31.9375	63.875					
1023	1111111111	CUSTOM	31.96875	63.9375					

6.9.9.1 DCR Current Sensing Accuracy

For additional information, see Section 5.10.1.1.

6.9.9.2 Integrated Power-Stage Current Sensing Accuracy

For additional information, see Section 5.10.1.2.

6.9.9.3 Output Current Telemetry Bandwidth and Sampling Rate

For additional information, see Section 5.10.1.3.

6.9.10 Output Voltage (Telemetry Reg. Index 001b)

Explicit measurement of the output voltage for telemetry purposes is required for all rails.

Output voltage telemetry data payloads consist of 10 bits. The encoding formula for output voltage telemetry is shown below:

```
VOUT_TELEMETRY[9:0] = Output Voltage (V) / 10 mV
```

Output voltage continues to be measured and reported when the VID is set to “OFF”. This is intended to measure pre-bias voltage or decaying voltage.

6.9.10.1 Output Voltage Telemetry Accuracy

Output voltage telemetry accuracy requirements are described in Table 52.

Table 52. Output Voltage Telemetry Accuracy Requirements

VID (V)	Controller Tj °C[1]	Min	Max	Unit
0.500 to 0.995	–40 to 0	–15	+15	mV
1.000 to 5.600	–40 to 0	–1.5	+1.5	%
0.500 to 0.995	0 to 85	–15	+15	mV
1.000 to 5.600	0 to 85	–1.5	+1.5	%
0.500 to 0.995	85 to 125	–15	+15	mV
1.000 to 5.600	85 to 125	–1.5	+1.5	%

Note:

1. *It is not required that SVI3 devices support the entire temperature range from -40°C to 125°C.*

6.9.10.2 Output Voltage Telemetry Bandwidth

For additional information, see Section 5.10.2.

6.9.11 Input Current (Telemetry Reg Index 100b) *Optional*

For additional information, see Section 5.10.3.

6.9.12 Input Voltage (Telemetry Reg. Index 101b) *Optional*

For additional information, see Section 5.10.4.

6.9.13 Temperature 1 / Warn Status (Telemetry Reg. Index 010b)

Each rail is capable of reporting temperature telemetry that is representative of the “hot-spot” of the rail. VRHOT/OTP fault and temperature telemetry shares the same input signal.

The formula for reporting temperature in a 10-bit encoding is:

```
Temp 1 / Warn [9] = VRHOT (active low; 1b = not asserted, 0b =
asserted)

Temp 1 / Warn [8] = 1b

Temp 1 / Warn [7:0] = Roundup (Temperature °C + 40)
```

6.9.13.1 Temperature 1 / Warn Status Accuracy

For additional information, see Section 5.10.5.1.

6.9.13.2 Temperature 1 / Warn Status Sampling Speed

For additional information, see Section 5.10.5.2.

6.9.14 Temperature 2 (Telemetry Reg. Index 011b) *Optional*

For additional information, see Section 5.10.6.

6.10 Debug Functions

For additional information, see Section 5.10.7.

6.10.1 Extend Timeout

For additional information, see Section 5.11.1.

6.10.2 Output Flag Manual Over-Ride

When enabled, VR_HOT and PWRGD may be manually controlled.

For additional information, see Section 5.10.6.

6.10.3 Telemetry Test Pattern

For additional information, see Section 5.11.3.

6.11 Registers

SVI3-defined registers are defined in the following sub-sections. Manufacturer specific registers are not defined in the SVI3 specification and should be described in respective datasheets.

All undefined register bits are considered "Don't care".

6.11.1 Read-Only Register

Read-only registers are set by the manufacturer, by platform-level programming methods (NVM, resistor strap, etc.) or by a specialized SVI3 command. Read-only registers cannot be modified directly using the Write Register command. If a Write Register command attempts to modify a read-only register, the target returns a NACK: Invalid Command.

The SVI3-specific read-only registers are described in Table 53.

Table 53. Read-Only Registers

Addr (Hex)	Bits	Register Name	Description
01	[7:0]	SVI3_VERSION	Indicates the version of SVI3 for which the target is compliant. Equal to x in Rev. x.yy of Specification.
02	[7:5]	TYPE_ID	Indicates the type of the target 000b = Type 1: Multi-Phase Step-Down 001b = Type 2: Point of Load

Table 53. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
02	[4:0]	MFG_ID	Indicates the manufacturer of the target/controller To be defined 00h = AMD (Eval Platform) 01h = Infineon 02h = Monolithic Power Systems 03h = Renesas 04h = Richtek 05h = MaxLinear 06h = OnSemi 07h = STMicro 08h = µPI 09h = ADI/Maxim Integrated 0Ah = Texas Instruments 0Bh = Anpec 0Ch = Ferric 0Dh = Vicor 0Eh = Alpha and Omega Semiconductor 0Fh = Aura Semiconductor
03	[7:0]	MODEL_ID	Unique model code defined by manufacturer
04	[7:0]	TEN_BIT_TEL_AVAIL	Indicates which types of 10-bit telemetry are available (1b = available, 0b = unavailable) Bit 7 = Reserved Bit 6 = Mfg. Custom Telemetry Bit 5 = Input Voltage Bit 4 = Input Current Bit 3 = Temp 2 Bit 2 = Temp 1 Bit 1 = Output voltage Bit 0 = Output current

Table 53. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
05	[7:0]	SIXTEEN_BIT_TEL_AVAIL	Indicates which types of 16-bit telemetry are available (1b = enabled, 0b = disabled) Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Reserved Bit 3 = Reserved Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved
06	[7:7]	CRC_ENABLED	Indicates if CRC is enabled 1b = enabled (default) 0b = disabled *Note: CRC can only be enabled/disabled through global command*
06	[4:2]	PSI	Indicates the PSI state of the target
06	[0:0]	VID[8]	Indicates the MSB of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
07	[7:0]	VID[7:0]	Indicates the 8 LSBs of the VID. Default VID copied from VID_DEFAULT_VOLTAGE
08	[5:4]	DEFAULT_SLEW_RATE	Default slew rate programmed at platform level (NVM, resistor strap, etc.) 00b = 2.5 mV/us 01b = 10 mV/us 10b = 20 mV/us 11b = 40 mV/us

Table 53. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
08	[3:0]	VID_DEFAULT_VOLTAGE	Default VID, programmed at platform level (NVM, resistor strap, etc.) 0h = Off (wait for SVI3 VID command) 1h = 0.500 V 2h = 0.600 V 3h = 0.700 V 4h = 0.800 V 5h = 0.900 V 6h = 1.000 V 7h = 1.100 V 8h = 1.200 V 9h = 1.300 V Ah = 1.400 V Bh = 1.500 V Ch = 1.800 V Dh = 2.500 V Eh = 3.300 V Fh = 5.000 V
09	[7:6]	V_IN_SCALE	Input voltage scale, programmed at platform level (NVM, resistor strap, etc.) 00b = Custom Scale / Reserved 01b = Custom Scale / Reserved 10b = 32V Scale 11b = 64V Scale
09	[5:3]	I_OUT_SCALE	Output current scale, programmed at platform level (NVM, resistor strap, etc.) 000b = Custom Scale / Reserved 001b = 32A Scale 010b = 64A Scale 011b = Reserved 100b = Reserved 101b = Reserved 110b = Reserved 111b = Reserved

Table 53. Read-Only Registers (Continued)

Addr (Hex)	Bits	Register Name	Description
09	[2:0]	I_IN_SCALE	Input current scale, programmed at platform level (NVM, resistor strap, etc.) 000b = Custom Scale / Reserved 001b = 4A Scale 010b = 8A Scale 011b = 16A Scale 100b = 32A Scale 101b = 64A Scale 110b = 128A Scale 111b = 256A Scale
0A	[7:0]	MAX_VOUT_SUPPORTED	Maximum output voltage supported by voltage regulator Max Vout = Reg[7:0] * 40 mV
0B	[7:0]	MIN_VOUT_SUPPORTED	Minimum non-zero output voltage supported by voltage regulator Min Vout = Reg[7:0] * 5 mV

6.11.2 Status Registers

Status registers record occurrences of warnings, NACKs or faults. All status bits are active high. All status bits are "sticky" and are cleared by writing 0b to the appropriate bits, provided the fault condition no longer exists. Writing 1b doesn't affect the status of the associated bit. For example, writing FEh to the FAULT_STATUS register only clears the over current protection flag.

The SVI3-specific status registers are described in Table 54.

Table 54. Status Registers

Addr (Hex)	Bits	Register Name	Description
10	[7:0]	FAULT_STATUS	Sticky flag asserted high when a fault/warning occurs Bit 7 = Reserved (0b) Bit 6 = Reserved (0b) Bit 5 = VRHOT asserted Bit 4 = Reserved (0b) Bit 3 = OTP fault Bit 2 = UVP fault Bit 1 = OVP fault Bit 0 = OCP fault
11	[7:0]	NACK_STATUS	Sticky flag asserted when a NACK occurs Bit 7 = Reserved (0b) Bit 6 = Reserved (0b) Bit 5 = NACK: Communication Error: Command before ACK Bit 4 = NACK: Communication Error: Framing Error Bit 3 = NACK: Communication Error: CRC Error Bit 2 = NACK: Invalid Command: Undefined Register Command Bit 1 = NACK: Invalid Command: Undefined Payload Bit 0 = NACK: Invalid Command: Not Executable / Not Supported

6.11.3 Read/Write Registers

Read/Write registers can be modified by the controller using the Write Register command. The SVI3-specific Read/Write registers are described in Table 55. For Read/Write registers, it is expected that register defaults are extracted from NVM (if available). If NVN is not available, the default is defined in Table 55.

Table 55. Read/Write Registers

Addr (Hex)	Bits	Register Name	Description	Default (if NVM default is not available)
20	[7:5]	DECAY_CONDITIONS	Down voltage decay enabled for following conditions 1b = enabled 0b = disabled Bit 7 = Decay in PSI0 Bit 6 = Decay in PSI3 Bit 5 = Decay in PSI6 or when PWR_ENABLE is de-asserted	000b
20	[4:4]	DOWN_SLEW_RATE	Slew rate when decay conditions not met (i.e., active slew rate control) 1b: Negative slew rate = 1/4 positive slew rate 0b: Negative slew rate = positive slew rate	0b
20	[3:0]	UP_SLEW_RATE	Slew rate for positive VID change Slew rate = Reg[3:0] * 2.5 + 2.5 mV/us	Copied from DEFAULT_SLEW_RATE
22	[7:0]	VOUT_OFFSET	Voltage offset applied to VID, VID_MIN, VID_MAX, OVP_THRESH and UVP_THRESH 00h = Disabled (no offset) Offset = Reg[7:0] * 20 - 500 mV	00h
23	[7:0]	VID_MAX	Maximum settable VID command 00h = Disabled Maximum VID = Reg[7:0] * 20 mV + 500mV	00h
24	[7:0]	VID_MIN	Minimum settable VID command 00h = Disabled Minimum VID = Reg[7:0] * 20 mV + 500 mV	00h

Table 55. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM default is not available)
25	[7:0]	TEN_BIT_TEL_EN	Controls which types of 10-bit telemetry are enabled (1b = Enabled, 0b = Disabled) Bit 7 = Reserved Bit 6 = Mfg. Custom Telemetry Bit 5 = Input Voltage Bit 4 = Input Current Bit 3 = Temp 2 Bit 2 = Temp 1 Bit 1 = Output voltage Bit 0 = Output current	00h
26	[7:0]	SIXTEEN_BIT_TEL_EN	Controls which types of 16-bit telemetry are enabled (1b = Enabled, 0b = Disabled) Bit 7 = Reserved Bit 6 = Reserved Bit 5 = Reserved Bit 4 = Reserved Bit 3 = Reserved Bit 2 = Reserved Bit 1 = Reserved Bit 0 = Reserved	00h
27	[7:0]	OCP_THRESH	Over current protection threshold level 00h = Disabled (no OCP protection) OCP Threshold = Reg[7:0] * 4 * I_OUT_SCALE / 512 A	Platform
29	[2:0]	OCP_FAULT_DELAY	Continuous time that current must exceed OCP_THRESH before triggering fault 000b = Instantaneous fault Fault delay = Reg[2:0] * 5 us	NVM (or 000b if NVM is unavailable)

Table 55. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM default is not available)
2A	[7:0]	VRHOT_THRESH	Voltage regulator hot warning threshold 00h = Disabled VRHOT Threshold = Reg[7:0] - 40°C	8Ch (100°C)
2B	[7:0]	OTP_THRESH	Over temperature protection threshold 00h = Disabled OTP Threshold = Reg[7:0] - 40°C	A5h (125°C)
2C	[7:7]	OVP_REF	Reference to set over-voltage protection threshold 0b = VID, 1b = VID_MAX	0b
2C	[6:4]	OVP_DELTA	Delta value to set over-voltage protection threshold 000b = Disabled OVP Delta = Reg[6:4] * 100 + 100 mV	011b (400 mV)
2C	[3:3]	UVP_REF	Reference to set under-voltage protection threshold 0b = VID, 1b = VID_MIN	0b
2C	[2:0]	UVP_DELTA	Delta value to set under-voltage protection threshold 000b = Disabled UVP Delta = Reg[6:4] * 100 + 100 mV	011b (400 mV)
40	[7:0]	DEBUG_ENABLED	Bit 6 = Extend timeout clock by factor of 1024 Bit 5 = Overwrite Temp 1 telemetry enabled Bit 4 = Overwrite output voltage telemetry enabled Bit 3 = Overwrite output current telemetry enabled Bit 2 = Manually control PWRGD enabled Bit 1 = Manually control VRHOT enabled	00h

Table 55. Read/Write Registers (Continued)

Addr (Hex)	Bits	Register Name	Description	Default (if NVM default is not available)
41	[7:0]	DEBUG_TEMP1_OVERRIDE	Data payload for TEMP1 when bit 5 of register 40 is asserted	00h
42	[7:0]	DEBUG_VOUT_OVERRIDE	Data payload for VOUT_TELEMETRY[9:2] when bit 4 of register 40 is asserted	00h
43	[1:0]	DEBUG_VOUT_OVERRIDE	Data payload for VOUT_TELEMETRY[1:0] when bit 4 of register 40 is asserted	00b
44	[7:0]	DEBUG_IOUT_OVERRIDE	Data payload for IOUT_TELEMETRY[9:2] when bit 3 of register 40 is asserted	00h
45	[1:0]	DEBUG_IOUT_OVERRIDE	Data payload for IOUT_TELEMETRY[1:0] when bit 3 of register 40 is asserted	00b
46	[2:0]	DEBUG_OUTPUT_OVERRIDE	Bit 2 = PWRGD when bit 2 of register 40 is asserted Bit 1 = VRHOT when bit 1 of register 40 is asserted	000b
50	[7:0]	GEN_PURPOSE_0	General purpose register 0	00h
51	[7:0]	GEN_PURPOSE_1	General purpose register 1	00h
52	[7:0]	GEN_PURPOSE_2	General purpose register 2	00h
53	[7:0]	GEN_PURPOSE_3	General purpose register 3	00h
54	[7:0]	GEN_PURPOSE_4	General purpose register 4	00h
55	[7:0]	GEN_PURPOSE_5	General purpose register 5	00h
56	[7:0]	GEN_PURPOSE_6	General purpose register 6	00h
57	[7:0]	GEN_PURPOSE_7	General purpose register 7	00h

NACK Conditions

Table 56 outlines SVI3 NACK conditions and the expected target response.

Table 56. SVI3 NACK Conditions and Expected Target Response

Item	Condition	ACK Response [1:0]	NACK_ STATUS Bit Asserted	NACK Target
CBA				
1	New command received before the previous command acknowledge was processed	11b	5	Every target that detects error
CE				
1	Communication Error: Framing; missing start/stop packet	11b	4	Every target that detects error
2	Communication Error: CRC Error	11b	3	Every target that detects error
URC				
1	Write to register offset not defined in SVI3 spec	10b	2	Selected target
2	Read from register offset not defined in SVI3 spec	10b	2	Selected target
3	Write to manufacturer register not defined by manufacturer	10b	2	Selected target
4	Read from manufacturer register not defined by manufacturer	10b	2	Selected target
5	Command type is 000b or 101b or 110b	10b	2	Selected target
6	Bit 8 or Bit 9 is 0b for Register Read command	10b	2	Selected target
7	Bit 17 or Bit 16 is 0b for Register Write command	10b	2	Selected target
URCP				
1	Change power state to PSI1, PSI2, PSI4, PSI5, and PSI7 (Reserved)	10b	1	Selected target
2	LL_ADJUST payload greater 14h	10b	1	Selected target
3	TEN_BIT_TEL_EN with bit 7 1b (Reserved)	10b	1	Selected target
4	Write 0000b to PHASE_SHED_1 or PHASE_SHED_2	10b	1	Selected target
5	Global command with payload 100b or 101b	10b	1	All targets

Table 56. SVI3 NACK Conditions and Expected Target Response (Continued)

Item	Condition	ACK Response [1:0]	NACK_STATUS Bit Asserted	NACK Target
	NENS			
1	VID_MAX < VID_MIN when VID_MAX ≠ 0	10b	0	Selected target
2	SET VID_MAX < VID when VID_MAX ≠ 0	10b	0	Selected target
3	SET VID_MIN > VID when VID ≠ 0	10b	0	Selected target
4	SET VID > VID_MAX when VID_MAX ≠ 0	10b	0	Selected target
5	SET VID < VID_MIN when VID ≠ 0	10b	0	Selected target
6	SET VID that causes VID + OFFSET > MAX_VOUT_SUPPORTED	10b	0	Selected target
7	SET VID that causes VID + OFFSET < MIN_VOUT_SUPPORTED when VID ≠ 0	10b	0	Selected target
8	SET OFFSET that causes VID + OFFSET > MAX_VOUT_SUPPORTED	10b	0	Selected target
9	SET OFFSET that causes VID + OFFSET < MIN_VOUT_SUPPORTED when VID ≠ 0	10b	0	Selected target
10	Write registers to read only registers	10b	0	Selected target
11	Enable unsupported telemetry (10 bit)	10b	0	Selected target
12	Enable unsupported telemetry (16 bit)	10b	0	Selected target
13	Write to PHASE_SHED_1 or PHASE_SHED_2 with phase count greater than supported	10b	0	Selected target
14	Global command sent in command stream	10b	0	All targets
15	Address > Max targets (for Address or VID packet type)	10b	0	Terminal Target
16	Address = 0 (for Address or VID packet type)	10b	0	All targets
17	Address Packet <= Address offset during initialization	10b	0	Every target that detects error
18	Non-global command sent before valid address pointed	10b	0	All targets
19	CRC enable/disable, initialization or Telemetry Request during telemetry process	10b	0	Every target that detects error target

Notes: *CBA = Command Before ACK*
CE = Communication Error
URC = Undefined Register / Command
URCP = Undefined Register / Command Payload
NENS = Not Executable / Not Supported