Vess A-class

(ASRock C236WSI)

BIOS Customization Requirement Document

Version 1.17

Date: 2019/08/27

Revision History

Revision	Date	Author	Description
1.0	2015/08/20	Billy Chiu	Add items 1~8.
1.1	2015/09/21	Billy Chiu	Add item 9, 10 and 11.
1.2	2015/09/23	Billy Chiu	Modify item 11.
1.3	2015/10/02	Billy Chiu	Update item 11, add item 12.
1.4	2015/10/21	Billy Chiu	Add new item 13
1.5	2015/12/03	Billy Chiu	Add new item 14
1.6	2016/03/07	Billy Chiu	Add new item 15, 16
1.7	2016/03/31	Billy Chiu	Modify item 6
1.8	2017/02/20	Samuel Lee	Add new item 17
1.9	2017/03/06	Eric Chung	Add new item 18
1.10	2017/06/08	Eric Chung	Add new item 19
1.11	2017/08/31	Eric Chung	Merge item 17, 18, 19 to one item 17 Modify item 17
1.12	2017/09/29	Eric Chung	Add new item 18, 19 Modify item 7, item 13
1.13	2017/10/18	Eric Chung	Modify item 19

1.15.1 1.15.2	2017/12/15	Eric Chung	Add item 20
1.16	2018/05/11	FILIPE LAO	Add item 21
1.17	**2018/08/27**	**Roy Wu**	**Add new item 22, 23**

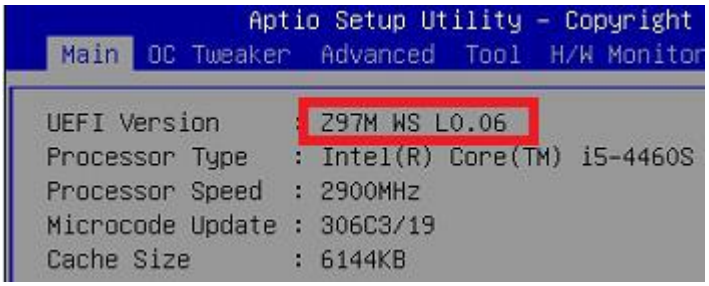
Promise BIOS Customization

1. BIOS Logo:

Please remove the BIOS Logo as black screen, but please help to keep information to indicate user how to enter BIOS and boot device manu.

2. Model Name:

Please help to remove the module name "**C236WSI**" from UEFI Version, but only keep the version number for checking.



3. Boot Device Sequence:

Please help to change the default boot device sequence,
USB -> DVD -> SATA device

4. Add Supervisor Password:

Please help to add the default supervisor password as "**VessApp**"

5. Remove key words on all BIOS information:

Please help to remove all the related key words as below,

- **ASRock**.
- **C236WSI**

6. Change the default setting of PCIE Device Power On:

~~Please help to change the default setting of "PCEI Device Power On" as "**Enabled**"~~

Please help to change the default setting of "PCEI Device Power On" as "**Disable**"

7. Change the default setting of Restore on AC/Power Loss:

Please help to change the default setting of "Restore on AC/Power Loss" as "**Power On**".

8. Reserve Memory:

Please help to reserve the memory and write information on special memory address.

a. Reserve memory pool,
   If system memory >= 8 GB, reserve 1GB.
   If system memory >= 4 GB, reserve 512MB.
   Others, reserve 256MB.

b. Reserve memory header, (the memory area is fixed)

- Start at 0x10000000
- Here is the structure about the header, please help to fill the red fields.

```
typedef struct ReservedMemoryHeaderInfo
{
   u8  rmhi_Signature1[4];              /* fill [P, r, o, e] for verification*/
   u32 rmhi_ReservedMemSize;      /* fill the size (MB) of reserved memory */
   u32 rmhi_ReservedMemLow;       /* (low) for reserve memory start address */
   u32 rmhi_ReservedMemHigh;      /* (high) for reserve memory start address */
   u8  rmhi_UEFI;                 /* for BIOS type */
   u8  rmhi_BIOSVendor;           /* for BIOS Vendor */
   u16 rmhi_PlatformType;         /* (Promise define)for Platform type */
   u8  rmhi_SouthBridge;          /* SouthBrigdge chipset */
   u8  rmhi_Reserved1[3];
   u64 rmhi_MemorySize;           /* (MB) Memory Size */
   u8  rmhi_MemoryNumber;         /* Memory number */
   u8  rmhi_Reserved2[1];
   u16 rmhi_MemoryBusWidth;       /* Memory Bus Bandwidth */
   u16 rmhi_MemorySpeed;          /* Memory Speed */
   u8  rmhi_MemoryGeneration;     /* Memory Generation */
   u8  rmhi_MemoryECCType;        /* Support ECC or not */
   u8  rmhi_BackendChipType;      /* Backend chip type */
   u8  rmhi_BackendChipNumber;    /* Backend chip number */
   u8  rmhi_CtrlBoardId;          /* Please fill “0xB1” for mother board model*/
   u8  rmhi_PSUType;              /* PSU type (VPD offset 0x70) */
   u8  rmhi_Reserved3[3];
   u32 rmhi_BootDeviceSize;       /* Size of boot device */
   u8  rmhi_PreInstallMode;
   u8  rmhi_BiosMajorVer;
   u8  rmhi_BiosMinorVer;
   u8  rmhi_BiosBuildNum;
   u32 rmhi_BiosOEMCode;
   u8  rmhi_BiosBuildMonth;
   u8  rmhi_BiosBuildDate;
   u16 rmhi_BiosBuildYear;
   u8  rmhi_Buffer[244];
   u8  rmhi_Signature2[4];        /* fill [E, O, R, p] for verification */
   u16 rmhi_PCIDeviceList[31][2];  /* list PCI device, VID and DID */
   u8  rmhi_PromiseProduct;       /* Check if it is Promise Product */
}ReservedMemoryHeaderInfo_t;
```

9. Change the default setting of SATA Mode Selection:

Please help to change the default setting of “SATA Mode Selection” as “**RAID**”.

F2 => Advanced => Storage Configuration => SATA Mode Selection => [RAID]

10. Remove the Intel RAID Option ROM:

Please help to remove the option ROM of Intel RAID.

11. Please help to set the Peripheral device:

Please help to setting the default value in I2C device.

/* Fan control */

/* Chip init */

// Write "0x00" to address "0x5C" offset 0x00

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x00
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x00" to address "0x5C " offset 0x21

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x21
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x00" to address "0x5C " offset 0x5E

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x5E
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x00" to address "0x5C " offset 0x5F

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x5F
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x01" to address "0x5C " offset 0x21

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x21
4. Set host data (SMB_BASE+0x05): Write 0x01
5. Set host control (SMB_BASE+0x02): Write 0x48

/* Set fan speed */

// Write "0x0F" to address "0x5C " offset 0x60

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x60
4. Set host data (SMB_BASE+0x05): Write 0x0F
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x0F" to address "0x5C " offset 0x61

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x5C
3. Set host command (SMB_BASE+0x03): Write 0x61
4. Set host data (SMB_BASE+0x05): Write 0x0F
5. Set host control (SMB_BASE+0x02): Write 0x48

/* LED init */

/* Clear Output port value */

// Write "0x00" to address "0x40" port0

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x40
3. Set host command (SMB_BASE+0x03): Write 0x02
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x00" to address "0x40" port1

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x40
3. Set host command (SMB_BASE+0x03): Write 0x03
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

//Write "0x00" to address "0x42" port0

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x42
3. Set host command (SMB_BASE+0x03): Write 0x02
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

//Write "0x00" to address "0x42" port1

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x42
3. Set host command (SMB_BASE+0x03): Write 0x03
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

/* Configure the I/O pins */

// Write "0x00" to address "0x40" port0

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x40
3. Set host command (SMB_BASE+0x03): Write 0x06
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x00" to address "0x40" port1

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x40
3. Set host command (SMB_BASE+0x03): Write 0x07
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

//Write "0x00" to address "0x42" port0

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x42
3. Set host command (SMB_BASE+0x03): Write 0x06
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

//Write "0x80" to address "0x42" port1

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x42
3. Set host command (SMB_BASE+0x03): Write 0x07
4. Set host data (SMB_BASE+0x05): Write 0x80
5. Set host control (SMB_BASE+0x02): Write 0x48

/* Set Output port value */

// Write "0x00" to address "0x40" port0

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x40
3. Set host command (SMB_BASE+0x03): Write 0x02
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

// Write "0x00" to address "0x40" port1

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x40
3. Set host command (SMB_BASE+0x03): Write 0x03
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

//Write "0x40" to address "0x42" port0

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x42
3. Set host command (SMB_BASE+0x03): Write 0x02
4. Set host data (SMB_BASE+0x05): Write 0x40
5. Set host control (SMB_BASE+0x02): Write 0x48

//Write "0x00" to address "0x42" port1

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x42
3. Set host command (SMB_BASE+0x03): Write 0x03
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

/* HDD spin up */

/* HDD spin up */

// Write "0xF0" to address "0x70"

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x70
3. Set host command (SMB_BASE+0x03): Write 0x00
4. Set host data (SMB_BASE+0x05): Write 0xF0
5. Set host control (SMB_BASE+0x02): Write 0x48

Delay 2 seconds

//Write "0x00" to address "0x70"

1. Check host status (SMB_BASE+0x00): Read HST_STS => Return 0x40
2. Set Slave address (SMB_BASE+0x04): Write 0x70
3. Set host command (SMB_BASE+0x03): Write 0x00
4. Set host data (SMB_BASE+0x05): Write 0x00
5. Set host control (SMB_BASE+0x02): Write 0x48

12. Please help to enable SPD write on BIOS:

Please help to change the default setting of SPD write to be eanbled.

13. Please help to set default fan speed to Silent:

Please help to set the default fan speed to Silent to decrease the noise.

⇨ Advanced -> H/W Monitor -> CPU_FAN1 -> [Silent Mode]

⇨ Advanced -> H/W Monitor -> FRNT_FAN1 -> [Silent Mode]

14. Please help to set default PCIE configuration to be [x8x4x4]:

Please help to set the default PCIE configuration be be [x8x4x4] to support Promise Riser card as a default component.

⇨ Advanced -> Chipset Configuration -> PCIE7 Link Width -> [x8x4x4]

15. Please help to set the default IGPU Multi-Monitor to be Enable:

⇨ Advanced -> Chipset Configuration -> IGPU Multi-Monitor -> [Enabled]

16. Please help to remove the confirm dialog after BIOS update completely.

17. Video BIOS and Micro Code for SkyLake & KabyLake

Please help update version of video BIOS to 1054 or latest version and update version of Micro Code for Skylake Series : 506E3/BA and Kabylake Series: 906E9/5E or latest version.

18. [2017/10/18] Change the default setting of Primary Graphics Adapter:

Please help to change the default setting of “Primary Graphics Adapter” as “**Onboard**”

19. [2017/10/18] Change the default setting of Launch video OpRom Policy:

Please help to change the default setting of "Launch video OpRom Policy" as "**Legacy only**"

20. **[2017/12/15] Add Intel Q3'17 ME 11.x, SPS 4.0, and TXE 3.0 Security Review Cumulative Update**
    Please help add Update ME version to 11.8.50.3399 to fix this risk.
21. **[2018/05/11] Add MCU Patch for issue "Spectre & Meltdown"**
22. **Change default setting of "Top of Lower Usable Dram" as "2.25GB" to keep sufficient 1GB reserved memory while add-on PCIE VGA card is adopted.**
23. **Change default setting of "Share Memory" as "128MB" to keep sufficient 1GB reserved memory while add-on PCI-E VGA card is adopted.**