Cadence Allegro and OrCAD (Including EDM): What's New in Release 17.2-2016

This document describes the new features and enhancements in Cadence® Allegro® and OrCAD® (Including EDM[1]) products in release 17.2-2016 (also referred to as 17.2 in this document).

1. Previously known as ADW.

Release-Level Changes

This section describes the enhancements and new features in Cadence® Allegro® and OrCAD® release 17.2-2016.

Product Rebranding

The ADW product line, individual ADW products, and product family names have been rebranded in release 17.2-2016. The Allegro Design Workbench (ADW) is now referred to as Allegro Engineering Data Management (EDM).

The following table lists the new terminology:

Original Term and Usage	New Terms
Allegro Design Workbench (when referring to the ADW product family)	Allegro EDM
ADW (when referring to the ADW product family)	Allegro EDM
Allegro Design Workbench (when referring to the PCB Design Workbench)	Allegro Data Manager
ADW (when referring to the PCB Design Workbench)	Allegro Data Manager
Allegro PCB Design Workbench	Allegro Data Manager
Allegro PCB Library Workbench	Allegro Library Manager
Component Browser	Part Information Manager
ECAD Collaboration Workbench	Allegro Pulse
Team Design Authoring, TDA, TDO	Allegro Design Management

Changes to Documentation Titles

The following table lists the changes to documentation titles:

Previous Title	New Title
ADW Administrator Reference Guide	Allegro® EDM Administrator Reference Guide
ADW Object Import User Guide	Allegro® EDM Object Import User Guide
Allegro® Design Workbench Solution Overview	Allegro® EDM Solution Overview
Allegro® Design Workbench Design Migration Guide	Allegro® EDM Migration Guide

Previous Title	New Title
Allegro® Design Workbench Configuration Guide	Allegro® EDM Configuration Guide
Allegro® Design Workbench Flow Manager User Guide	Allegro® EDM Flow Manager User Guide
Allegro® Design Workbench Database Administrator User Guide	Allegro® EDM Database Administrator User Guide
Allegro® Design Workbench Database Editor User Guide	Allegro® EDM Database Editor User Guide
Allegro® Design Workbench Library Distribution User Guide	Allegro® EDM Library Distribution User Guide
Allegro® Design Workbench Library Import Guide	Allegro® EDM Library Import User Guide
Allegro® Design Workbench Data Exchange Reference Guide	Allegro® EDM Data Exchange Reference Guide
Allegro® Design Workbench Library Flow User Guide	Allegro® EDM Library Flow User Guide
Allegro® Design Workbench: What's New in Release	Allegro® EDM: What's New in Release
Component Browser User Guide	Part Information Manager User Guide
Allegro® Design Workbench Version Management Utilities Guide	Allegro® EDM Version Management Utilities User Guide
Allegro® Design Authoring Team Design Option User Guide	Allegro® Design Management User Guide

Installation Directory Structure Changes

With 17.2-2016, the Cadence Allegro and OrCAD (Including EDM) hierarchy has been modified. All the user-accessible programs are now consolidated in the `<installation_directory>/tools/bin` folder. Sub-binary directories, such as `pcb/bin` and `fet/bin` no longer appear in the `PATH` environment variable, as they do not contain any user-accessible programs. It is no longer required to set the environment `PATH` variable to run 17.2-2016 programs.

The 17.2-2016 version of Cadence SPB Switch Release is updated to understand the Cadence hierarchy differences between releases. The Windows file associations path differences are automatically updated between releases.

If you run batch programs from the command prompt (`cmd.exe`) or batch files, a new batch file, `allegro_cmd.bat`, is provided in the `<installation_directory>\tools\bin` folder. Modify your batch file to include `<installation_directory>\tools\bin\allegro_cmd.bat`. If you run installed products from the command prompt, add `<installation_directory >\tools\bin` to the *PATH* variable.

In 17.2-2016, only documents for the selected products are installed. This is different from previous releases that installed all or no documents.

The latest version of the online help tool, Cadence Help, creates a table of content on the fly and then updates the search index to enable searching content across installed documents. The installer provides a new option to generate search index at the end of installing the products. If you are installing a server, generate the documentation index by selecting the option so that users accessing the server can view and search documents.

Support Only for 64-Bit Windows Operating Systems

The 17.2-2016 products are supported only on the following 64-bit versions of Windows operating systems:

- Microsoft® Windows® 7 (Enterprise, Ultimate, Professional, or Home Premium)
- Microsoft® Windows® 8 (All service packs, such as Windows 8.1)
- Microsoft® Windows® 10
- Microsoft® Windows® 2008 Server R2
- Microsoft® Windows® 2012 Server

Cadence Allegro and OrCAD (Including ADW) Installer for Windows

This section describes the enhancements and new features in the Cadence® Allegro® and OrCAD® (Including ADW) Windows Installer for Release 17.2-2016.

New License Manager

You must remove any earlier version and upgrade the License Manager to the Cadence License Manager 12.05 (FlexNet® LMTOOLS 13.0.3) version shipped with Cadence Allegro and OrCAD (Including EDM) Installer 17.2-2016 for the installed products to work. License Manager shipped with earlier releases will not work for the 17.2-2016 products.

To use Cadence products, setup licensing locally or over a network.

Important

Remove or uninstall any earlier version of License Manager before installing Cadence License Manager 12.05.

1. Install the latest license manager shipped with the installer.

   To check the LMTOOLS version installed in your system, start LMTOOLS (choose *Cadence — License Manager — LmTools* from the Start menu) and then choose *Help — About*.

2. Replace the license file in the License Server
3. In the system where products are installed, configure the license server

   Note: For more information, refer to the section on Licensing in this manual.

Cadence Download Manager

Use the new Cadence® Download Manager to download and install available Cadence Allegro and OrCAD (Including EDM) product releases and updates. The easy to use manager lets you quickly view, install, and update products from a single window without opening any external browser.

Use the Updates tab of the Preferences dialog box of Cadence Download Manager to schedule automatic updates. Specify the update mode, select packages, and set the schedule by specifying start time, frequency (in terms of weekly recurrence), and the days of the week.

The Download Manager can also be used to manage a local cache to store releases and updates for distribution across an enterprise, streamlining the deployment process.

The user friendly interface lets you keep a tab on all Cadence Allegro and OrCAD (Including EDM) downloads and installations by displaying the current status of downloads and installations. You can also pause a download and then resume it at a later time, ensuring that the download starts from where it was stopped.

Installing Without Administrative Privileges

You can now perform installation without administrative privileges (standard-user) using the *Only for me* option. If you do not have administrative privileges and need to install hotfixes, ensure that you install products as a standard user.

For base releases, install the products as a standard user and then configure the installation by running the `InstallConfig` utility using administrative privileges. This utility is present in the `<installation_location>\tools\InstallUtils` folder. The configuration is required only one time.

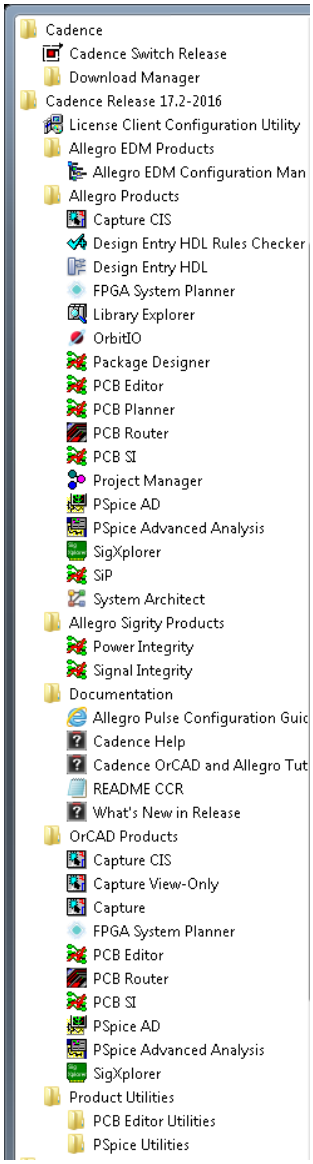
Note: The `AdminActions.bat` file located at `<installation_location>\tools\InstallUtils` can be used to configure the installation in the silent or unattended mode.

Note that the installation process will remain same for the standard-user mode except that a standard user cannot perform *all user* installation.

Changes in Start Menu

In 17.2-2016, you can quickly access the installed release from *Cadence Release 17.2-2016* of the Start menu. The installed products are organized under different categories for easier identification and access.

Cadence Switch Release and Download Manager are listed under *Start – Cadence*.



Diagnosing Installation Issues

Run the Allegro® Install Diagnose utility (`<installation_location>\tools\InstallUtils\InstallDiagnose`) to recognize, list, and repair issues with licensing and installation. The tool identifies and lists issues related to environment variables and runtime environments, redistributable packages, and other software packages depending on the tools installed. The tool also validates license server and client.

Repair Installation to Add Missing Files

Now, you can run the installer in repair mode to add any files or folders missing from the installed hierarchy.

Silent Installation Without Any Graphical Interface

The silent or unattended installation mode, that runs in the background without user intervention, now does not show any graphical interface.

Control File in Silent Installation

Now, you can specify a control file in the silent or unattended installation mode to select products for installation.

Incrementally Adding Products After Installing a HotFix

You can now incrementally add new products to an installation even after it has been updated with a HotFix. To add products after installing a HotFix, simply run the base release installer and select the new features to be added.

Note: This will roll back the installation to the base release version. Install the latest HotFix after adding new products.

Performance Improvement in HotFix Backup Feature

In 17.2-2016, there is a significant improvement in the performance of the feature to backup the files updated in HotFix installations.

Allegro PCB Editor

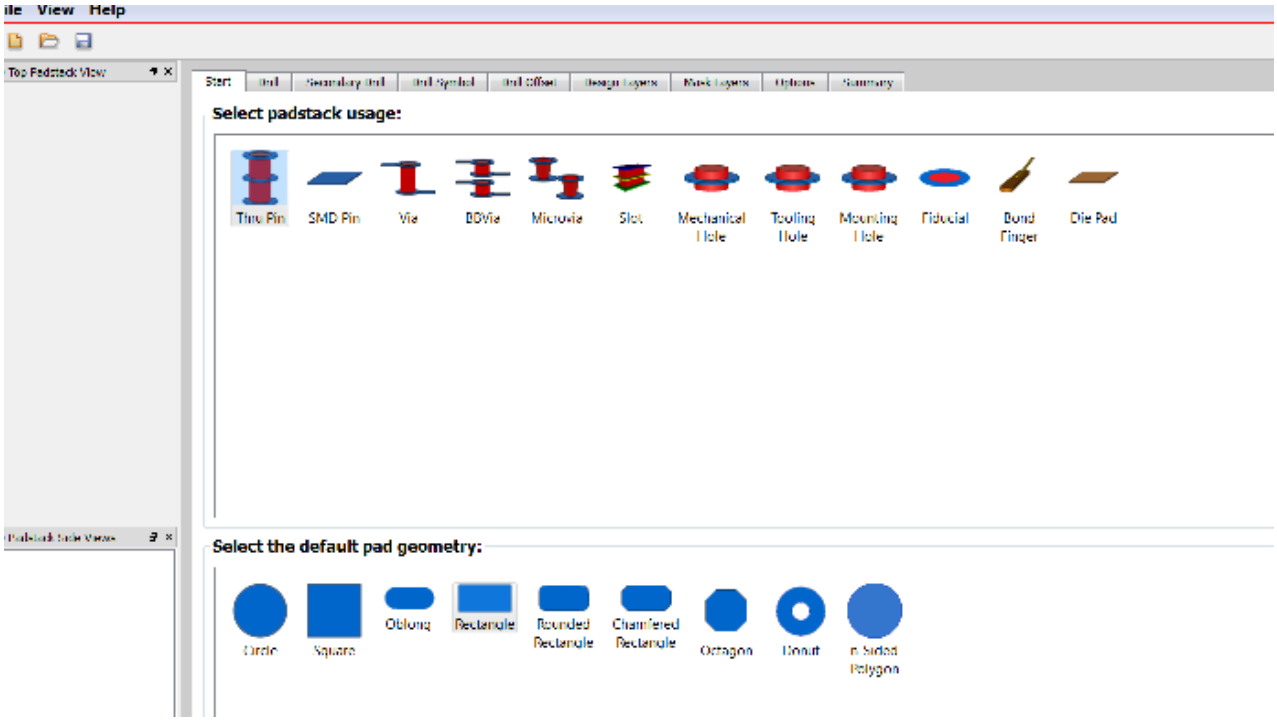
This document describes new features in the 17.2-2016 release of Allegro PCB Editor. Significant enhancements have been made in the following areas:

Padstack Overhaul

In release17.2-2016, a new Padstack Editor has been introduced to ease padstack creation through a new modern user interface. As part of this major effort, new geometries have been introduced to help minimize dependency on shape-based pads. Counter-bore/counter-sink definitions are now supported along with the ability to define both, the finished drill size, and actual drill tool. Keepouts are associated with the padstack with provision to extend beyond the begin/end layers of the pad.

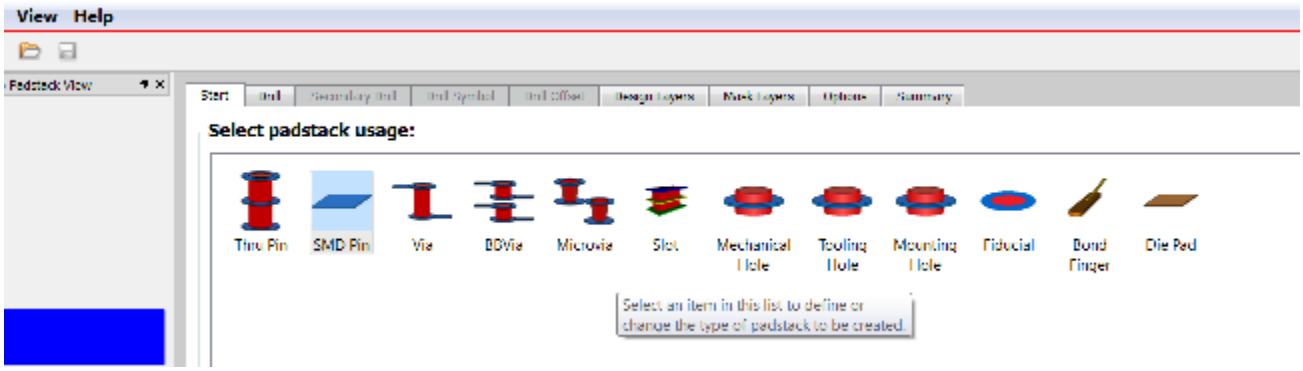
New Padstack Designer User Interface

Allegro Padstack Editor has been completely redesigned for 17.2-2016. The new user interface includes tabs for specific pad stack features. These tabs are structured left to right to promote a flow that guides the typical padstack creation process. These tabs are also smart-enabled based upon the padstack type to be created. For example, when a SMD Pin is selected as the padstack use type, the Secondary Drill Tab is disabled. When a Fiducial is selected, all drill tabs are disabled.



Padstack Usage Types

New attributes are assigned to padstacks based on the intended usage type. You can begin creation of a padstack by selecting the intended use type from the Pad Designer user interface, or from a *File – New* menu.



The padstack types include:

- Thru Pin
- SMD Pin
- Via
- BBVia
- Microvia
- Slot
- Mechanical Hole
- Tooling Hole
- Mounting Hole
- Fiducial
- Bond Finger
- Die Pad

The usage type attribute is used internally within Allegro and is also passed as labels to export formats such as IPC-2581. Padstack usage type does not restrict a pad from being used for another purpose.

New Pad Geometries

Four new standard pad geometries have been introduced in the Allegro PCB Editor 17.2 release. These standard pad geometries are driven by user request and are supported by the IPC-2581 pad figure standards.

Rounded Rectangle

The rounded rectangle requires a width and height similar to the rectangle pad geometry, with the addition of a corner radius that may be assigned for 1, 2, 3, or 4 corners. Only a single radius value can be defined, and at least one corner must have a radius for each rounded rectangle pad definition. Varying the radius and corner selection can result in a wide variety of geometric figures such as the samples shown in the following image.

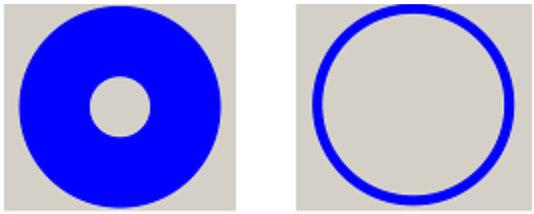
Chamfered Rectangle

The chamfered rectangle requires a width and height similar to rectangle pad geometry, with the addition of a chamfered corner value that may be assigned for 1, 2 3, or 4 corners. Only a single chamfered value can be defined, and at least one chamfered corner must be defined for each chamfered rectangle pad definition. Varying the chamfered value and corner selection can result in a wide variety of geometric figures as shown in the next figure.

Donut

The donut pad geometry is defined with an inner and outer diameter value. This pad geometry is intended for use in Fiducials and mounting holes where contact with a chassis ground may be required. This pad geometry uses a different connectivity model (touch vs.

connect point) from all other pad geometries. In order to use the touch model in the design level, the snap to connect point must be disabled.



n-sided Polygon

The n-sided polygon pad geometry is intended for use in Advance Packaging and related to vectoring of pad figures when exporting artwork data for manufacturing (stream data). The diameter (across points of the geometry) and the number of sides can be specified. The number of sides must be an even number with a minimum value of 6, but should not be greater than 64.

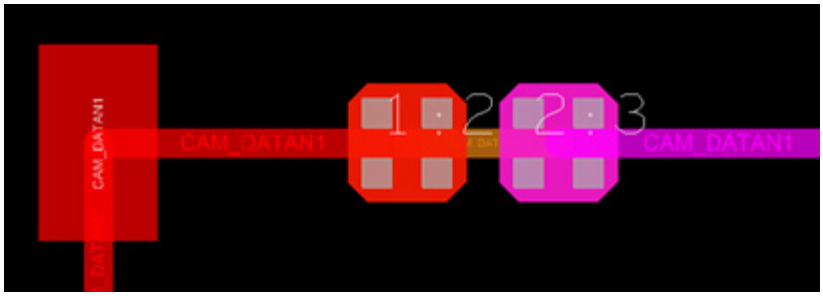
Note: There is a distinct difference between the Octagon pad figure and the n-sided (8) figure in the way the dimension size is calculated. The Octagon figure is measured across the flat surfaces of the geometry, whereas the n-sided figure is measured across the corners.

New Drill Features

The Allegro PCB Editor 17.2 release has added several drill features into the padstack definition.

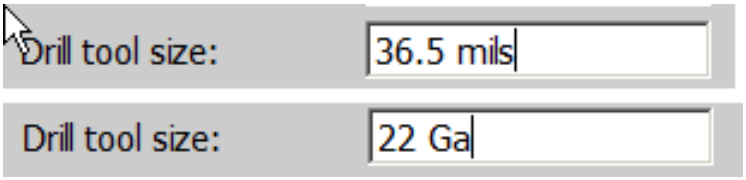
Hole Type

A new “Square hole” type is now supported, which is typically used for punch or microvia applications.



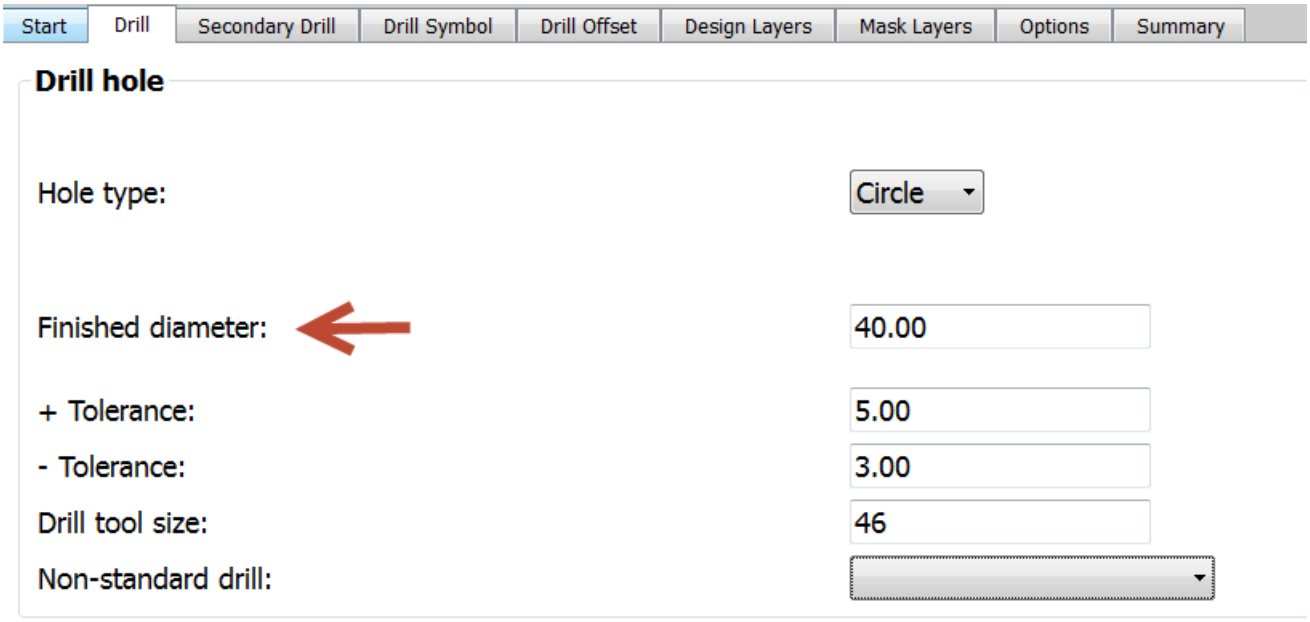
Drill tool size

This new field defines the actual drill size or tool identification to be used to drill the hole before plating. The drill size is often specified by press fit pin component manufacturers to ensure proper press fit pin to hole size. The field is a free-text field. The data entered into this field is only passed on to the drill legend, not the drill output formats such as *Excellon*. Values defined in this field are not altered by change in design units.



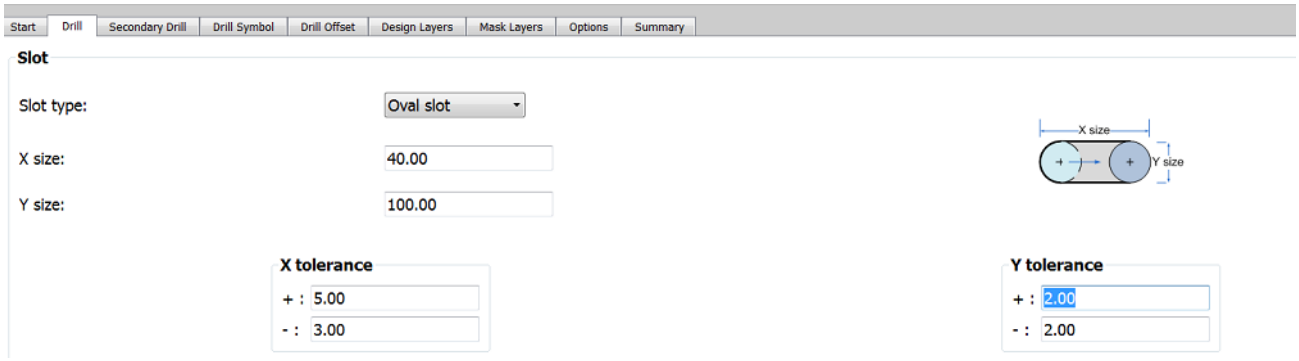
Finished diameter/Finished Size

The drill size definition used in the padstack definition in prior releases has been renamed to finished diameter for a circle drill, and finished size for a square drill. 16.x drill data has been migrated to the finished diameter field.



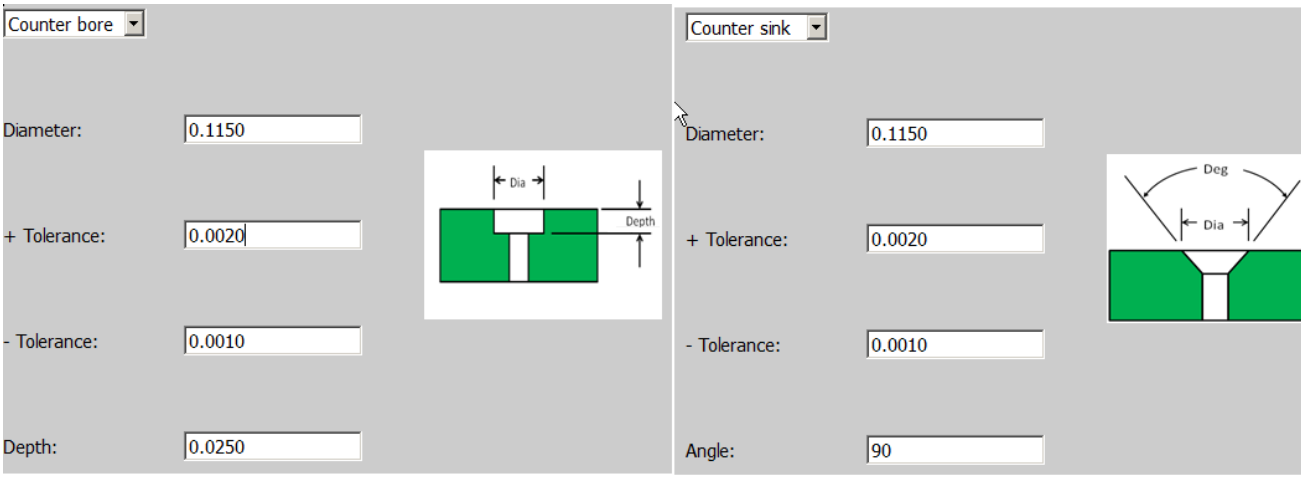
Slot tolerance

Slot tolerances are divided into two sets of values, X tolerance and Y tolerance. These tolerance pairs function independently of each other and are populated in the Drill Legend when used.



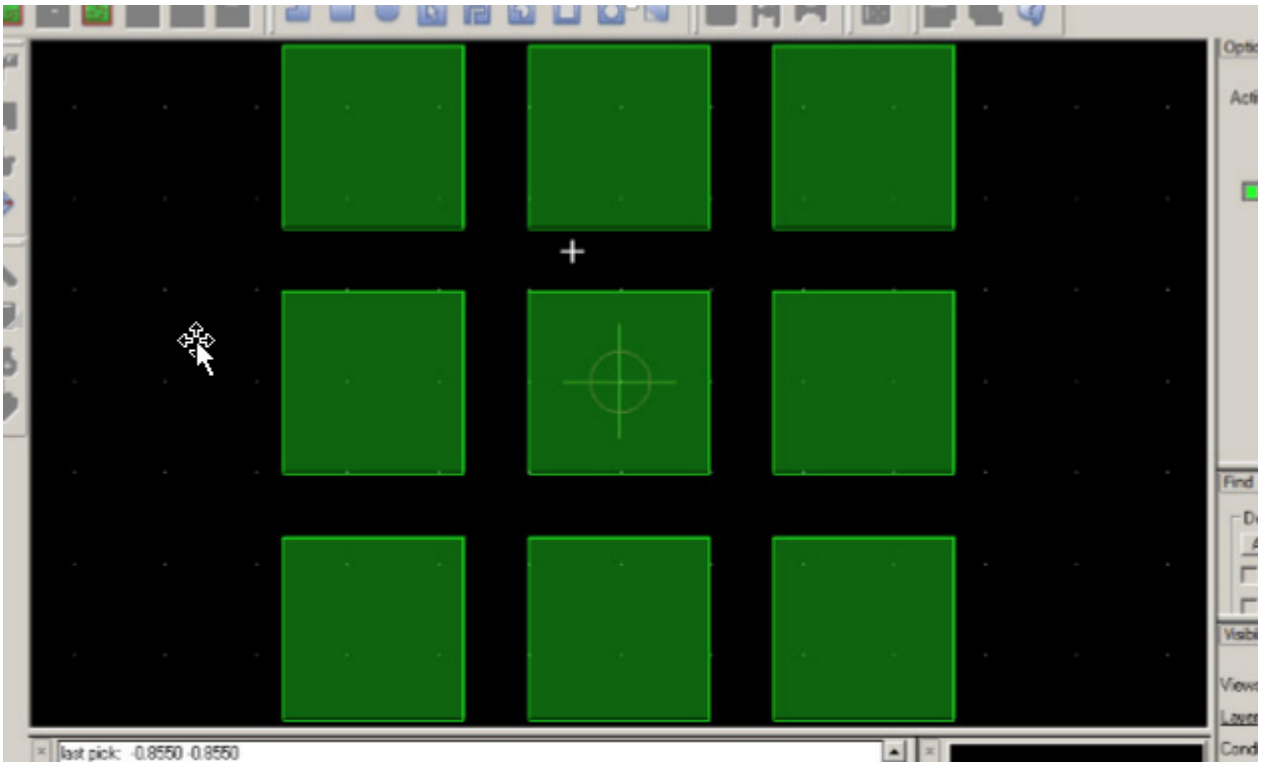
Secondary Drill

Two secondary drill options have been added to the padstack definition–Counter sink and Counter bore. Counter bore requires a counter bore diameter and depth, with optional counter bore plus and minus tolerance. Countersink requires a countersink diameter and countersink angle, with optional plus and minus tolerance.



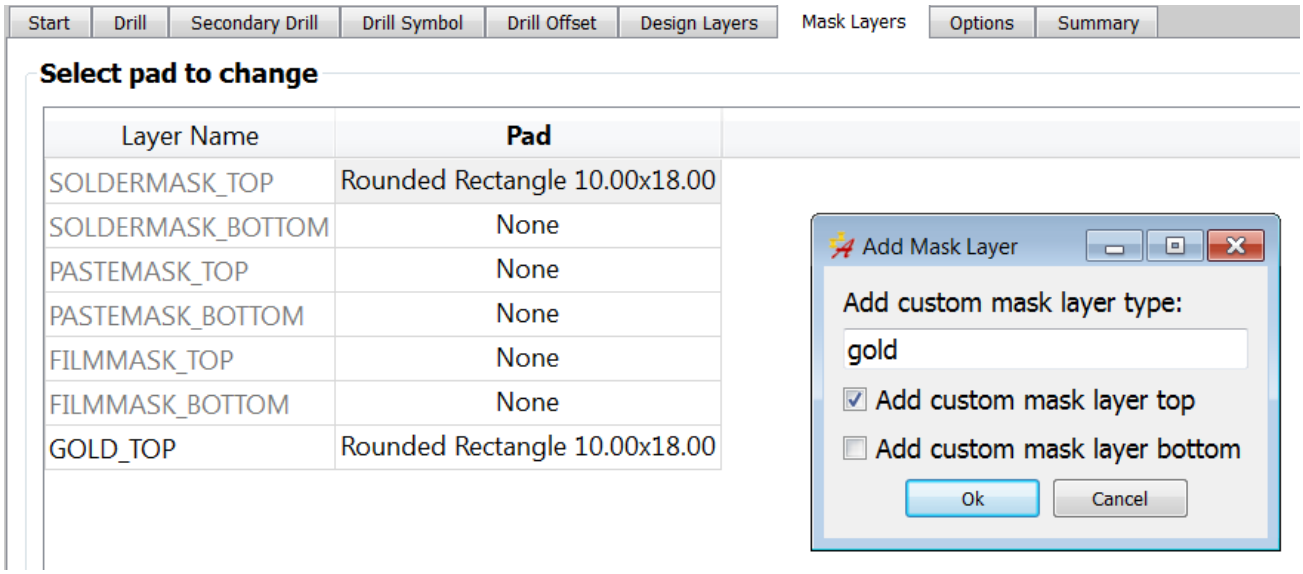
Multi-shape mask pad geometries

Multiple shapes can now be used for mask Layer definitions. The multi-shape mask scheme must be created as a flash symbols (`.fsm` file) and assigned in the mask pad layer definition. Window pane mask schemes are one example that can benefit from this enhancement.



User Mask Layers Increased to 32

The pad definition now supports a maximum of 32 user-defined mask layers; formerly, 16 were supported in version 16.6x. There is now UI support for adding the root name of the mask layer and options for the top and bottom layers.



Keepout Features

The 17.2 padstack provides support for route keepout geometry as part of its definition. These keepout objects can be controlled on each layer of the pad structure or on adjacent layers that can extend beyond the begin/end layers. When considering an adjacent layer keepout strategy, first define the geometry in the pad definition or instance then apply properties to pins or vias at the board level. The new properties are:

- Adjacent_layer_void_above
- Adjacent_layer_void_below

Usage examples range from SI to Manufacturing including voids under SMD pads to control Impedance and voids associated with Buried/Blind Vias. The maximum property value is 8 (layers) and are applied to consecutive layers. All pad figures, with the exception of Donut Pad may be used to define the keepout figure.

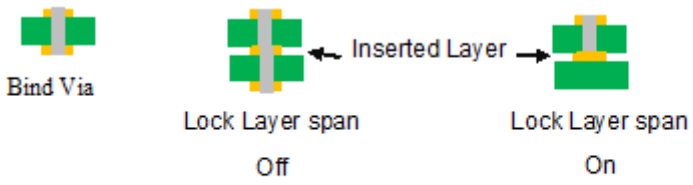
For same layer route keepouts, typically used in mounting holes or laser drilled skip vias, it is required that regular pad be defined for that layer. If no regular pad exists for a pad layer defined with the same layer route keepout, the route keepout will not be applied.

Layer Name	Regular Pad	Thermal Pad	Anti Pad	**Keep Out**
BEGIN LAYER	Circle 0.6250	None	None	None
DEFAULT INTERNAL	Circle 0.0500	None	None	Circle 0.6500
END LAYER	Circle 0.6250	None	None	None
ADJACENT LAYER	-	-	-	None

Padstack Options

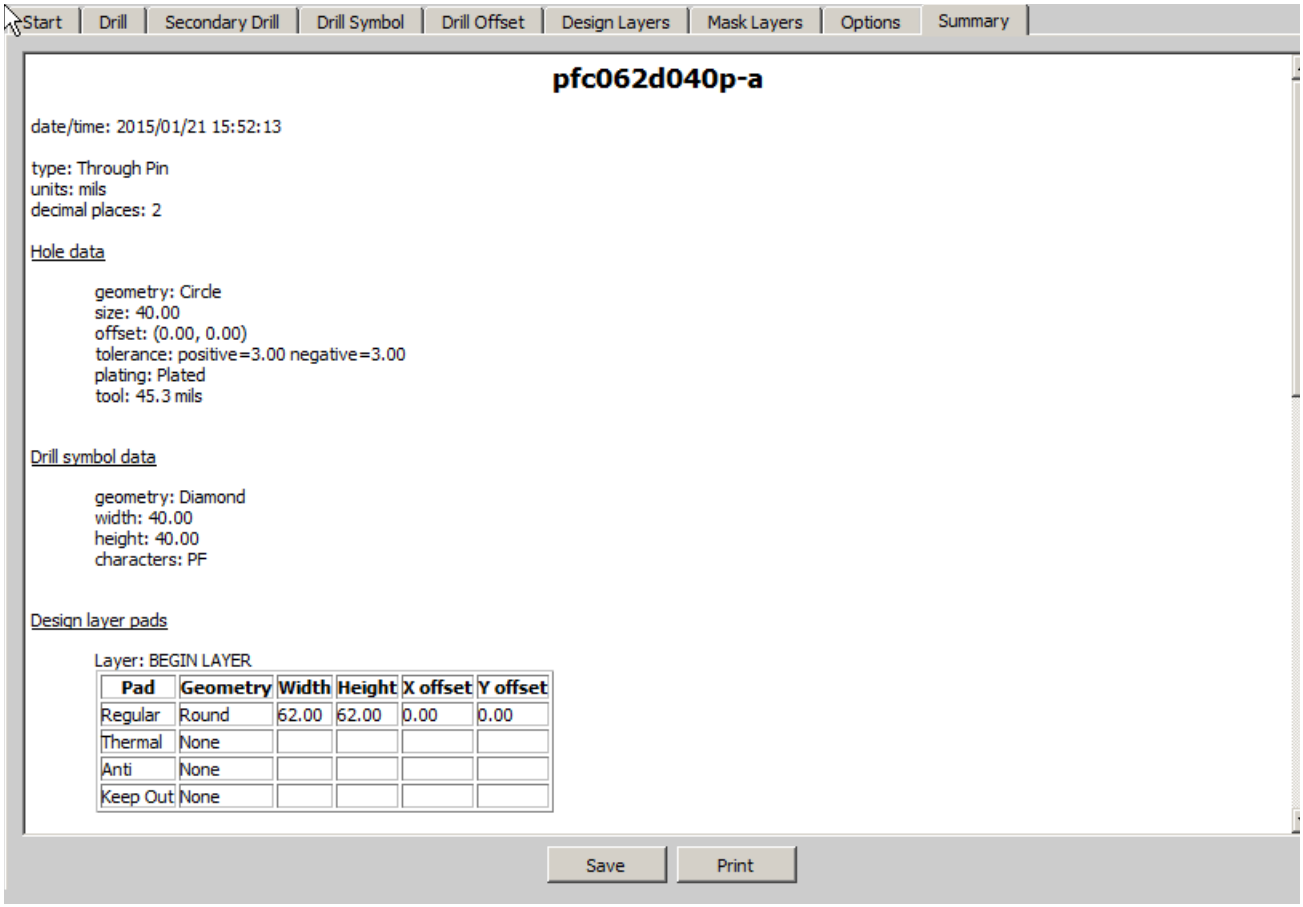
Two padstack options exist in the 17.2 Pad Designer tool.

- Suppress unconnected internal pad (required for legacy artwork) - This option maintains support for removing unused internal padstacks supported in prior releases.
- Lock Layer Span - This option prevents the layer expansion for bbvias when a new signal/plane layer is inserted. For example, a bbvia exists in a design that starts at layer_4 and ends on layer_5. A new layer (Layer_4A) is inserted between layer_4 and layer_5. The existing via still starts on layer_4, but now ends on the newly inserted Layer_4A.



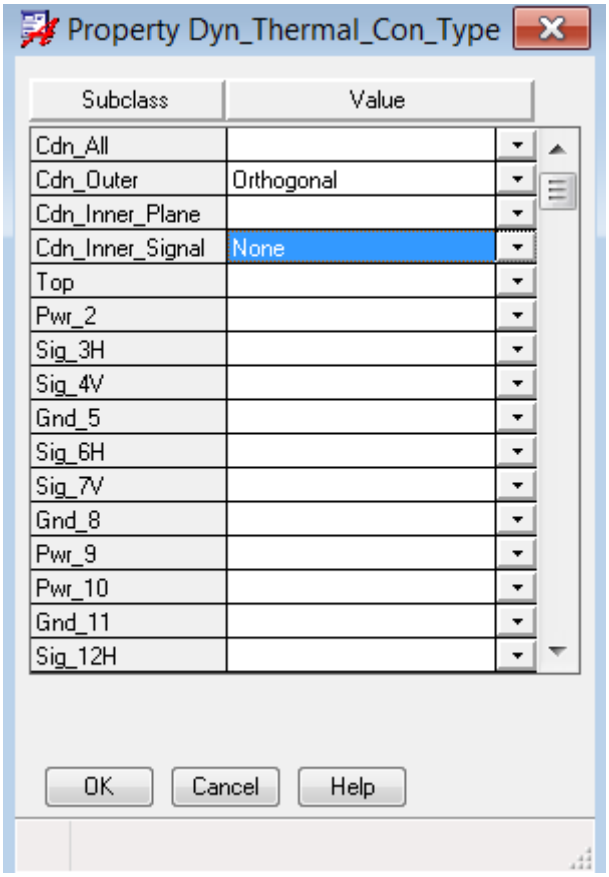
Summary Report

The summary tab displays the values, definitions, and options for the current padstack. This summary can be saved to a file in HTML format, or can be printed.



Layer support for Dynamic Shape Properties

The thermal and clearance properties associated with Dynamic Shapes can now be applied on a per-layer basis. These properties offer customization controls in the form of thermal spoke width and quantity, connection type and clearance size. Similar to the use model for creating Constraint Regions, you have the option of applying properties hierarchically; this includes Outer Layers, Inner Plane, and Inner Signal as well as individual layers.



The suite of properties supporting array entry includes:

- Dyn_clearance_oversize_array
- Dyn_clearance_type
- Dyn_fixed_therm_width_array
- Dyn_max_thermal_conns
- Dyn_min_thermal_conns
- Dyn_oversize_therm_width_array

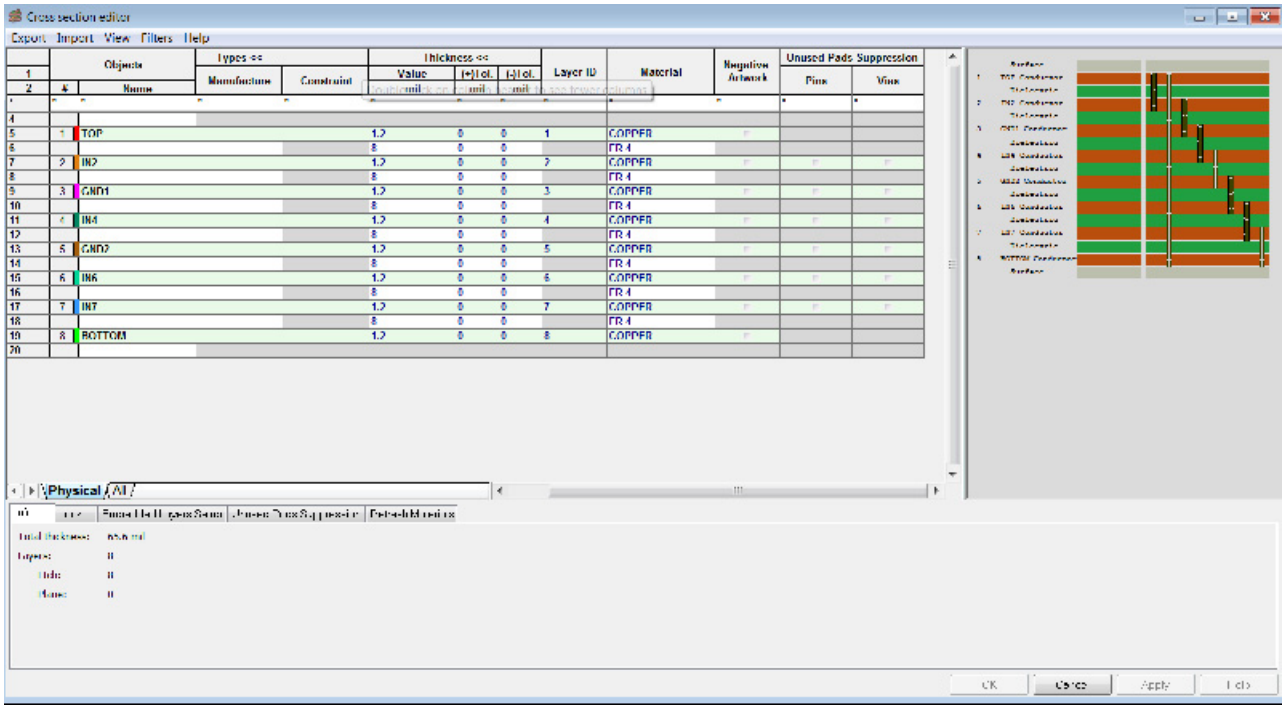
- Dyn_thermal_best_fit
- Dyn_thermal_con_type

Note: Three of the properties support elements other than Pins or Vias. The array extension has been added to those properties with this conflict. For example, apply Dyn_clearance_type to a cline; apply Dyn_clearance_oversize_array to a Pin.

Cross Section Overhaul

The Cross Section Editor has been redesigned leveraging the underlying spreadsheet technology found in Constraint Manager. It offers one-stop shopping for features that require the cross section for their setup; dynamic unused pad suppression and embedded component design for example. A graphical image of the stackup construct is available in a dock-able window. The stackup image includes functionality to reverse drill direction. Grid editing enhancements include functions to add layer pairs or a user-defined number of layers. Miscellaneous enhancements include the increase of material character length from 19 to 250, positive/negative tolerance support for each layer, via label customization, controls to prevent editing of layers or values and support of unnamed Dielectric layers above top/below bottom.

The default view combines the spreadsheet grid with the stackup viewer. The drill display within the viewer is based on actual padstack usage in the database. Vias in Physical CSets that are unused do not contribute to the display.



Physical/All Tabs

Select *Physical* for a reduced view of the cross section spreadsheet. Supported columns are those typically used for physical design that include Objects, Layer Types, Thickness and Tolerances, Physical, Layer ID, Material name, Negative Artwork and Unused Pad Suppression.

Select *All* to include all those listed for Physical in addition to Signal Integrity and Embedded Component Design.

Functional Tabs

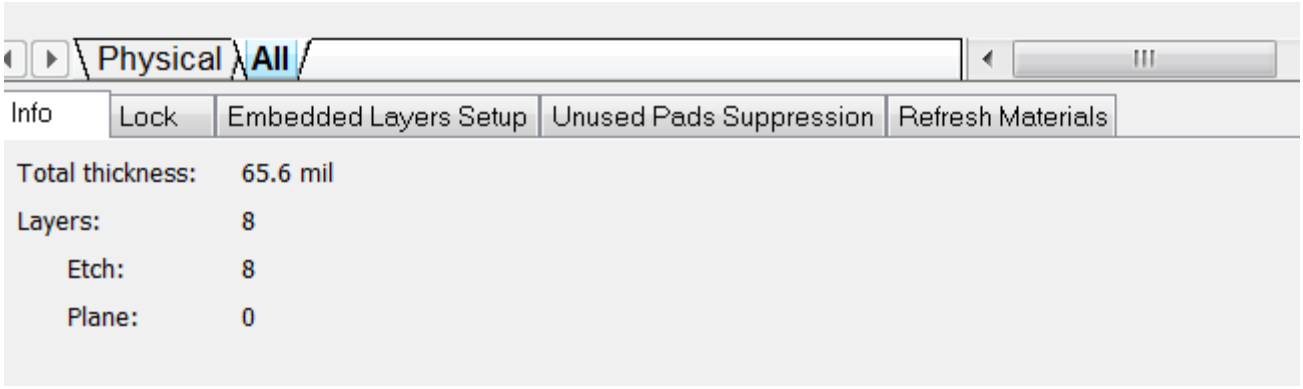
There are five functional tabs located at the bottom of the spreadsheet.

- *Info*: displays total thickness and number of layers (Etch + Plane)
- *Lock*: prevents editing within the spreadsheet in terms of adding layers or changing values

- *Embedded Layers Setup*: setup form for Embedded Component Design. Formerly located in *Setup – Embedded Component Setup*.

Note: This tab is available only with the *Miniaturization* product option.

- *Unused Pads Suppression*: setup form for Unused Pad Suppression. Formerly located in Setup – Unused Pads Suppression.
- *Refresh Materials:* use to refresh parameters from the `materials.dat` file.



General Enhancements to Cross Section Editor

Layer Types

- *Manufacture:* Assign hierarchical names to signal and plane layers. For example, INNER_SIGNAL, PLANE. This information is supported in the IPC2581 data schema.
- *Constraint*: Assign hierarchical names to signal and plane layers similar to the *Manufacture* column. However, their names are integrated into Spacing CSet structures and provide the opportunity to manage CSets hierarchically.

Tolerances

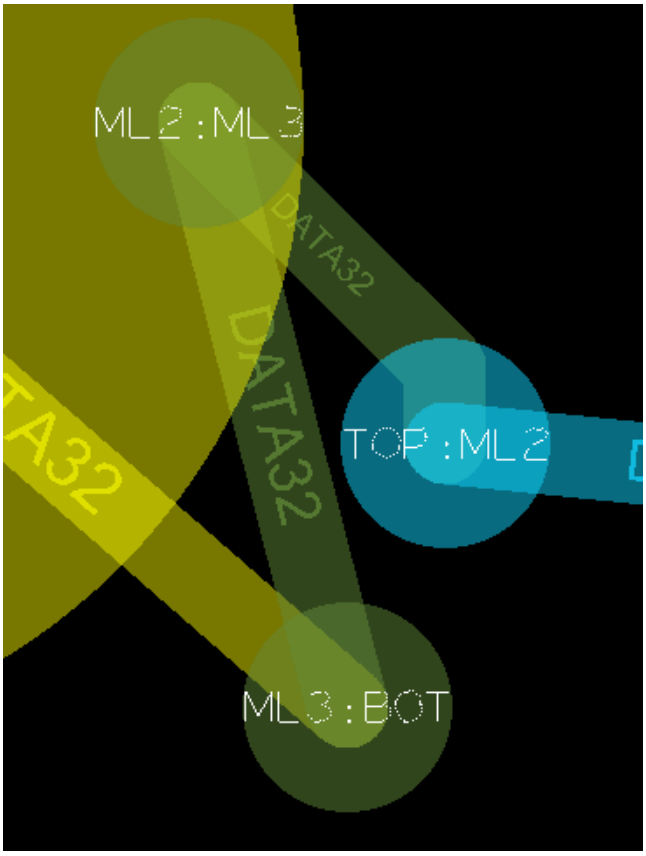
Positive and negative tolerance fields are now supported. The Materials Editor has also been updated to align with this change to the Cross Section Editor.

Materials

The character limit has been increased from 19 to 250.

Layer ID

Use to customize buried and blind via labels. Up to 3 alpha-numeric characters are supported.

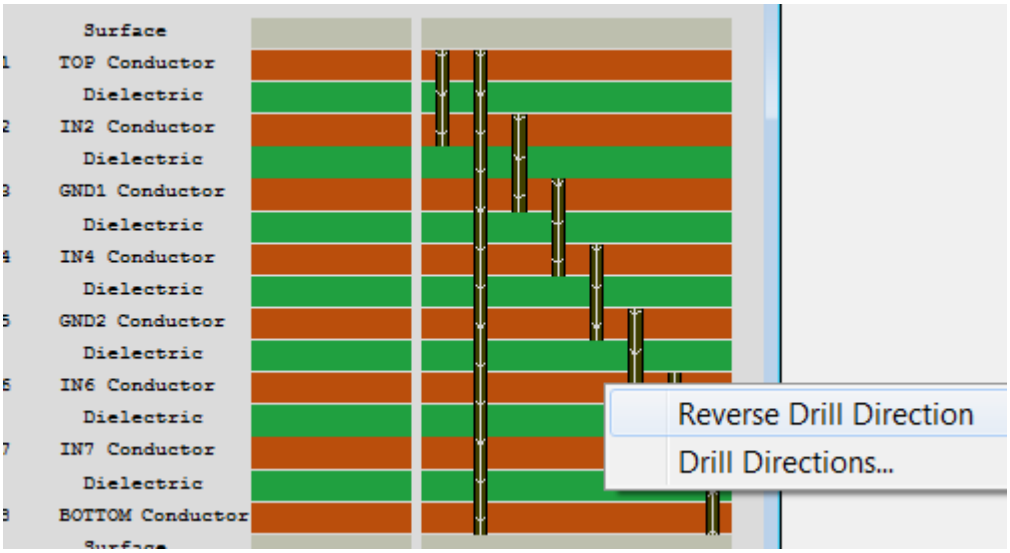


Support for Layers above top/below bottom

This is limited to unnamed dielectric layers.

Reverse Drill Direction

Hover over a drill bitmap to reverse the direction of Buried/Blind/Microvias. The reversal only impacts the ordering of layers used in the NC Drill Legend Chart.

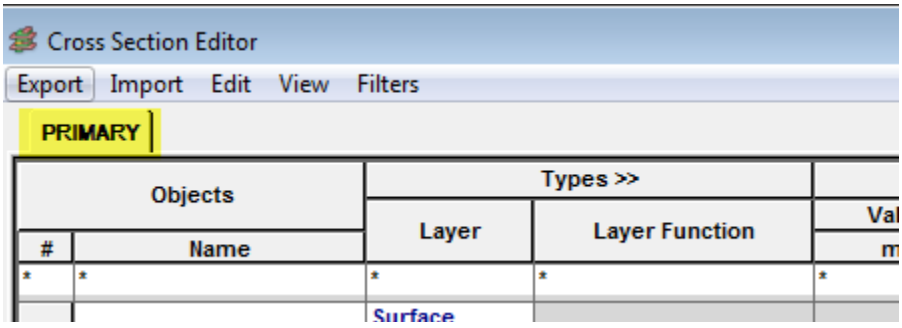


Multi-Cross Section Support for Rigid-Flex Design

Note: Requires *Allegro PCB Designer* and *OrCAD Professional* licenses.

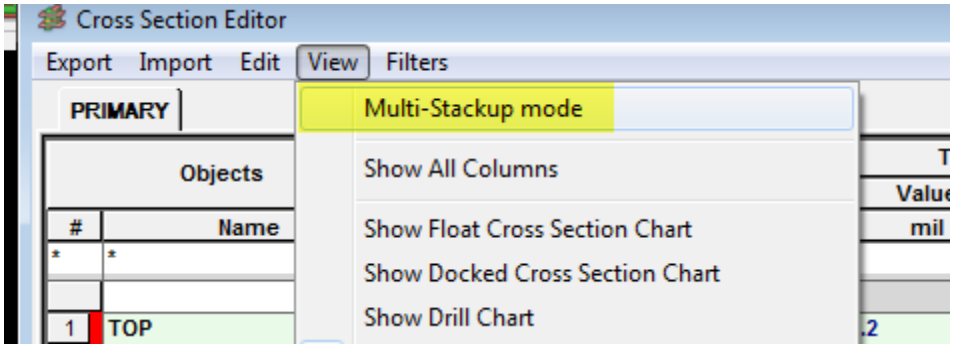
The Cross Section Editor has been enhanced to support multiple stackups, each capable of supporting conductor and non-conductor layers such as Soldermask and Coverlay. The Cross Section Editor provides total thicknesses for each stackup in terms of accumulated conductor layers as well as an option with mask layer thicknesses included.

When launched for the first time, the editor appears with only one tab, Primary, and the default stackup is shown in the Primary tab.



Enabling Multiple Stackups

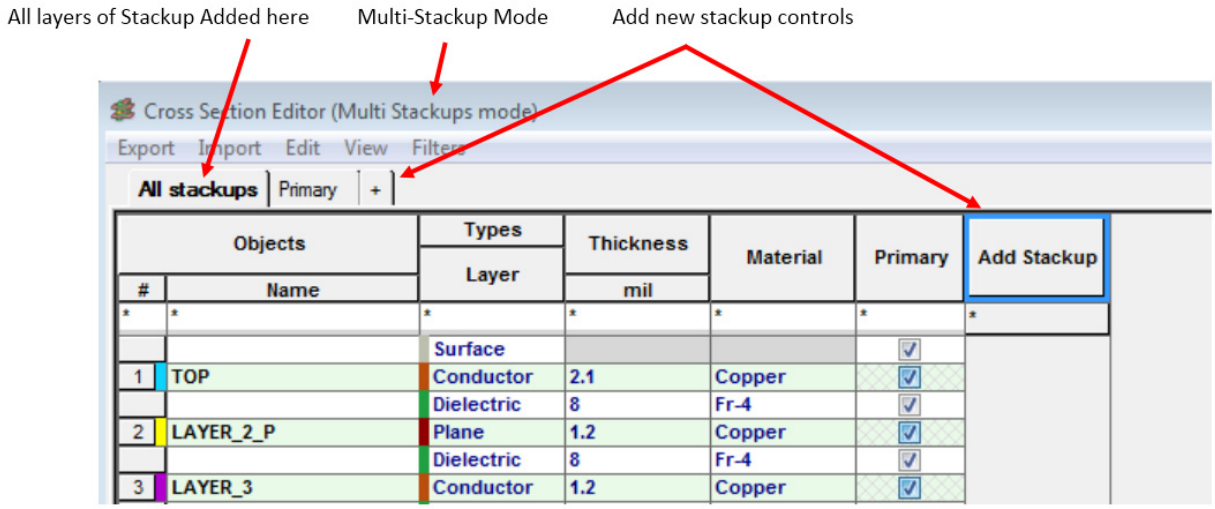
To add multiple stackups, enable the multi-stackup mode by choosing *View – Multi-Stackup mode*.



Note the following in the Multi-Stackup mode:

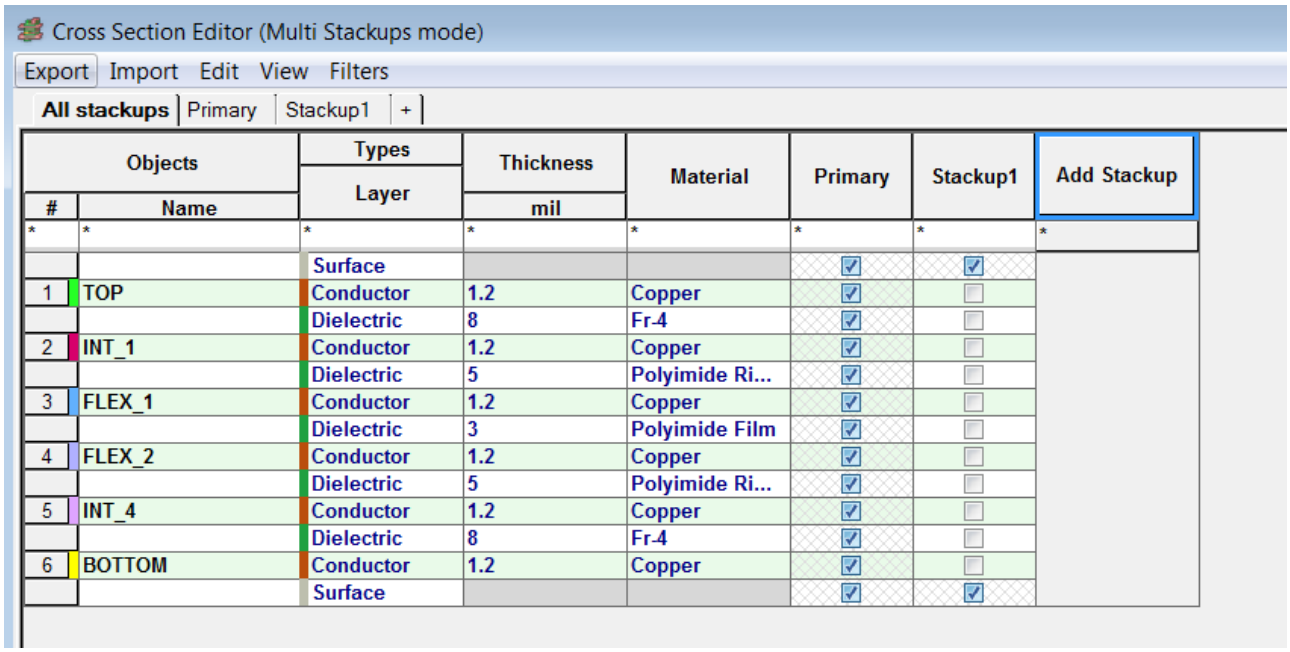
- All stackups tab – Location of all conductor and non-conductor layers comprising the portfolio of stackups
- Primary tab – The default stackup that contains all conductor layers, such as conductor and planes. It is used for non-zone applications and is also used to represent the area outside the design outline for place/quickplace applications to run.
- Controls to add new stackup – There are two methods to add a new stackup:
  - Click + on top banner

- Click *Add Stackup* cell to the right of Primary



Adding a New Stackup

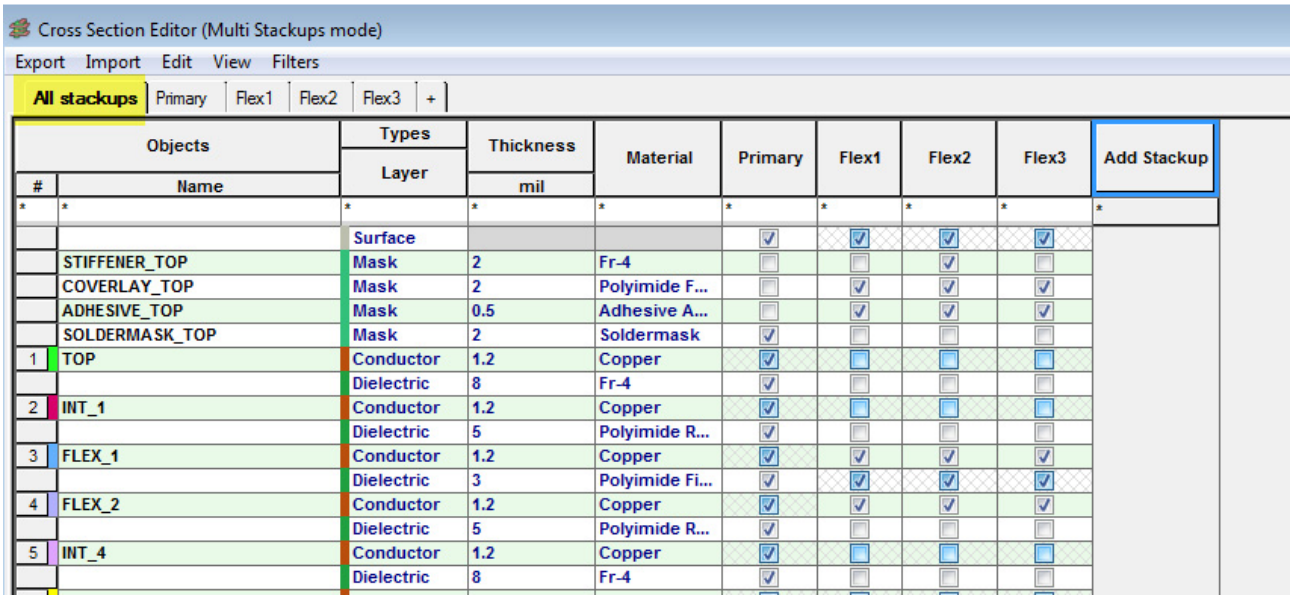
The initial stackup name is seeded to “STACKUP1” but it can be renamed within the “Create Stackup” UI or within the stackup grid.



Configuring Layers in Stackup

Each stackup supports check boxes to control the layer intent of that respective stackup.

- Primary Stackup – Since this stackup represents the largest number of conductor layers and is considered the “default” stackup, only non-conductor layers can be toggled on or off. If a conductor layer must be deleted, click the All Stackups tab and delete the entry in that column.
- Rigid-Flex Designs - the Primary stackup is most likely the Rigid stackup consisting of the most conductor layers. Additional stackups are created to support flex sections or lower count rigid sections. These additional stackups are mapped to physical zones. It may not be necessary to create a physical zone for the section regarded as Primary.
- Material Inlay - the Primary stackup is most likely the main section of the PCB. Physical zones are created for the inlay sections utilizing different materials for RF/Analog.



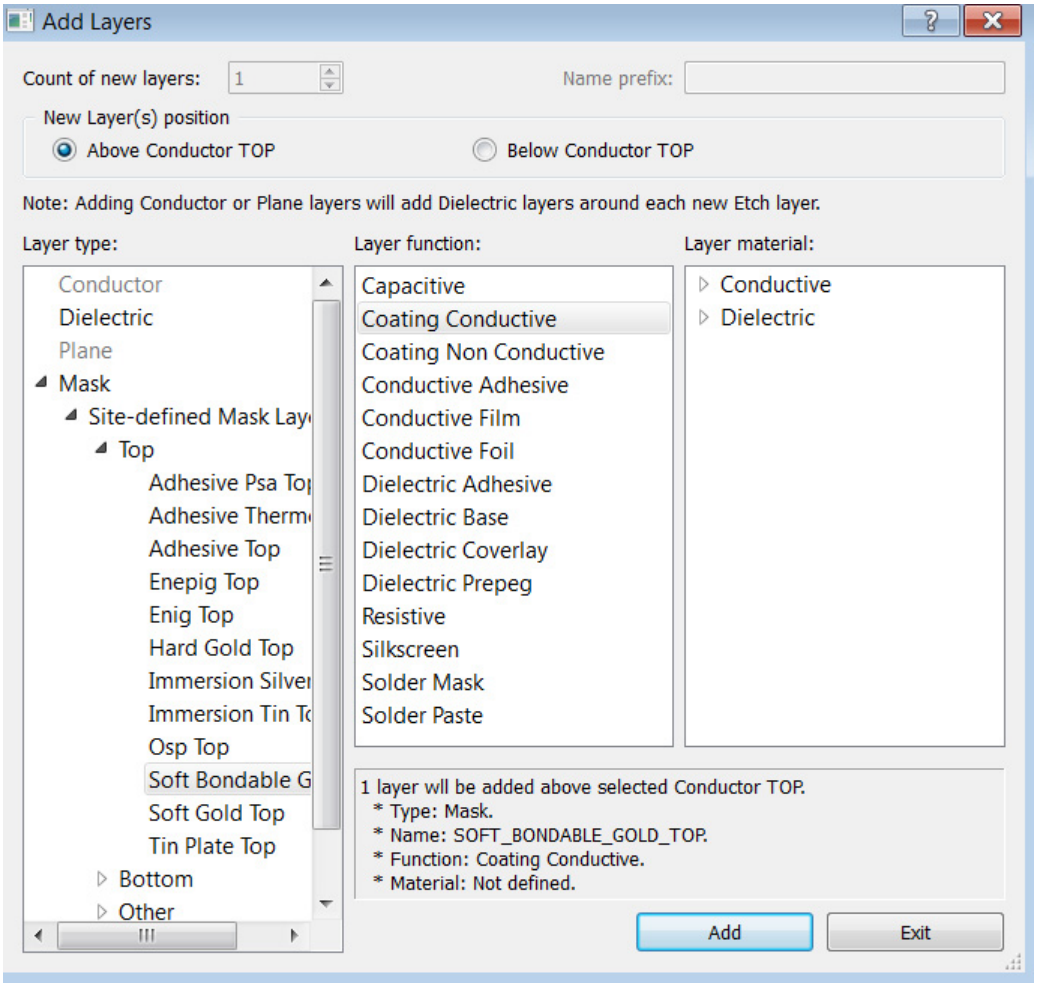
Objects		Types	Thickness	Material	Primary	Flex1	Flex2	Flex3	Add Stackup
#	Name	Layer	mil						
*	*	*	*	*	*	*	*	*	*
		Surface			☑	☑	☑	☑	
	STIFFENER_TOP	Mask	2	Fr-4	☐	☐	☑	☐	
	COVERLAY_TOP	Mask	2	Polyimide F...	☐	☑	☑	☑	
	ADHESIVE_TOP	Mask	0.5	Adhesive A...	☐	☑	☑	☑	
	SOLDERMASK_TOP	Mask	2	Soldermask	☑	☐	☐	☐	
1	TOP	Conductor	1.2	Copper	☑	☐	☐	☐	
		Dielectric	8	Fr-4	☑	☐	☐	☐	
2	INT_1	Conductor	1.2	Copper	☑	☐	☐	☐	
		Dielectric	5	Polyimide R...	☑	☐	☐	☐	
3	FLEX_1	Conductor	1.2	Copper	☑	☑	☑	☑	
		Dielectric	3	Polyimide Fi...	☑	☑	☑	☑	
4	FLEX_2	Conductor	1.2	Copper	☑	☑	☑	☑	
		Dielectric	5	Polyimide R...	☑	☐	☐	☐	
5	INT_4	Conductor	1.2	Copper	☑	☐	☐	☐	
		Dielectric	8	Fr-4	☑	☐	☐	☐	

Cross Section Support for Non-Conductor Layers

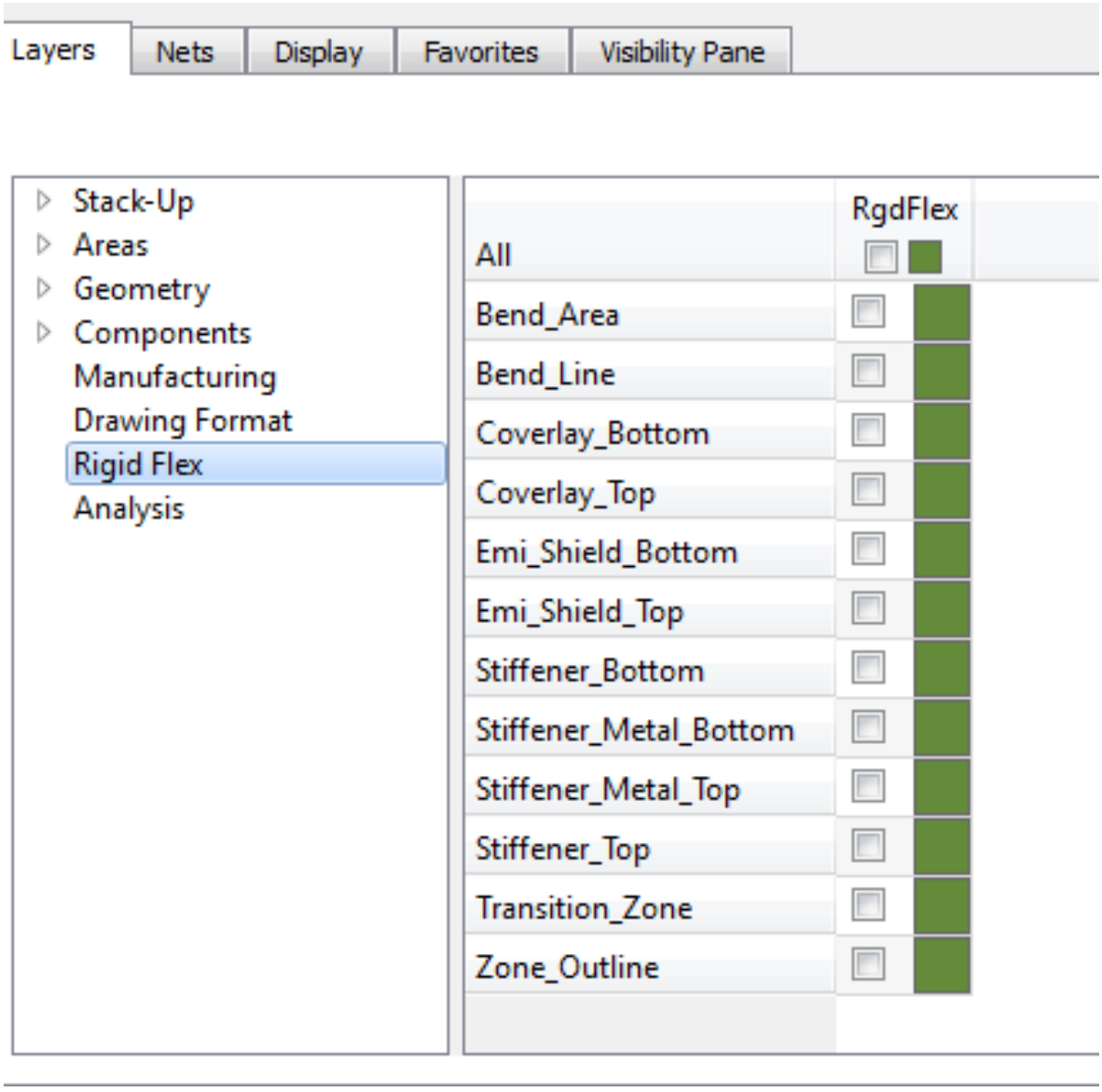
The Cross Section Editor now supports the entry of non-conductor layers; typically mask and coating layers used in rigid, flex or rigid-flex applications. These layers are usually added above the top or below the bottom surfaces but can also be added within the core stackup to accommodate multiple independent flex laminates.

Note: The PCB Editor Database represents non-conductor layers as Mask or Dielectric although they may serve different purposes like coating, shield or plating areas.

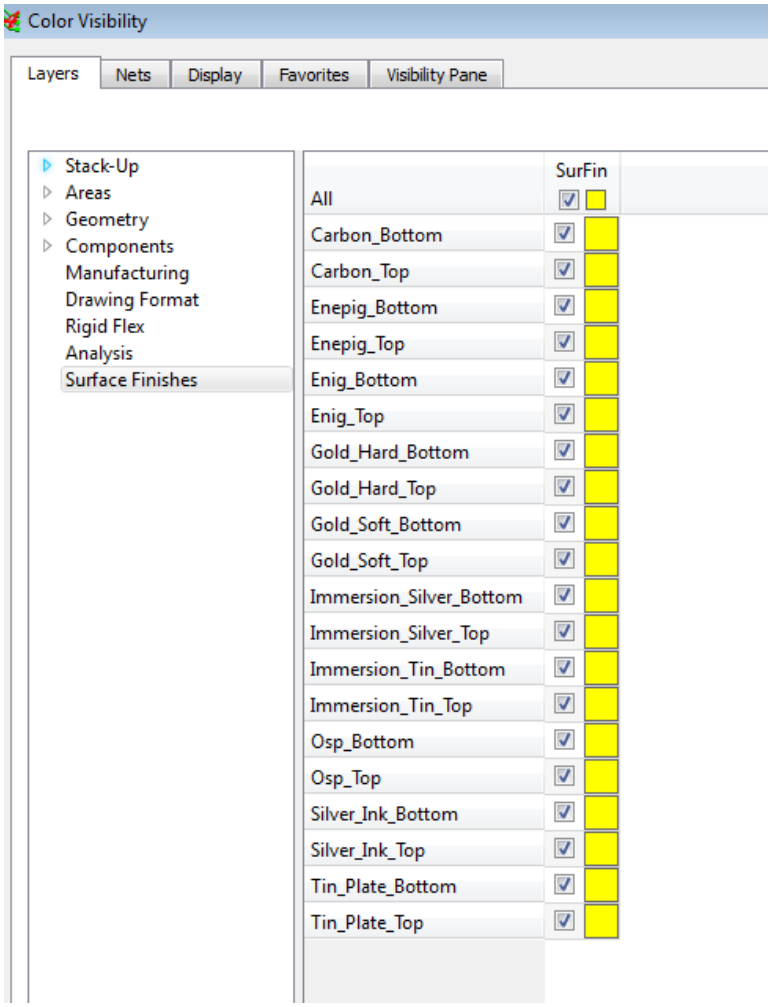
- Adding Mask Layers - To add a mask layer above top, select the top cell in the Cross Section grid, then right-click and select Add Layers command.
- Candidate layers fall into the database category of Mask or Dielectric. Dielectric layers can be named or unnamed. If named, they take on the properties of a conductor layer. In most cases, you will select the Mask category then decide if the layer is sourced from the design database or from the user-defined mask layer site file.
- The site file is named `masklayersitefile.xml` and is controlled by the *materialpath* variable.



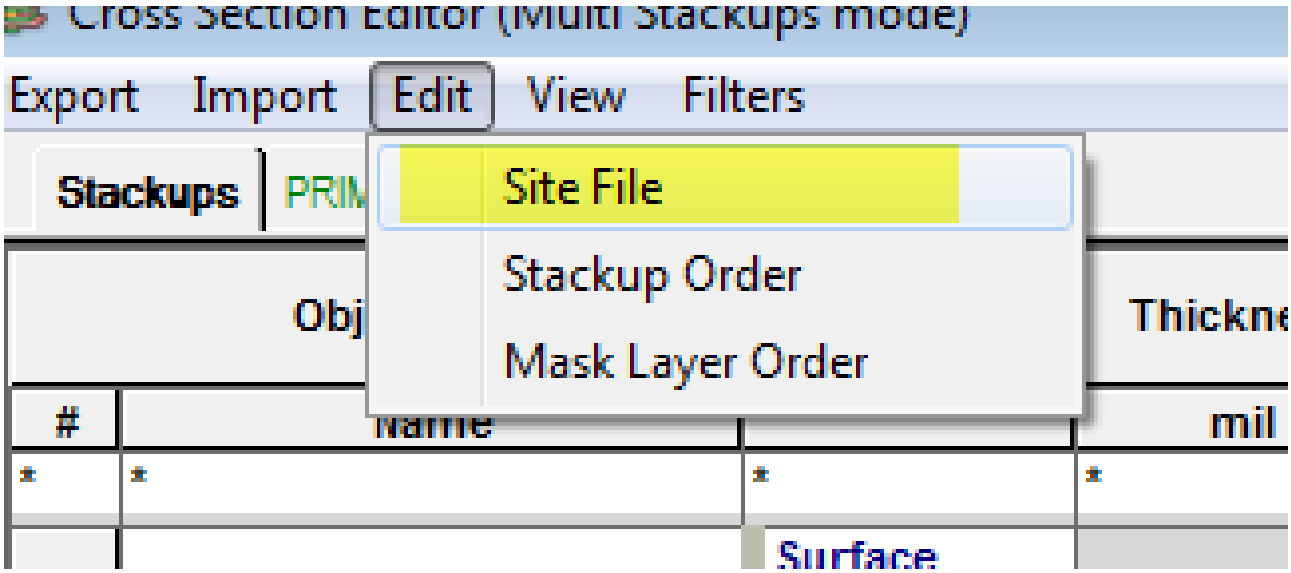
- Database-sourced layer names can be user-defined; typical use model for pre-17.2 designs or from the new Classes (Rigid-Flex and Surface Finishes)
- The new Rigid-Flex Class supports the following subclasses:


Layers
Nets
Display
Favorites
Visibility Pane
Stack-Up
Areas
Geometry
Components
Manufacturing
Drawing Format
Rigid Flex
Analysis
All
RgdFlex
Bend_Area
Bend_Line
Coverlay_Bottom
Coverlay_Top
Emi_Shield_Bottom
Emi_Shield_Top
Stiffener_Bottom
Stiffener_Metal_Bottom
Stiffener_Metal_Top
Stiffener_Top
Transition_Zone
Zone_Outline

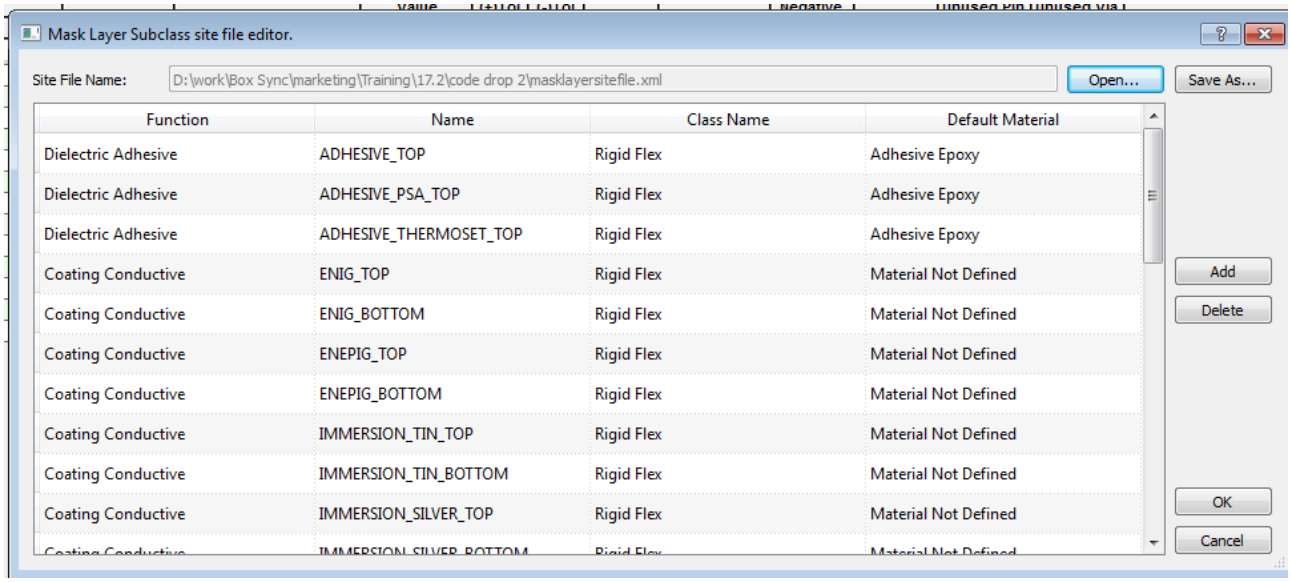
- The new Surface Finishes Class supports the following subclasses:



- The site file can be opened from the *Edit – Site File* command in the Cross Section Editor.



- The Mask Layer Subclass Site file should be considered a library element and stored adjacent to the materials.dat file since both files are sourced from the *materialpath* variable.



Rigid-Flex Physical Zone Management

Note: Requires Allegro PCB Designer or OrCAD Professional.

A physical zone is used to map that respective area of the design to one of the stackups created in the Cross Section Editor. Zones can be rigid or flex areas consistent of varying layers. Rigid zones for example might be comprised of 10 conductor layers and soldermask whereas a flex zone may contain 2 conductor layers plus several mask layers such as coverlay, adhesive or stiffeners.

Class:Rigid-Flex

- Bend_Area
- Bend_Line
- Coverlay_Bottom
- Coverlay_Top
- Emi_Shield_Bottom
- Emi_Shield_Top
- Stiffener_Metal_Bottom
- Stiffener_Metal_Top
- Stiffener_Bottom
- Stiffener_Top
- Transition_Zone
- Zone_Outline

Class: Surface Finishes

- Carbon_Bottom
- Carbon_Top
- Enepig_Bottom
- Enepig_Top
- Enig_Bottom
- Enig_Top
- Gold_Hard_Bottom
- Gold_Hard_Top
- Gold_Soft_Bottom
- Gold_Soft_Top
- Immersion_Silver_Bottom
- Immersion_Silver_Top
- Osp_Bottom
- Osp_Top
- Silver_Ink_Bottom
- Silver_Ink_Top
- Tin_Plate_Bottom
- Tin_Plate_Top

Zones automatically include associated keepouts and optional constraint regions and rooms. Any part of the board that is outside of any zone will use the Primary Stack-up for its layer cross-section. The Zone Editor will only use the Design_Outline class when defining zone boundaries that follow the board outline. It will not be able to use Board_Geometry/Outline, since that subclass allows arbitrary lines and graphics that do not form a legal boundary.

New Database Classes and Subclasses

Rigid Flex and Surface Finish Classes

Two new classes have been introduced: Rigid Flex and Surface Finishes. The new subclass provides better identification of subclass groups used for specific purposes. These classes are also recognized by other functions within the database, such as stack-up, as classes with special use cases and applications.

- Rigid Flex
  - Zones
    - Stack-up zones
    - Transition zones
  - Contains common subclasses for flex and rigid flex technology
    - Masks
    - Adhesives
    - Bend geometry
  - Additional user-defined subclasses may be added
  - Mask layers may be recognized by stackup
  - Layer types can be linked through the mask layer site file
- Surface Finishes
  - Represents the different materials and masks used for standard PCBs as well as rigid, and rigid-flex designs
    - Precious metals plating
    - OSP
  - Additional user-defined subclasses may be added
  - Metal mask layers may be recognized by Stack-up but there is no DRC checking for connectivity.
  - Layer types can be linked through the mask layer site file

The PCB Editor database now natively supports the following new class structures to support not only rigid-flex design, but standard rigid as well. The structured list of new class/ subclasses include:

Class:Rigid-Flex

- Bend_Area
- Bend_Line
- Coverlay_Bottom
- Coverlay_Top
- Emi_Shield_Bottom
- Emi_Shield_Top
- Stiffener_Metal_Bottom
- Stiffener_Metal_Top
- Stiffener_Bottom
- Stiffener_Top
- Transition_Zone
- Zone_Outline

Class: Surface Finishes

- Carbon_Bottom
- Carbon_Top
- Enepig_Bottom
- Enepig_Top
- Enig_Bottom
- Enig_Top
- Gold_Hard_Bottom
- Gold_Hard_Top
- Gold_Soft_Bottom
- Gold_Soft_Top
- Immersion_Silver_Bottom
- Immersion_Silver_Top
- Osp_Bottom
- Osp_Top
- Silver_Ink_Bottom
- Silver_Ink_Top
- Tin_Plate_Bottom
- Tin_Plate_Top

Design_Outline and CUTOUTS subclasses

The BOARD GEOMETRY class has had two new subclasses added, DESIGN_OUTLINE and CUTOUT. These new subclasses provide greater capabilities to leverage the board outline in various ways.

- Enhanced DRC capabilities – Object to board outline checks
  - pad to board edge

- mask to cutout and/or board edge
- cutout to board edge

- Rigid-flex support – Zone creation
  - trimming of zone edges to DESIGN_OULTINE edge
- ECAD/MCAD collaboration
  - Independent management of board outline and cutouts
  - Eliminates determining what is an outline and/or cutout from other objects
  - Enhanced STEP Export of outline and cutouts
- Manufacturing
  - Eliminates determining what is an outline and/or cutout from other objects

The new DESIGN_OUTLINE subclass is a shape that defines the outline of the PCB, flex, or rigid flex. The OUTLINE subclass may still be used to define the outline as there is no requirement for the outline to be a closed polygon, though it has always been preferred.

Both, IDX and IDF interfaces, will recognize and adopt the use of the new DESIGN_OUTLINE and CUTOUT subclasses. When importing IDF or IDX, the board outline geometry will be mapped to the DESIGN_OUTLINE subclass. Cutouts will be mapped to the OUTLINE subclass.

IDF Export will first check for the existence of geometry on the DESIGN_OUTLINE and CUTOUT subclasses and use that data to export board outline data. If there is no geometry on the DESIGN_OUTLINE subclass, the OUTLINE subclass will be used.

IDX_Out and IPC-2581-Out will fail if no Design Outline is present.

Create Artwork will prompt you with a warning if an outline is present in the film records.

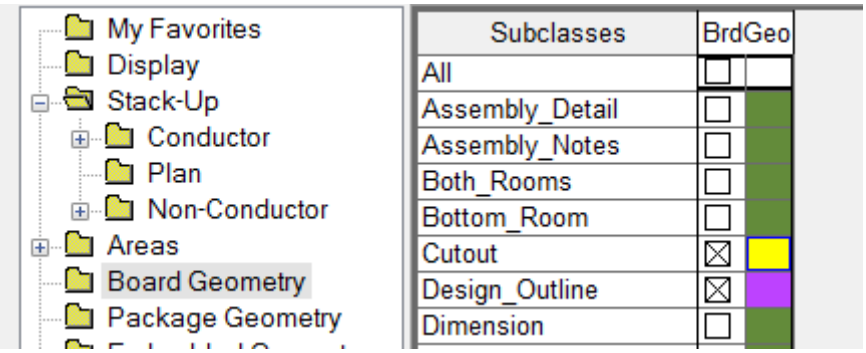
Design Uprev

Board files in SPB16.6 contain the board outline and cutout data on the Board Geometry OUTLINE Subclass. When moving the design to the 17.2 release, these geometries get copied to the new DESIGN_OUTLINE and CUTOUT subclasses.

Limitations:

- Only one DESIGN_OUTLINE geometry can exist in a drawing database.

- When converting OUTLINE to DESIGN_OUTLINE, the OUTLINE geometry must be able to be converted into a shape. Gaps, overlaps and crossing geometries will fail to convert.
- OUTLINE geometry inside of the board outline is copied to the CUTOUT subclass
- OUTLINE geometry outside of the board outline is ignored.
- Text and non-contiguous lines are ignored.
- Both, Design Outline, and Cutout are located in the Board Geometry class.



Visibility Pane - Access to Mask Layers and Zones

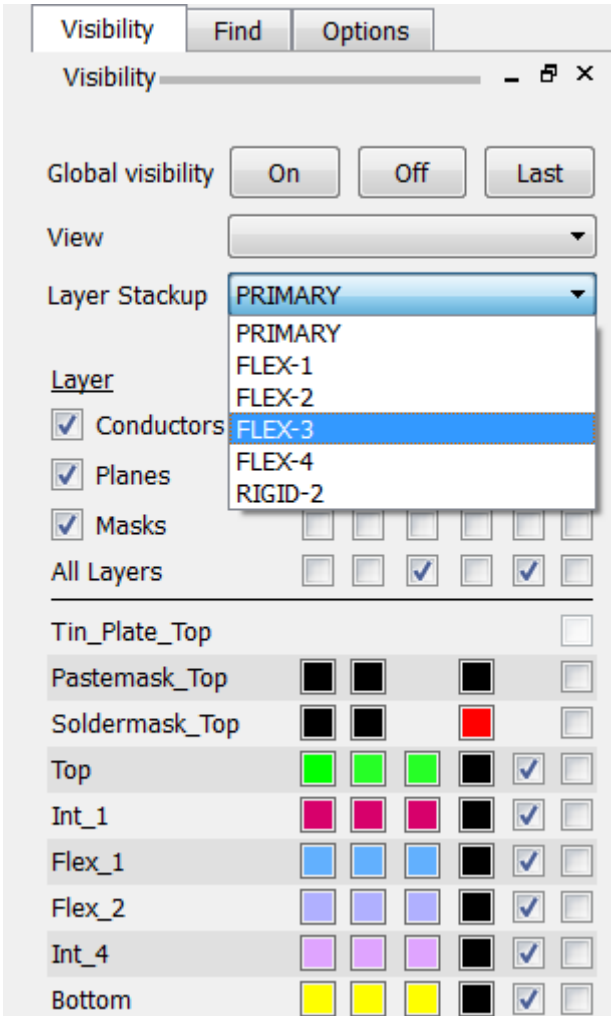
The Visibility Pane has been enhanced to allow designers access and control of layer content more quickly and more efficiently. Instead of a single stackup approach, the Visibility Pane now gives you quick access to easily configure and view different Zone stackups. This pane now has the added benefit of being able to control layers other than conductor. And, as an added benefit, you can now easily switch to a single layer view and quickly review saved layer sets – such as all your routing layers.

Layer Stackup

All stackups created in the Cross Section Editor are available in the pull-down list. Layer visibility settings adjust to the selected stackup.

Masks

The new Visibility category populates all mask layers from the respective stackup.



Dynamic Zone-based Placement

In typical rigid-flex designs, various stackup definitions are assigned to different zones where the top or bottom level may differ from zone to zone. In a traditional workaround, package symbols require special attention for padstack definitions, such as special flex symbols, etc., or use the embedded component process to place these symbols onto the correct layer for not only artwork purposes, but for documentation as well.

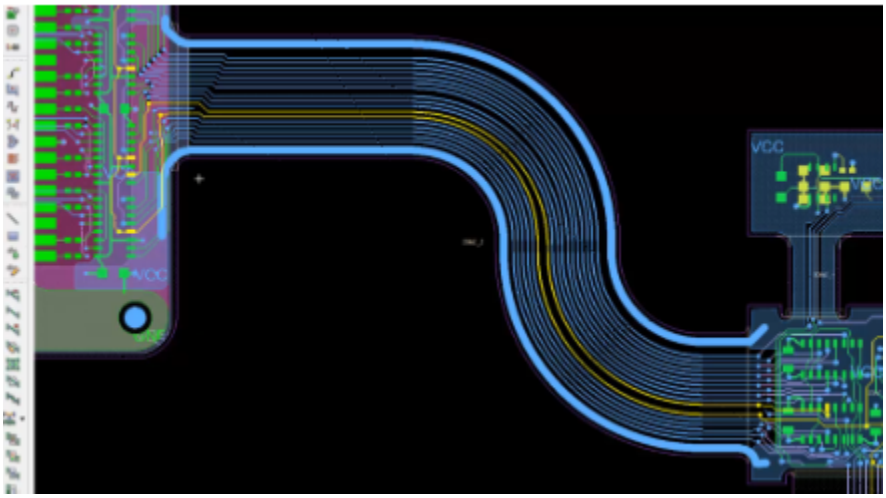
The PCB Editor's placement functions are zone aware, recognizing the top-most or bottom-most layer, and when a symbol is placed in a zone, the component definition is adjusted for

the appropriate layers for that zone. This task is performed without the need for defining embedded layers, or different padstacks, or symbols.

Enhanced Contour Routing

Note: Available in Allegro PCB Designer (Unsupported Prototype).

Enhanced Contour (*Route – Unsupported Prototype – Enable Enhanced Contour*) is a new prototype feature that provides a more efficient method to add routing during Add Connect by following an existing connect line or a route keepin. This feature has been improved over the legacy Contour feature by removing a continuous dialog popup, introducing a simple canvas-based two-state click use model and enabling Shove of existing connect lines. Transitions between the non-contoured and the contoured routing are smoothed for line or arc corners.

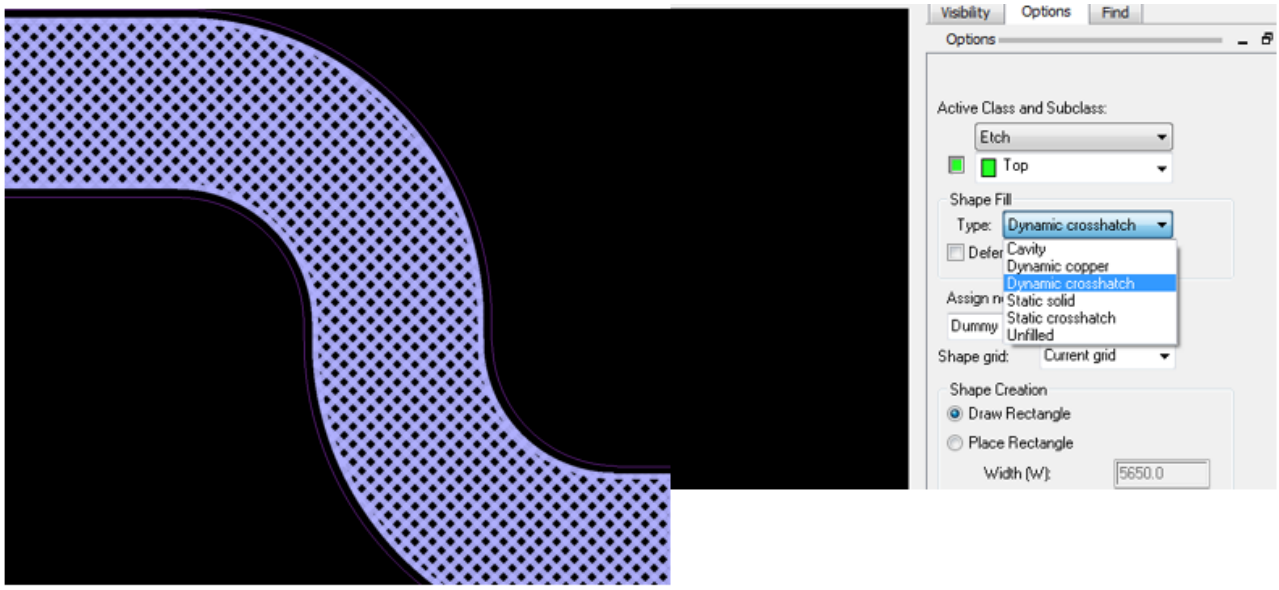


Crosshatch Shape Update

Adding Dynamic XHatch Shapes

Use of dynamic crosshatch shapes is prevalent in flex designs. Crosshatch is lighter in weight and is less prone to cracking when material is flexed. Adding dynamic crosshatch shapes

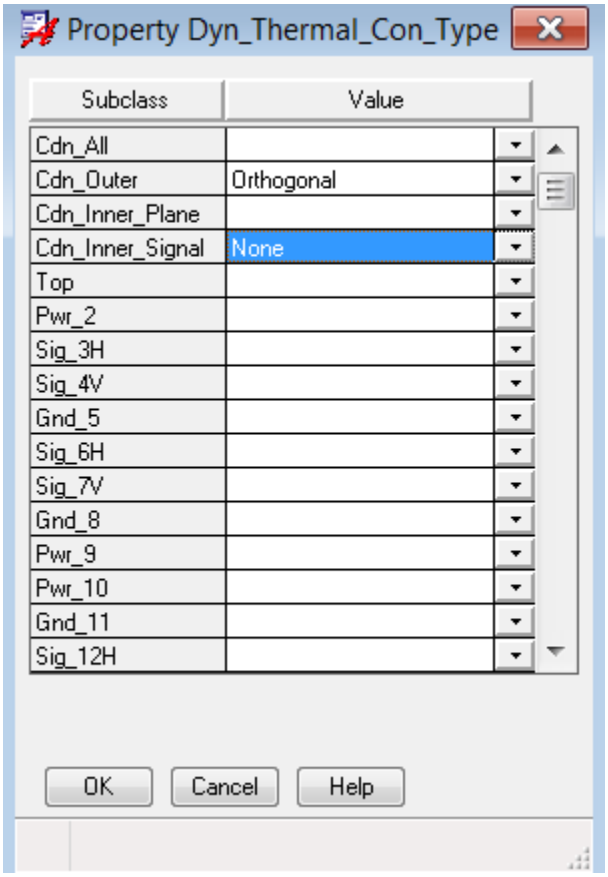
becomes easier in the 17.2 release as the shape fill drop-down menu now supports the dynamic crosshatch entry.



Dynamic Shape Update

Layer-based Property Settings

The thermal and clearance properties associated with dynamic shapes can now be applied on a per-layer basis. These properties offer you controls in the form of thermal spoke width and quantity, connection type and clearance size. Similar to the use model for creating constraint regions, you have the option of applying properties hierarchically; this includes Outer Layers, Inner Plane, and Inner Signal as well as individual layers.



The suite of properties supporting array entry includes:

- Dyn_clearance_oversize_array
- Dyn_clearance_type
- Dyn_fixed_therm_width_array
- Dyn_max_thermal_conns

- Dyn_min_thermal_conns
- Dyn_oversize_therm_width_array
- Dyn_thermal_best_fit
- Dyn_thermal_con_type

Note: Three of the properties support elements other than Pins or Vias. The array extension has been added to those properties with this conflict. Example – Apply Dyn_clearance_type to a cline; apply Dyn_clearance_oversize_array to a Pin.

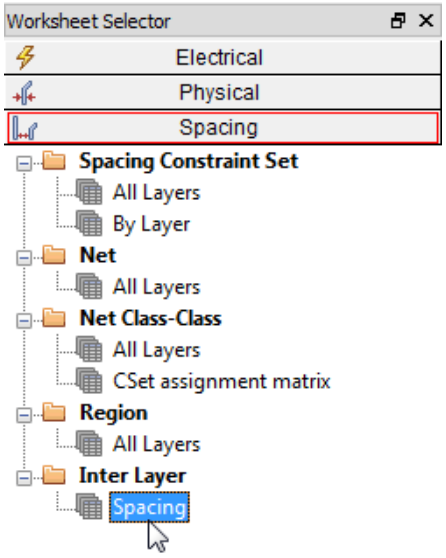
Inter Layer Checks for Rigid-Flex Design

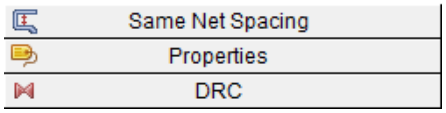
Note: Available in Allegro PCB Designer and Orcad Professional.

The PCB Editor 17.2-2016 release introduces new inter layer check functionality that provides the ability to check geometries between two different class/subclasses. In typical PCB designs, various masks and surface finishes require verification of proper clearances and coverage. Rigid-flex designs not only have the same mask and surface finish requirements but the addition of bend areas, stiffeners, and so on, that require special clearances or overlaps of materials, spacing and design features. These objects that are represented on different subclasses require verification between these layers, and this capability is now supported using the inter layer checks capabilities.

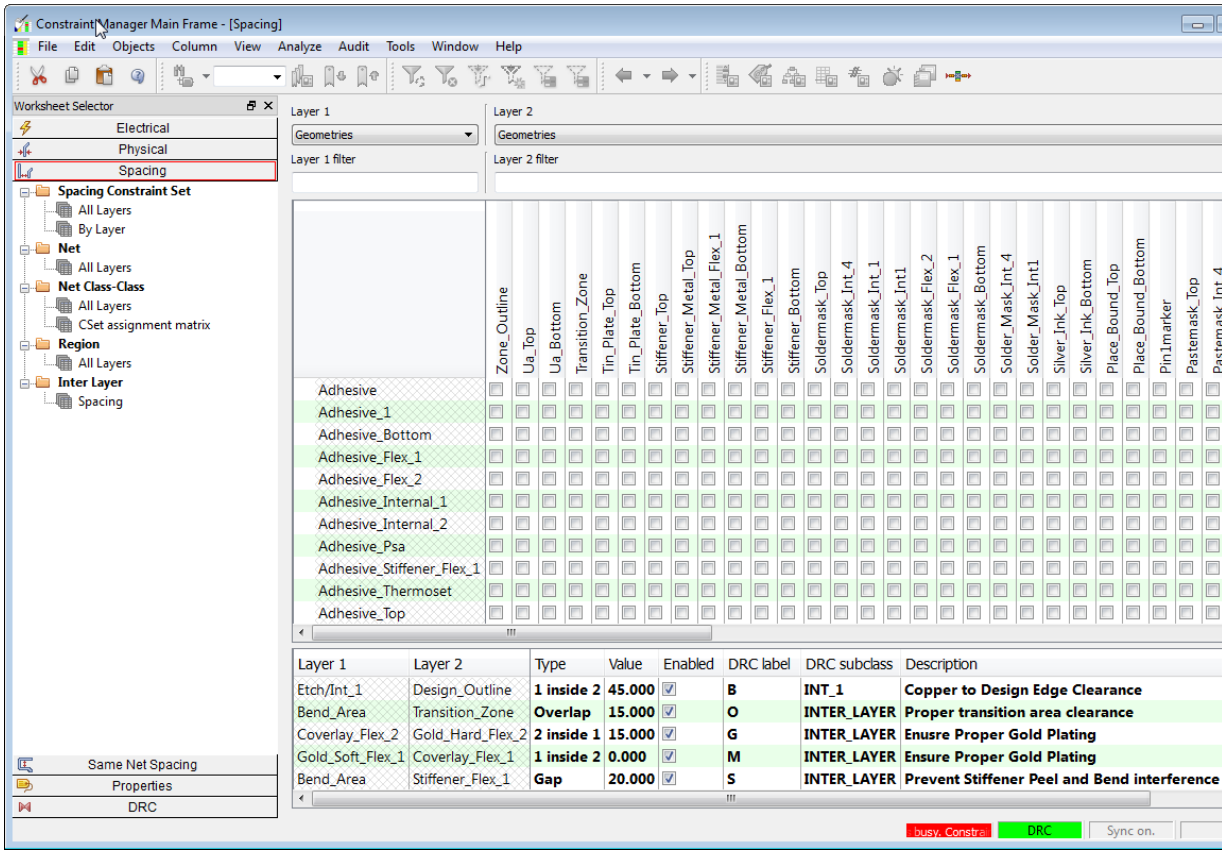
Understanding Inter Layer Check Rules

Rules that define the selection of subclasses and rule type are defined in Constraint Manager *Spacing – Inter Layer – Spacing* workbook.


Worksheet Selector
Electrical
Physical
Spacing
Spacing Constraint Set
All Layers
By Layer
Net
All Layers
Net Class-Class
All Layers
CSet assignment matrix
Region
All Layers
Inter Layer
Spacing


Same Net Spacing
Properties
DRC

Selecting this node opens a matrix of subclasses that may be selected for subclass to subclass checks.



The column on the left side of the matrix that lists eligible subclasses are labeled as Layer 1, the columns running from left to right across the top of the matrix are labeled as Layer 2.

Inter layer checks do not:

- Permit checking between etch Layers, such as top etch to bottom etch
- Same layer checks (Coverlay_top to Coverlay_top).
- Distinguish a difference between a trace (cline) or copper area (shape).

Other classes, subclasses, and objects that are not included in the inter layer checks are as follows:

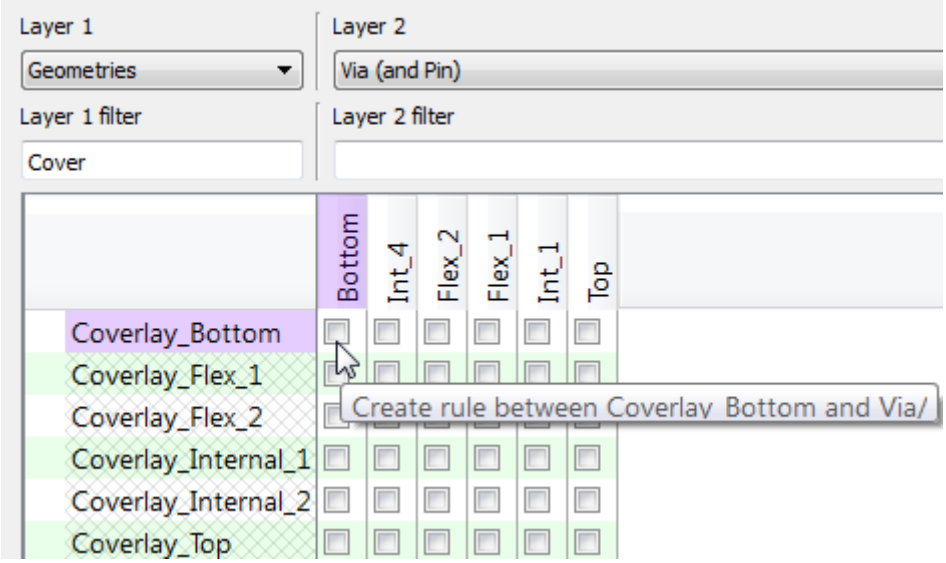
- Drawing format
- Analysis
- DRC

- Text (on any subclass)
- Board geometry outline
- Silk screen layers
- Named dielectric layers

The subclasses enabled for inter layer checking are

Subclass	Description
Conductor Layers (No Text)	Place Bound (TOP/EMBEDDED/BOTTOM)
Pin/Via Layers	Filmmask (TOP/BOTTOM)
All Mask Layers (stackup defined)	Soldermask (TOP/BOTTOM)
Rigid Flex Subclasses	Pastemask (TOP/EMBEDDED/BOTTOM)
Surface Finishes Subclasses	User-defined subclasses **Note:** User-defined subclasses in excluded classes are not enabled.

Row and column filters as well as layer type filters are provided to permit you focus on specific subclasses and subclass types. To define a check between two subclasses, the checkbox where the two subclasses intersect is enabled.



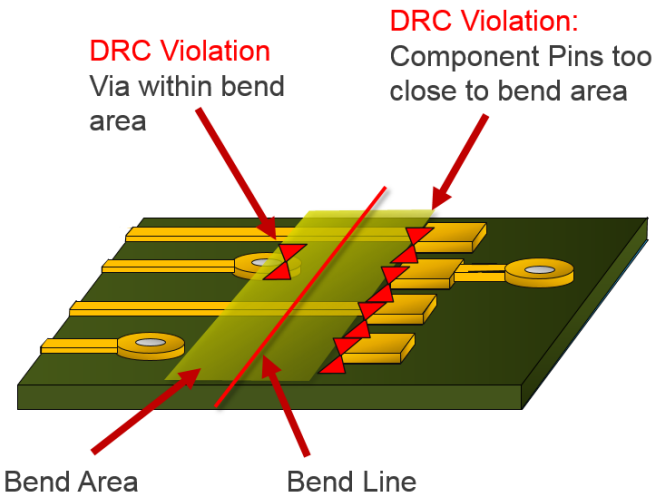
When selected, an entry is added at the top of the Rules Table. The table is located at the bottom of the Inter Layer Spacing window of Constraint Manager.

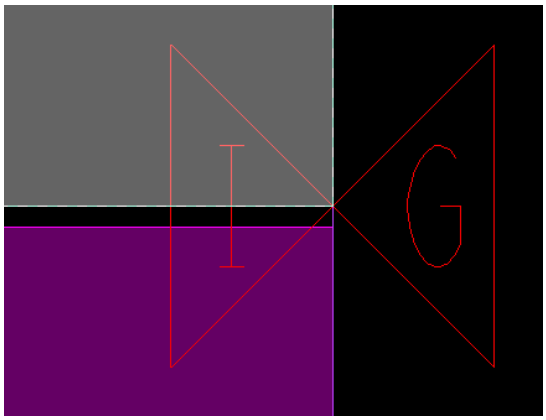
Layer 1	Layer 2	Type	Value	Enabled	DRC label	DRC subclass	Description
Coverlay_Bottom	Via (and Pin)/BOTTOM	**Undefined**	**0.000**	☐	**a**	**PACKAGE_TOP**	
Etch/Int_1	Design_Outline	**1 inside 2**	**45.000**	☑	**B**	**INT_1**	**Copper to Design Edge Clearance**
Bend_Area	Transition_Zone	**Overlap**	**15.000**	☑	**O**	**INTER_LAYER**	**Proper transition area clearance**
Coverlay_Flex_2	Gold_Hard_Flex_2	**2 inside 1**	**15.000**	☑	**G**	**INTER_LAYER**	**Enusre Proper Gold Plating**
Gold_Soft_Flex_1	Coverlay_Flex_1	**1 inside 2**	**0.000**	☑	**M**	**INTER_LAYER**	**Ensure Proper Gold Plating**
Bend_Area	Stiffener_Flex_1	**Gap**	**20.000**	☑	**S**	**INTER_LAYER**	**Prevent Stiffener Peel and Bend interference**

The rule table defines the following:

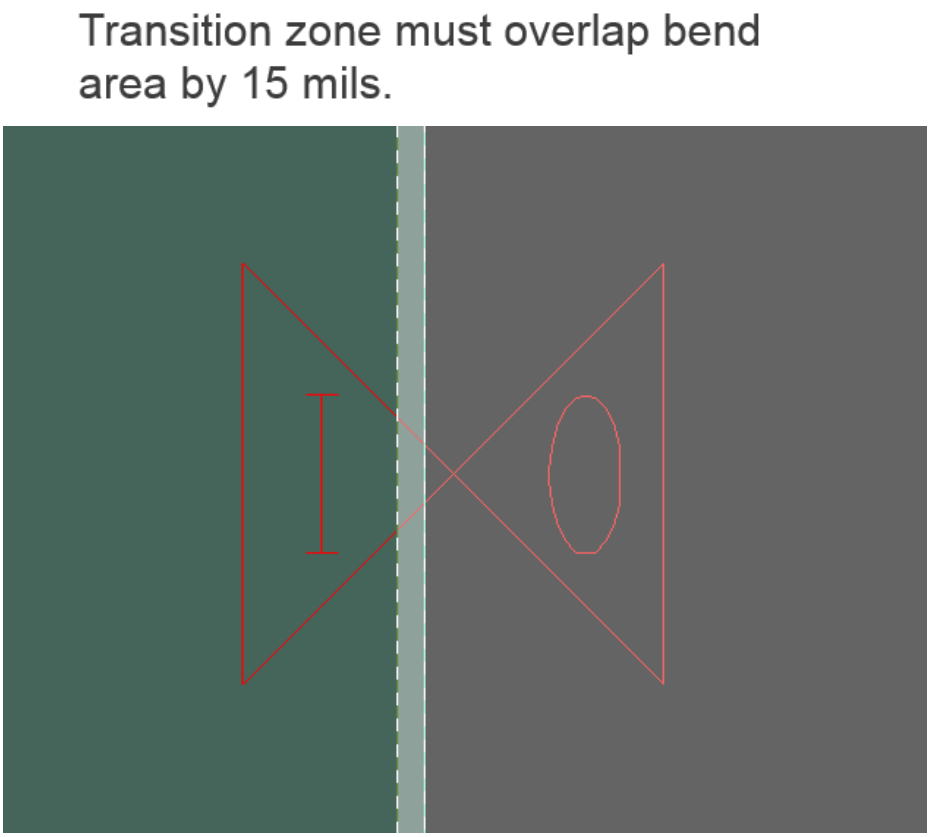
- Layer 1: The subclass name selected as Layer 1
- Layer 2: The subclass name selected as layer 2
- Type: The specific checking type to be defined. A drop-down provides a list of possible checks

- Gap: A minimum spacing value between two objects on the selected subclass layers.



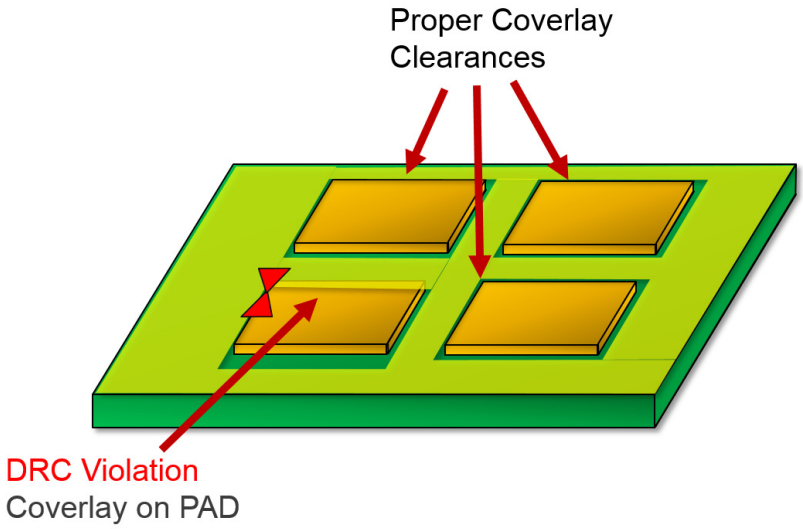


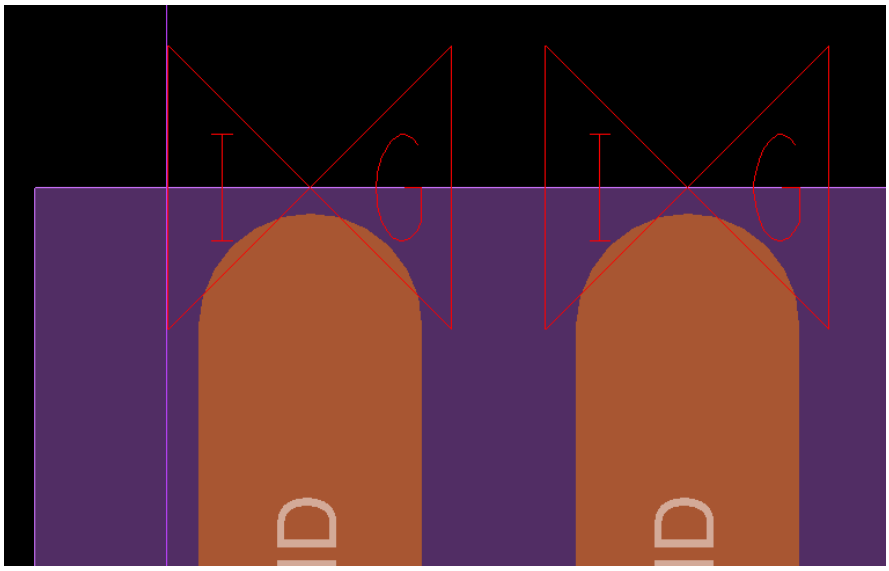
- Overlap: minimum overlap value between two objects on the selected subclass layers.



- 1 inside 2: The geometry on the subclass defined as layer 1 must be contained within a geometry on the subclass defined as layer 2.

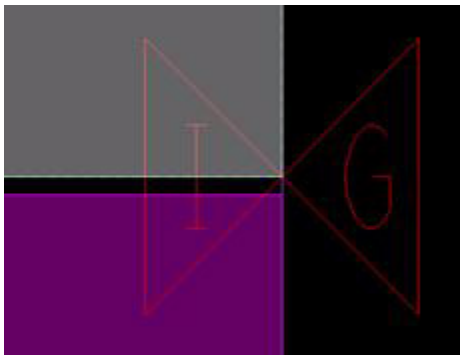
- 2 inside 1: The geometry on the subclass defined as layer 2 must be contained within a geometry on the subclass defined as layer 1.





- Value: the spacing dimension defined in user units
- Enabled: the check, when enabled, allows the check to be performed. When not enabled, the check is disabled.
- DRC Label: This field allows you to add your own DRC marker label for the second character. The first character is reserved with the character “I” for inter layer checks. The

second character can be any, single character a-z, A-z, 0-9. No special characters are not supported.



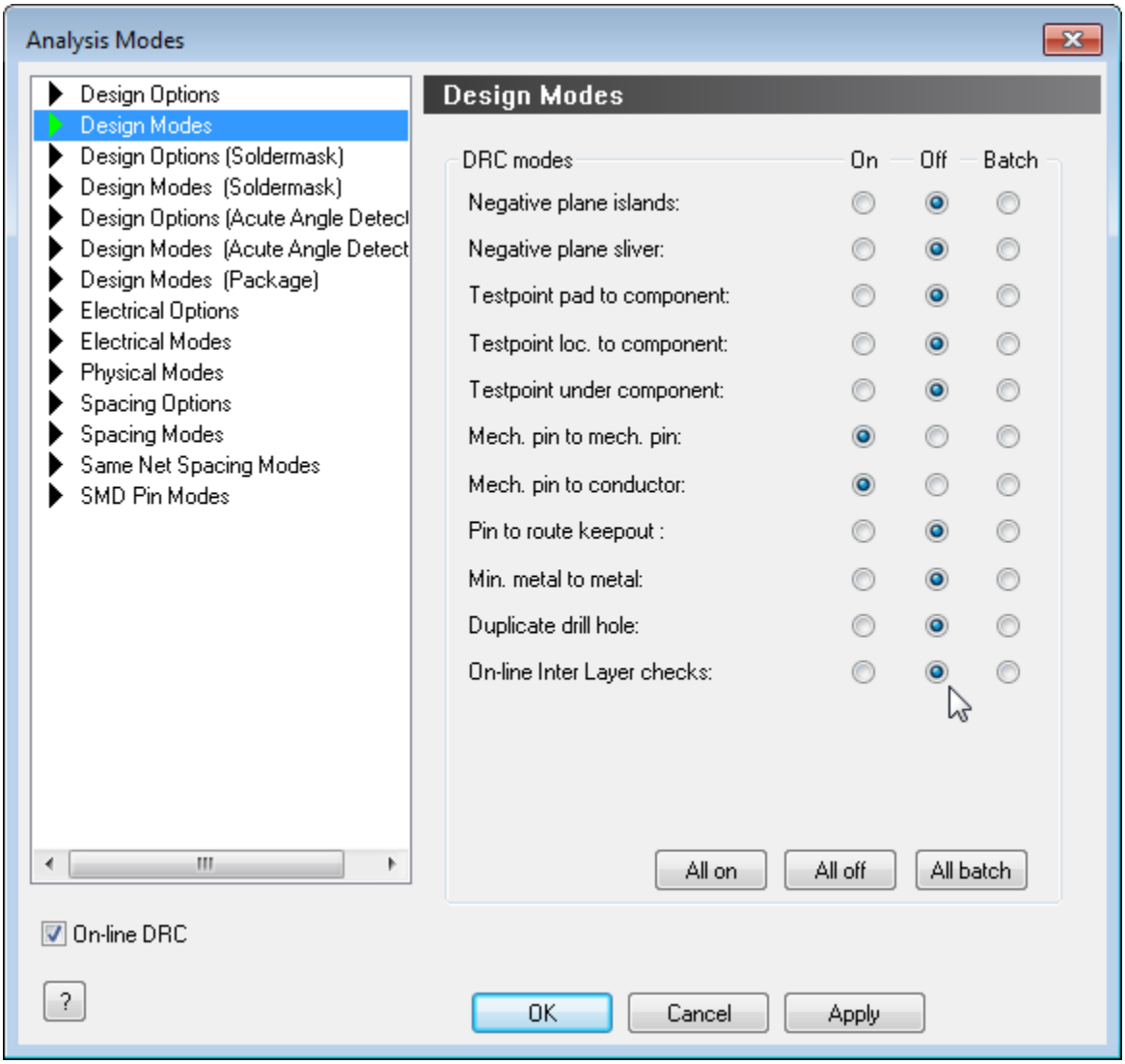
- DRC Subclass: This defines the display layer for the DRC marker. A pull-down menu lists the available subclasses that the rule's DRC marker can be displayed on. A new INTER_LAYER subclass was added under the DRC class to assist in distinguishing inter layer DRCs from other DRCs.
- Description: A comment or description of the rule may be added for reference. This description can only be seen in the rules table form within the constraint manager.
- Delete: Selecting the "X" in the Delete column will remove the rule entry.

Known Limitations

- Inter layer checks are checks between subclass, not same layer checks.
- Filtered groups for vias (and pins) are one single group.
- Filtered groups for conductors consists of clines and shapes.
- Overlap and inside checks do not detect missing geometry. For example, a gold pin requires an opening in the cover lay. If a cover lay geometry partially covers the pin, the DRC is detected. If no cover lay opening exits, no error is detected.

Enabling On-line Inter-Layer Checking

By default, the on-line inter layer checks are set to *Off* in the PCB Editor. To enable this capability, you must set the constraint mode for inter layer checks. There are two options: On-line and Batch.



Manufacturing Prep - Rigid-Flex Design

Multiple Stackup Table

The *Manufacture – Cross Section Chart* program now supports an option to output a multi stackup table. The table supports entries for all conductor and non-conductor layers, material and thicknesses.

MULTIPLE STACKUP TABLE

Unit = mils

#	NAME	TYPE	MATERIAL	RIGID-2	FLEX-3	FLEX-4	PRIMARY	FLEX-1	FLEX-2
=		SURFACE	AIR	0.000	0.000	0.000	0.000	0.000	0.000
=	STIFFENER FLEX 1	MASK	FR-4		8.000				
=	TIN PLATE TOP	MASK	TIN	0.500	0.500	0.500	0.500	0.500	0.500
=	ADHESIVE STIFFENER FLEX 1	MASK	ADHESIVE EPOXY		0.984			0.984	
=	COVERLAY FLEX 1	MASK	POLYIMIDE		8.000	8.000		8.000	8.000
=	ADHESIVE FLEX 1	MASK	ADHESIVE ACRYLIC		0.500	0.500		0.500	0.500
=	GOLD SOFT FLEX 1	MASK	POLYIMIDE						8.000
=	PASTEMASK TOP	MASK	SOLDER PASTE SAC				3.000		
=	SOLDERMASK TOP	MASK	SOLDERMASK FLEXIBLE LPI				0.591		
=	SOLDERMASK INT1	MASK	SOLDERMASK FLEXIBLE LPI	0.591					
=	PASTEMASK INT1	MASK	SOLDER PASTE SAC	3.000					
1	TOP	CONDUCTOR	COPPER				1.200		
=		DIELECTRIC	FR-4				8.000		
2	INT 1	CONDUCTOR	COPPER	1.200			1.200		
=		DIELECTRIC	POLYIMIDE RIGID 5MIL	5.000			5.000		
3	FLEX 1	CONDUCTOR	COPPER	1.200	1.200	1.200	1.200	1.200	1.200
=		DIELECTRIC	POLYIMIDE FILM	3.000	3.000	3.000	3.000	3.000	3.000
4	FLEX 2	CONDUCTOR	COPPER	1.200	1.200	1.200	1.200	1.200	1.200
=		DIELECTRIC	POLYIMIDE RIGID 5MIL	5.000			5.000		
5	INT 4	CONDUCTOR	COPPER	1.200			1.200		
=		DIELECTRIC	FR-4				8.000		
6	BOTTOM	CONDUCTOR	COPPER				1.200		
=	PASTEMASK BOTTOM	MASK	SOLDER PASTE SAC				3.000		
=	SOLDERMASK BOTTOM	MASK	SOLDERMASK FLEXIBLE LPI				0.591		
=	PASTEMASK INT 4	MASK	ADHESIVE ACRYLIC	0.500	0.500	0.500	0.500	0.500	0.500
=	SOLDERMASK INT 4	MASK	POLYIMIDE	8.000	8.000	8.000	8.000	8.000	8.000
=	GOLD HARD FLEX 2	MASK	POLYIMIDE			8.000			
=	ADHESIVE FLEX 2	MASK	POLYIMIDE		8.000	8.000		8.000	8.000
=	COVERLAY FLEX 2	MASK	POLYIMIDE		8.000	8.000		8.000	8.000
=		SURFACE	AIR	0.000	0.000	0.000	0.000	0.000	0.000
			TOTAL THICKNESS	30.391	47.884	46.900	52.381	39.884	46.900
			ZONE NAME	ZONE_5 ZONE_3	ZONE_8	ZONE_9		ZONE_4 ZONE_7 ZONE_2	ZONE_6

Dynamic Fillets

Dynamic fillets can now be controlled on a per-layer basis. The control setting is located in the Physical section of the Cross Section Editor.

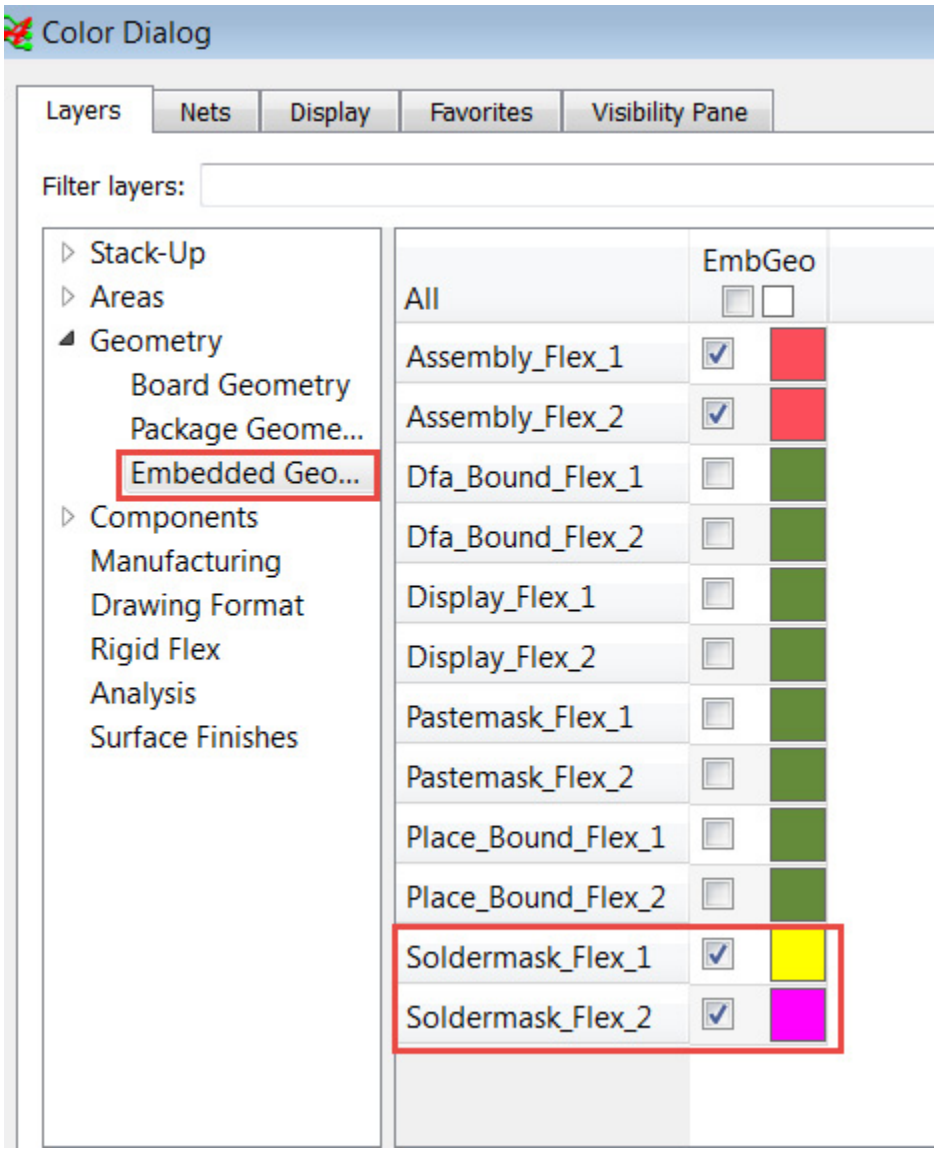
Missing Tapers Report

A new report, missing tapers report, detects missing tapers on line-width transitions.

Embedded Component Design Updates

Note: Available in Allegro PCB Designer (Miniaturization Product Option)

- The Copy command now supports embedded package symbols.
- The Swap Components command can now be used on dummy components.
- Embedded Soldermask subclasses are now supported (similar to Pastemask).
- Extracta support for embedded Components was provided in 16.6-2015 ISR.



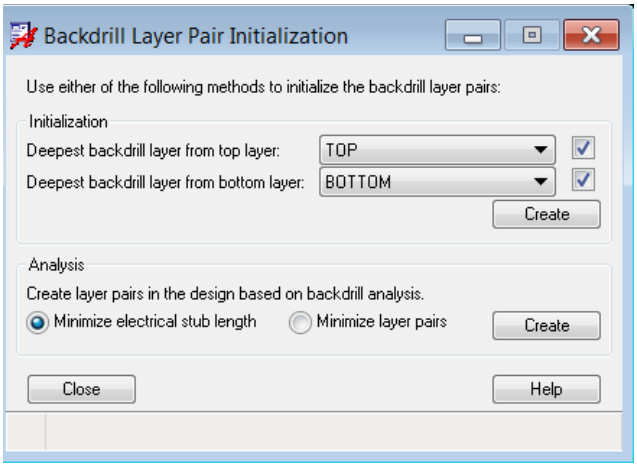
Backdrill Overhaul

Note: Requires Allegro PCB Designer

The Backdrill application has undergone some significant enhancements. Backdrill data is now stored in the library padstacks and utilized at the design level during the analysis and backdrill generation process. Padstacks which do not have pre-defined backdrill information can be automatically updated at the design level by the entering the backdrill criteria prior to running backdrill. Design layers which are backdrilled will have Route Keepout Shapes generated to ensure that design integrity is maintained with separate padstack definition controls for the backdrill start layer, internal layer and negative layer anti-pad geometries without the need for custom padstacks or scripts. All backdrill data is available on the individual Pin/Via objects displayed on the canvas or by simply querying the object using Show Element, and generating the Backdrill Legends and detailed Backdrill Report. In addition, the setup time for backdrill can now be improved as a result of algorithms designed to create intelligent layer pairs.

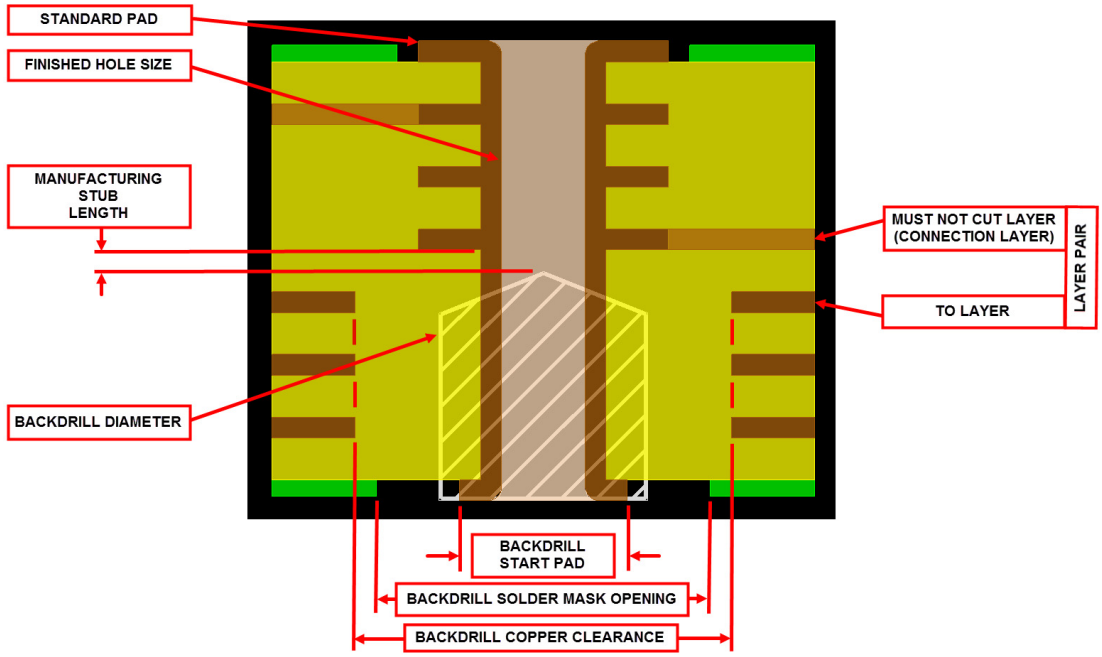
Design Flow Considerations

You can consider one of two backdrill flows. The preferred flow is based on updating and maintaining padstacks at the library level to drive backdrill requirements into the design. Library driven flows typically provide the highest level of consistency and flexibility over parameterized flows. An example of flexibility could be defining the backdrill requirements for a via used specifically for BGA fanout vs. convention signal vias. The via used for BGA fanout may require smaller backdrill clearances due to tighter routing channels.



The alternative flow has no library dependencies and setup is done in the backdrill setup and analysis form inside the PCB Editor. A series of oversize/undersize parameter values are entered and utilized when backdrill is executed. Padstacks in the database are updated

based on the values specified. This is the quickest adoption method but may lack flexibility or pose risk if oversize/undersize values are not entered correctly.

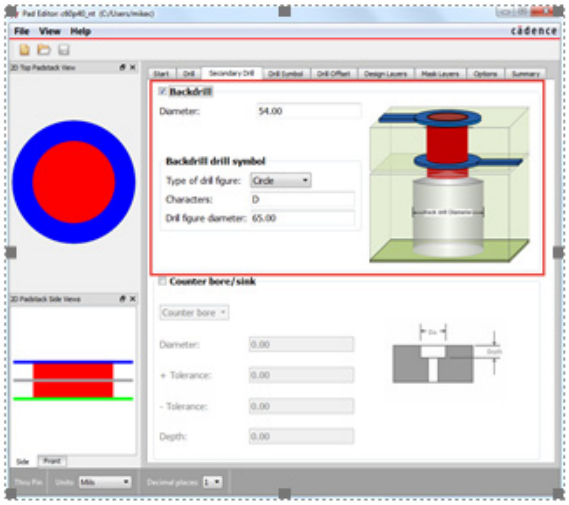


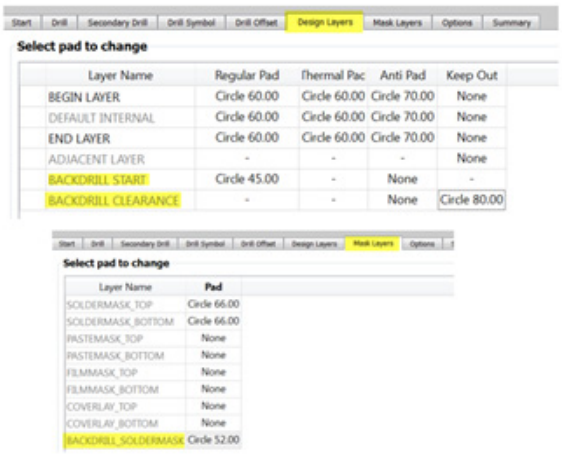
Library-Driven Flow (Cadence Recommended)

At the heart of the backdrill enhancements are the updates made to the pad definition. It now supports several records for defining the backdrill diameter and supporting clearances/entry pads. Before committing 17.2 into production, one should examine the work required to update existing padstacks in their corporate library; ones typically used in backdrill applications such as those associated with connectors, thru or core vias. Assuming the update is against very large libraries, developing a ‘just in time’ process should be considered. Once implemented, there should not be a reason to run padstack replacement routines or manual editing of pad instances as commonly done in the 16.x releases. The summary of enhancements made to the pad definition to support backdrill include:

- Backdrill hole diameter along with unique drill figure, character and figure diameter
- Drill Tool Size used to specify actual drill size or tool number (commonly used to instruct fabrication to drill per connector supplier specifications)
- Start Layer pad size for backdrill entry layer (typically top, bottom or both)
- Signal and Positive Plane Keepout Pad (used in start-end range of backdrill path)

- Negative Plane Antipad (used in start-end range of backdrill path)
- Soldermask pad for backdrill entry layer





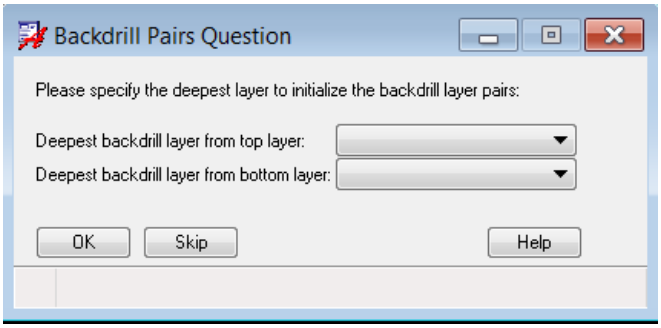
Setup and Analysis User Interface

The Setup and Analysis form continues to be the primary interface to setup Layer Pairs (formerly called passes). The setup of layer pairs can be a time consuming, experimental process. In 17.2, new controls help you to determine the best strategy based on certain qualifiers. The next few sections review the controls within the user interface.

Layer Pair Initialization

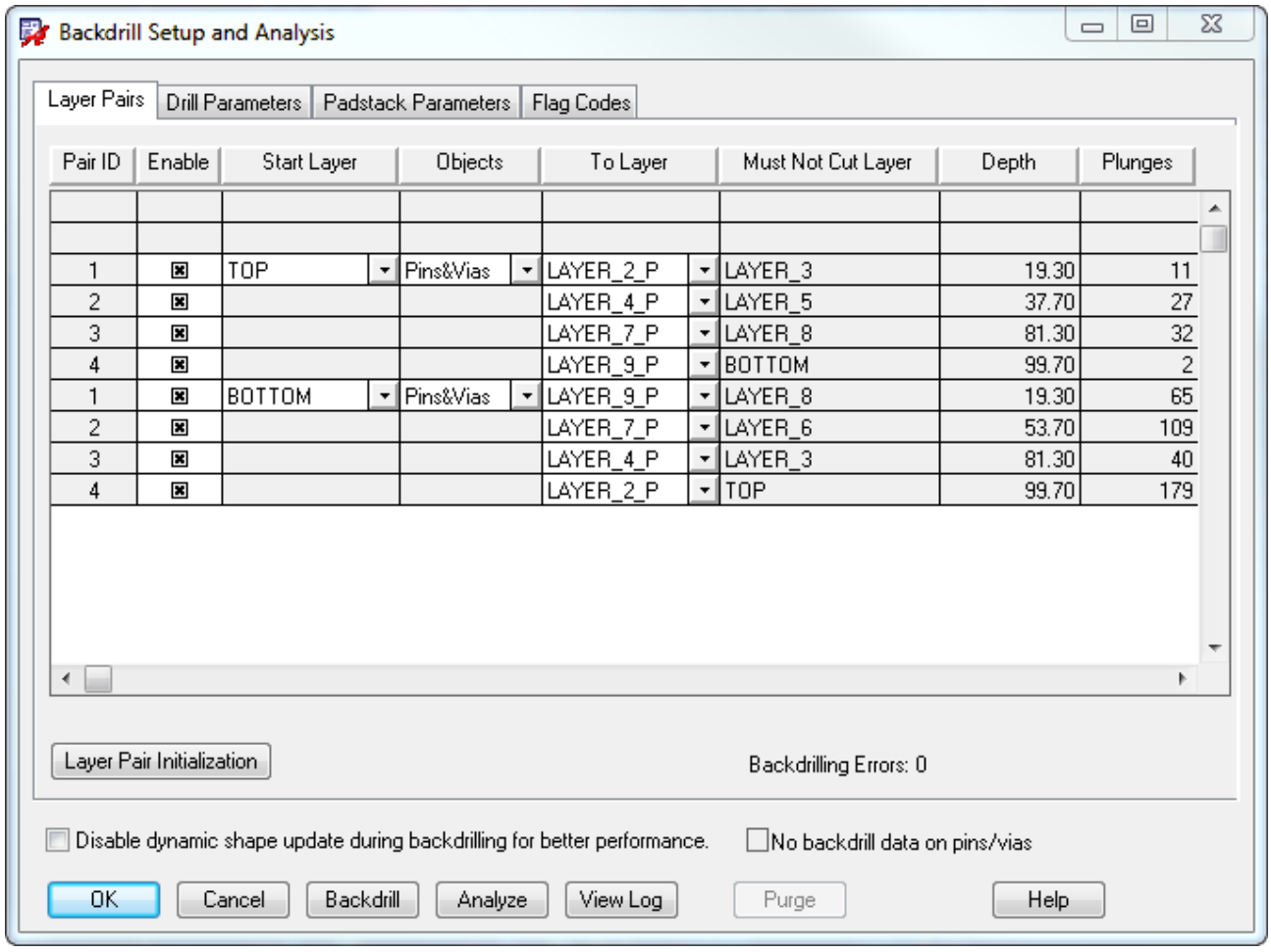
Clicking this button automatically generates Backdrill Layer Pairs. Choose the qualifier that is best for your design flow. They include:

- Deepest Backdrill Layer from Top and Bottom Layers (all combinations produced but generally too many to consider). Click ‘skip’ to proceed to next 2 options.
- Minimized electrical stub lengths (highest electrical performance, shortest stubs)
- Minimize layer pairs (cost efficient, least amount of layer pairs)



Layer Pairs Tab

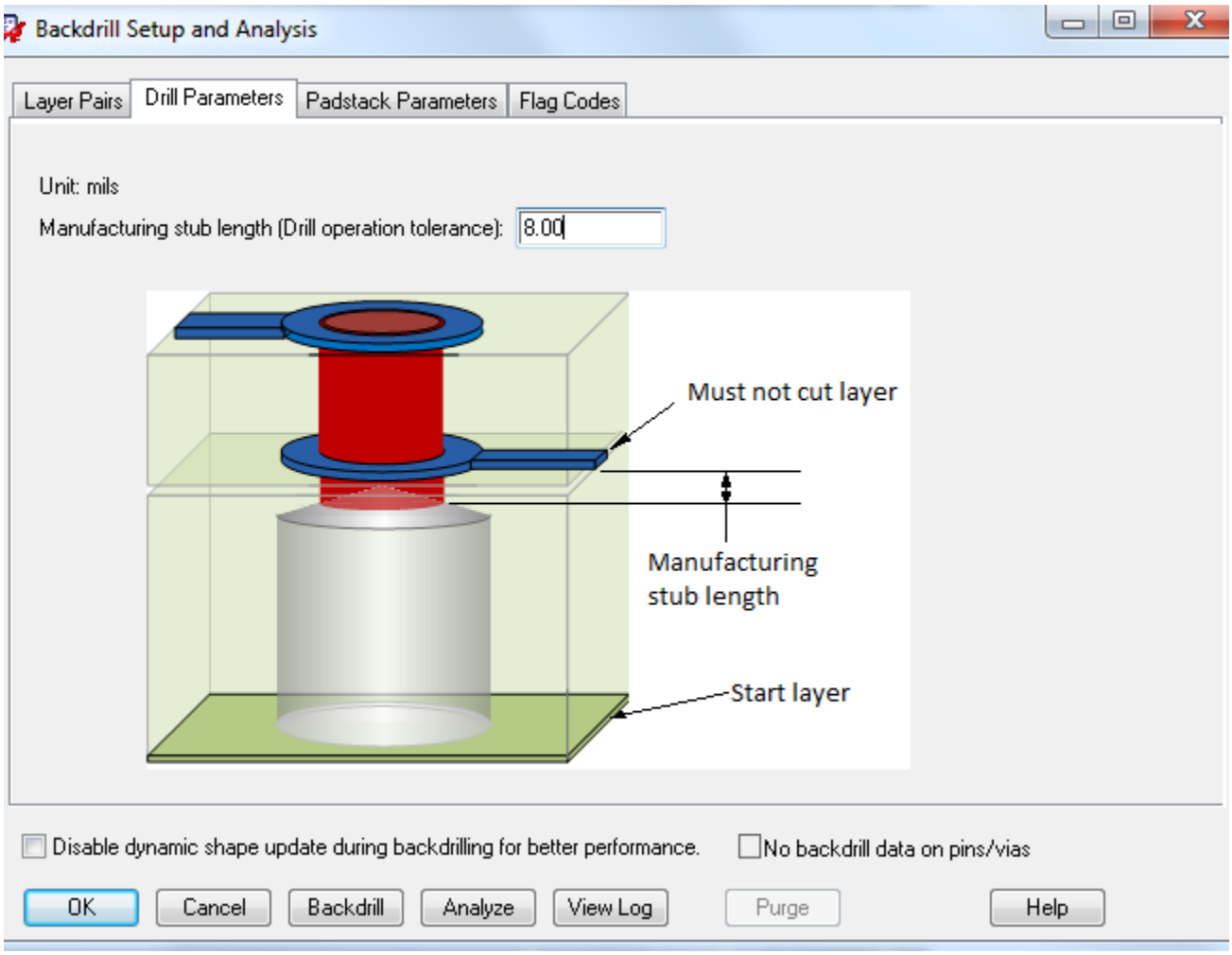
- Pair ID – Backdrill From-To Pair (Was Pass # on 16.6)
- Start Layer – Start layer of Backdrill (Was From Layer on 16.6)
- Objects – Objects to be Back-drilled (Pins, Vias or Pins/Vias)
- To Layer – Last layer to be Back-drilled
- Must Not Cut Layer – Layer with connection that required conductivity (New)
- Depth – Depth from Start Layer to outside surface of the Must Not Cut Layer
- Plunges – Number of possible Backdrill locations (New)



Drill Parameters Tab

- Manufacturing Stub Length – Minimum tolerance for secondary drill operation
- Typically the backoff tolerance from the MNC layer; varies between Fabricators and may be dependent on drill depth.

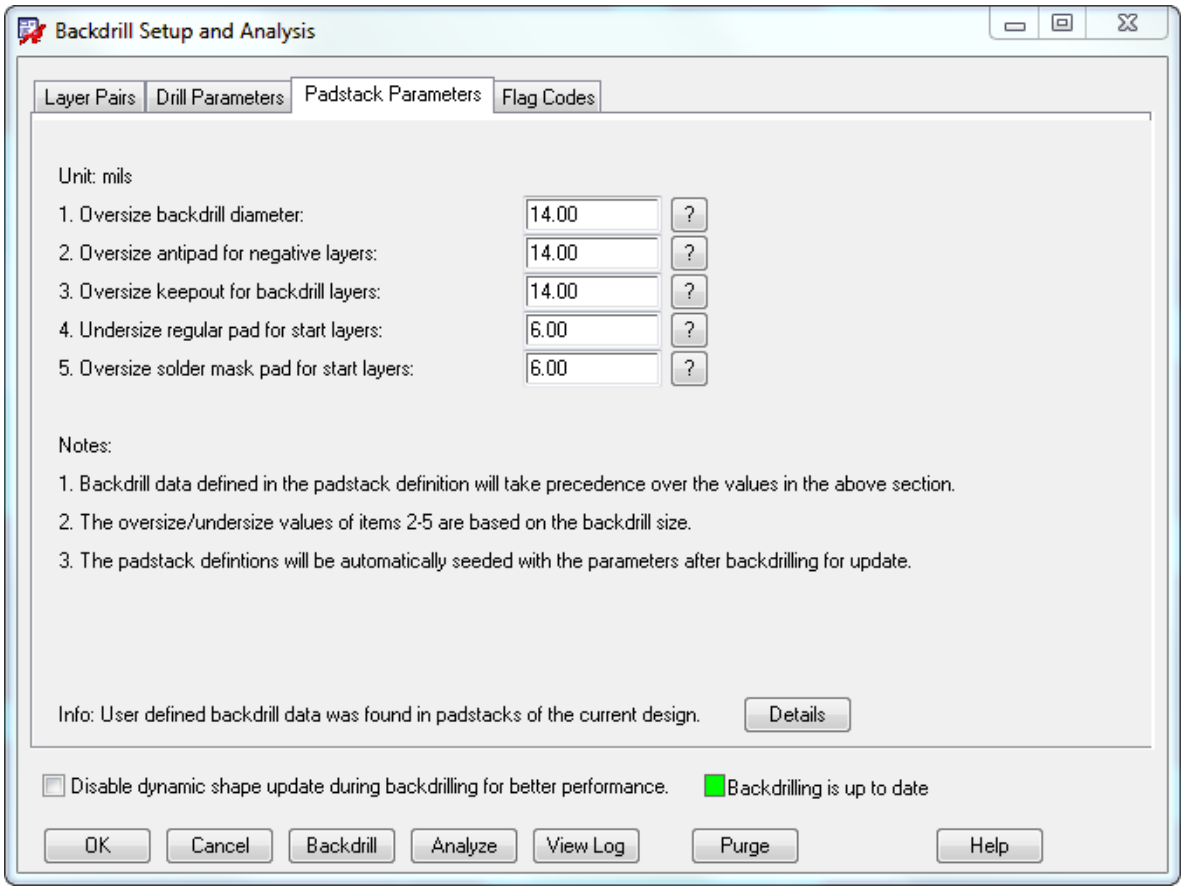
- Value is populated in NC Legend



Padstack Parameters Tab (Optional)

- Parameter values are used to update/generate backdrill data in design level padstacks.
- Important - Library defined pads with backdrill data will always supersede parameterized pads in the database. In short, library wins!
- Oversize backdrill diameter – Value added to Finished Hole Size in padstack to determine the Backdrill Diameter size.
- Oversize/Undersize values of items 2-5 are based on the backdrill size generated.
- Clicking on “?” button next to each of the fill-in fields will describe and assist in value entry to achieve the desired result.

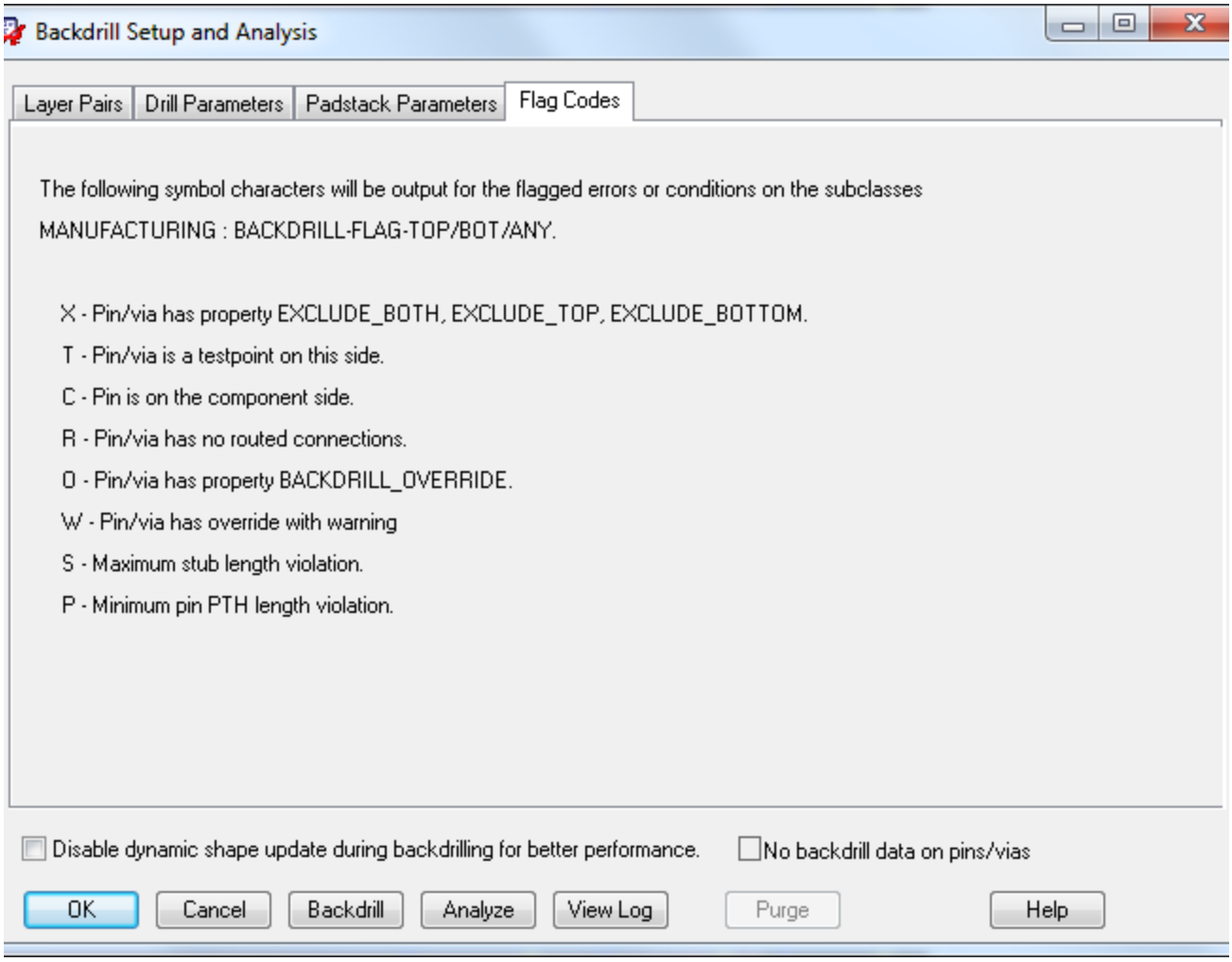
- The Details button will list all plated padstack in the design and identify which have defined backdrill data driven from the library or manually entered in the design. This report can be very helpful if implementing a 'just in time' library driven flow.



- Backdrill button– Analyze and generate backdrill data on pins/vias in the design. Padstacks without pre-defined Backdrill data, driven from the library or manually entered, will be updated based on the criteria under the Padstack Parameter tab
- Analyze button – Analyze design only and report backdrill information but do not add backdrill data on pins/vias or update padstack backdrill values
- Purge button – Purge Backdrill data on pins/vias only, padstacks will not be purged of backdrill data
- Backdrill status
  - Red – Backdrill data are out of date, Click button "Backdrill" to update the status.
  - Green – Backdrill data on pins/vias are in sync
  - Grey – No backdrill data (side, start layer, must-cut-layer) saved on pins/vias yet

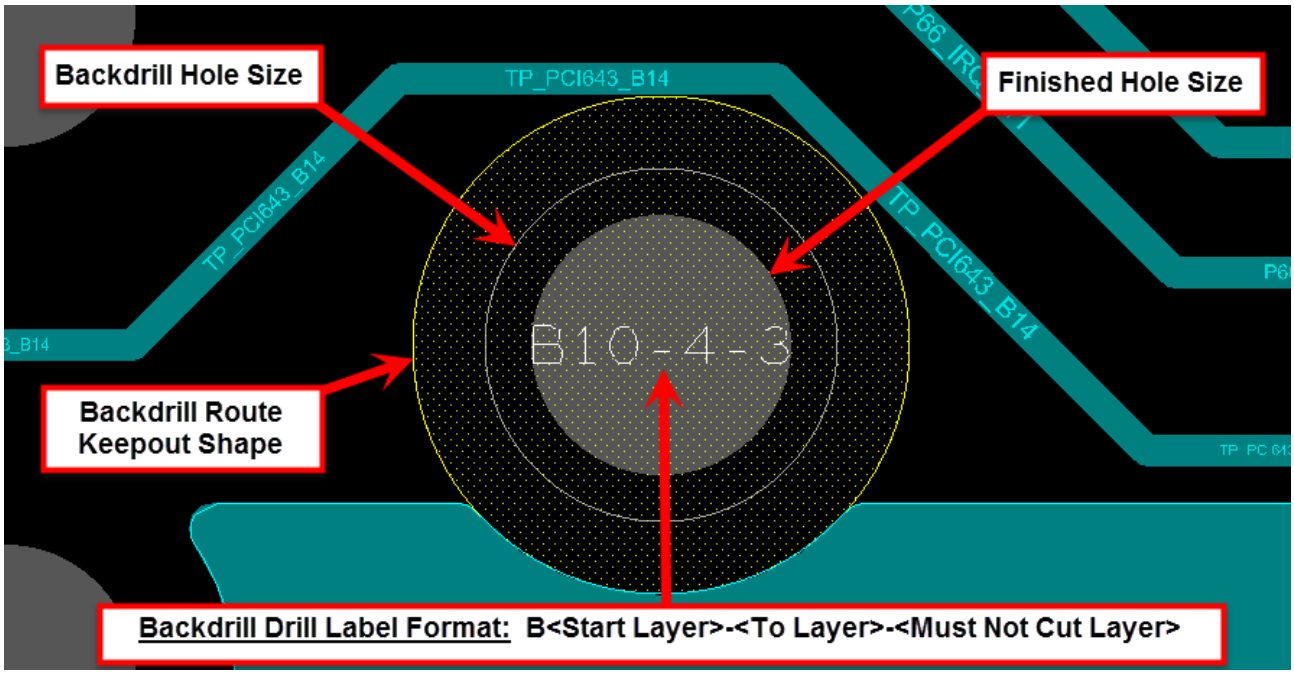
Flag Codes Tab

Quick reference legend for symbols generated on MANUFACTURING BACKDRILL-FLAG-TOP, BACKDRILL-FLAG-BOT and BACKDRILL-FLAG-ANY which identify reasons why a backdrill was not generated.


Backdrill Setup and Analysis
Layer Pairs
Drill Parameters
Padstack Parameters
Flag Codes
The following symbol characters will be output for the flagged errors or conditions on the subclasses
MANUFACTURING : BACKDRILL-FLAG-TOP/BOT/ANY.
X - Pin/via has property EXCLUDE_BOTH, EXCLUDE_TOP, EXCLUDE_BOTTOM.
T - Pin/via is a testpoint on this side.
C - Pin is on the component side.
R - Pin/via has no routed connections.
O - Pin/via has property BACKDRILL_OVERRIDE.
W - Pin/via has override with warning
S - Maximum stub length violation.
P - Minimum pin PTH length violation.
Disable dynamic shape update during backdrilling for better performance.
No backdrill data on pins/vias
OK
Cancel
Backdrill
Analyze
View Log
Purge
Help

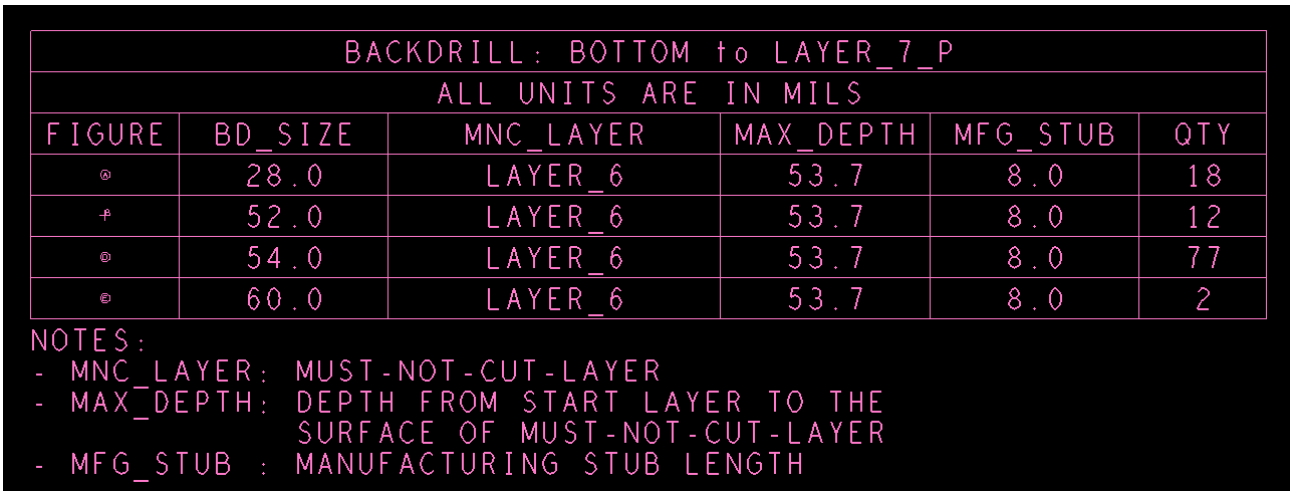
Backdrill Canvas Display Controls

Using the “backdrill holes” and “drill label” settings found in the Setup –Design Parameters – Display form, it’s now possible to visualize the actual backdrill hole size and drill labels that define the backdrill layer range.



Backdrill NC-Drill Legend updates

The NC Legend has been enhanced to support the backdrill diameter, figure, Mfg Stub and Must Not Cut Layer (MNC). The Mfg Stub value is driven from the entry in the backdrill setup form – Drill Parameter Tab.



BACKDRILL: BOTTOM to LAYER_7_P

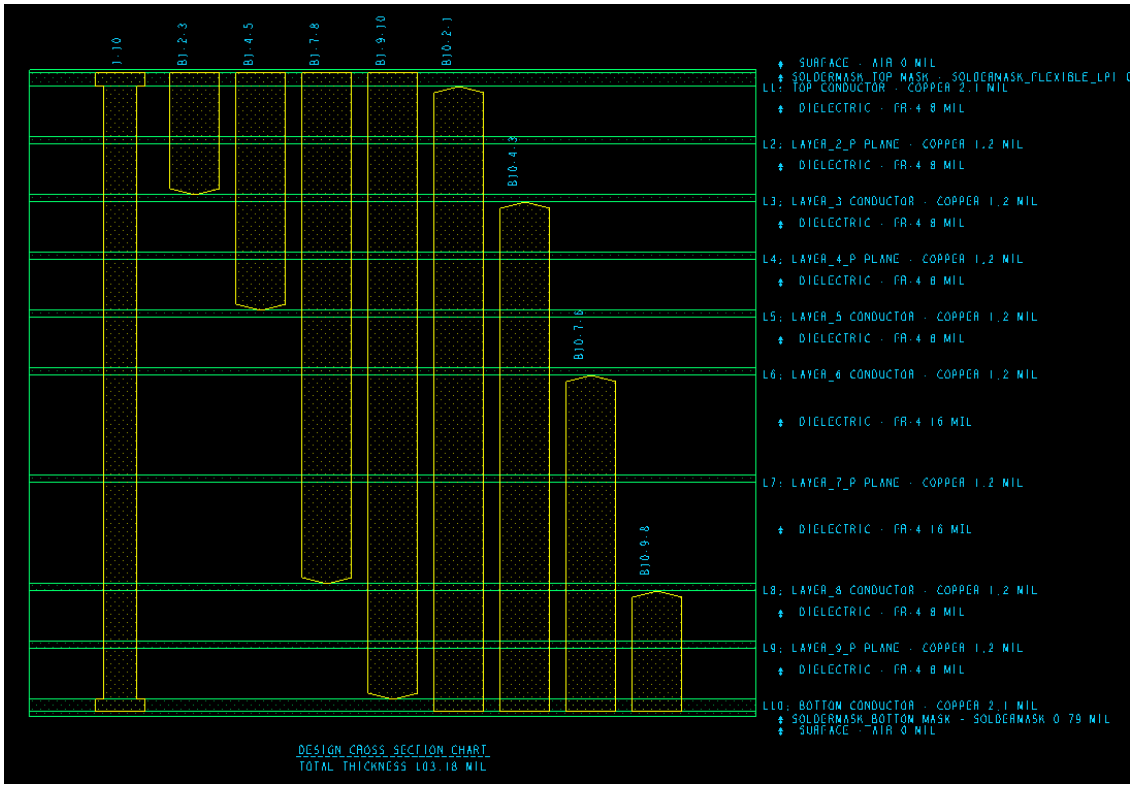
ALL UNITS ARE IN MILS

FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
⊗	28.0	LAYER_6	53.7	8.0	18
⊕	52.0	LAYER_6	53.7	8.0	12
⊙	54.0	LAYER_6	53.7	8.0	77
◎	60.0	LAYER_6	53.7	8.0	2

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

Backdrill Cross Section Chart Display

Backdrill span in cross section detail will show a tapered end before just below first active conductive layer. (Must Not Cut Layer)



Test Prep update

Adding Test Points manually or automatically will respect existing backdrill sites and will not update the padstack or attempt to mark them as a test point.

Existing Test Point sites will be skipped during backdrilling and marked with a T Flag Code indicating it is a potential backdrill candidate that was not backdrilled.

Manufacturing Data

- IPC-D-356 – Output will include any backdrill data with an option to ignore the backdrill data during output.

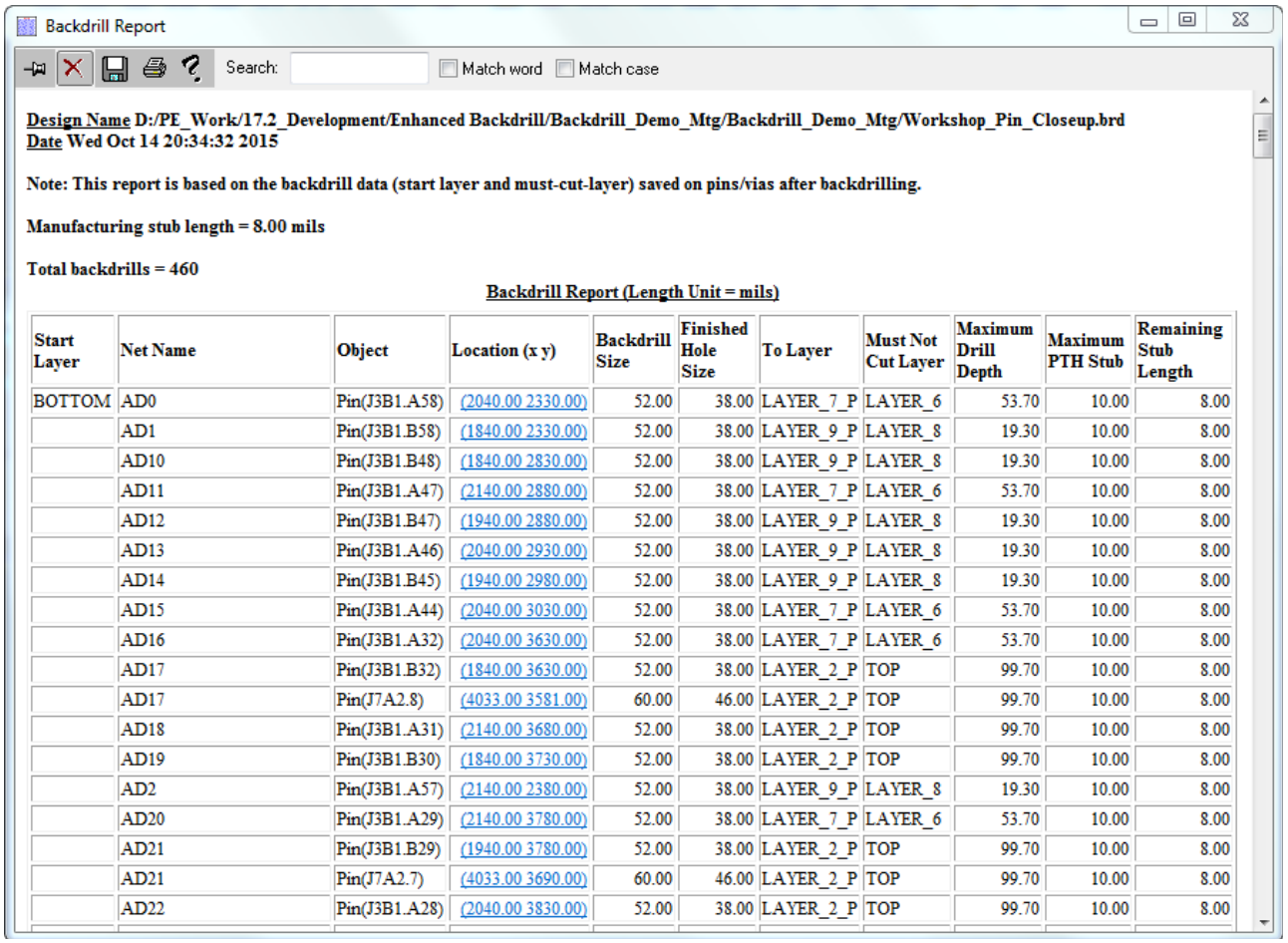
- IPC-2581 – Backdrill specification is updated with START_LAYER, MUST_NOT_CUT_LAYER, and MAX_STUB_LENGTH.
- Backdrill NC Drill File– Comment/Notes is updated with backdrill size, MUST-NOT-CUT-LAYER, MAX_DRILL_DEPTH, and MFG_STUB_LENGTH.

Extracta

API and extracta program can be used to get backdrill data on pins/vias.

Reports

- New detailed backdrill report added to standard reports
- Lists all backdrill data for the backdrilled pins/vias
- Lists total backdrills and manufacturing stub length



Design Name D:/PE_Work/17.2_Development/Enhanced Backdrill/Backdrill_Demo_Mtg/Backdrill_Demo_Mtg/Workshop_Pin_Closeup.brd
Date Wed Oct 14 20:34:32 2015

Note: This report is based on the backdrill data (start layer and must-cut-layer) saved on pins/vias after backdrilling.

Manufacturing stub length = 8.00 mils

Total backdrills = 460

Backdrill Report (Length Unit = mils)

Start Layer	Net Name	Object	Location (x y)	Backdrill Size	Finished Hole Size	To Layer	Must Not Cut Layer	Maximum Drill Depth	Maximum PTH Stub	Remaining Stub Length
BOTTOM	AD0	Pin(J3B1.A58)	(2040.00 2330.00)	52.00	38.00	LAYER_7_P	LAYER_6	53.70	10.00	8.00
	AD1	Pin(J3B1.B58)	(1840.00 2330.00)	52.00	38.00	LAYER_9_P	LAYER_8	19.30	10.00	8.00
	AD10	Pin(J3B1.B48)	(1840.00 2830.00)	52.00	38.00	LAYER_9_P	LAYER_8	19.30	10.00	8.00
	AD11	Pin(J3B1.A47)	(2140.00 2880.00)	52.00	38.00	LAYER_7_P	LAYER_6	53.70	10.00	8.00
	AD12	Pin(J3B1.B47)	(1940.00 2880.00)	52.00	38.00	LAYER_9_P	LAYER_8	19.30	10.00	8.00
	AD13	Pin(J3B1.A46)	(2040.00 2930.00)	52.00	38.00	LAYER_9_P	LAYER_8	19.30	10.00	8.00
	AD14	Pin(J3B1.B45)	(1940.00 2980.00)	52.00	38.00	LAYER_9_P	LAYER_8	19.30	10.00	8.00
	AD15	Pin(J3B1.A44)	(2040.00 3030.00)	52.00	38.00	LAYER_7_P	LAYER_6	53.70	10.00	8.00
	AD16	Pin(J3B1.A32)	(2040.00 3630.00)	52.00	38.00	LAYER_7_P	LAYER_6	53.70	10.00	8.00
	AD17	Pin(J3B1.B32)	(1840.00 3630.00)	52.00	38.00	LAYER_2_P	TOP	99.70	10.00	8.00
	AD17	Pin(J7A2.8)	(4033.00 3581.00)	60.00	46.00	LAYER_2_P	TOP	99.70	10.00	8.00
	AD18	Pin(J3B1.A31)	(2140.00 3680.00)	52.00	38.00	LAYER_2_P	TOP	99.70	10.00	8.00
	AD19	Pin(J3B1.B30)	(1840.00 3730.00)	52.00	38.00	LAYER_2_P	TOP	99.70	10.00	8.00
	AD2	Pin(J3B1.A57)	(2140.00 2380.00)	52.00	38.00	LAYER_9_P	LAYER_8	19.30	10.00	8.00
	AD20	Pin(J3B1.A29)	(2140.00 3780.00)	52.00	38.00	LAYER_7_P	LAYER_6	53.70	10.00	8.00
	AD21	Pin(J3B1.B29)	(1940.00 3780.00)	52.00	38.00	LAYER_2_P	TOP	99.70	10.00	8.00
	AD21	Pin(J7A2.7)	(4033.00 3690.00)	60.00	46.00	LAYER_2_P	TOP	99.70	10.00	8.00
	AD22	Pin(J3B1.A28)	(2040.00 3830.00)	52.00	38.00	LAYER_2_P	TOP	99.70	10.00	8.00

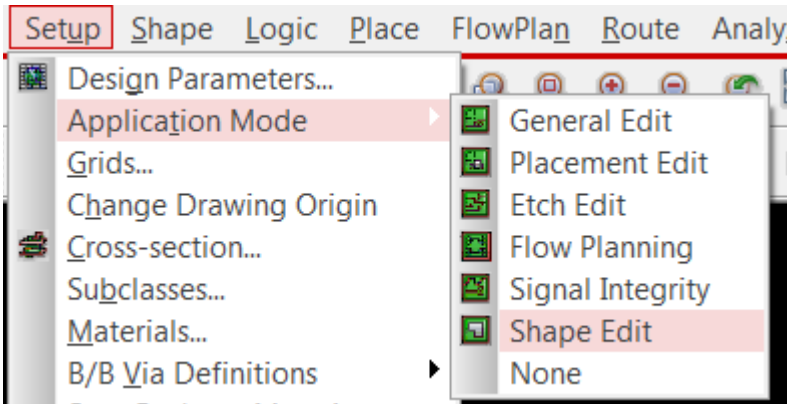
Shape Edit Application Mode

The Shape Edit Application Mode is a tuned editing environment primarily designed to increase efficiency with shape boundary editing. It is available in all backend PCB and Packaging products. This object-action environment simplifies the actions of sliding a shape edge, adding a notch or chamfering/rounding the corners. You will notice similarities with existing application modes but also new functional that allows customization of single pick and drag operations.

Selecting an Application Mode

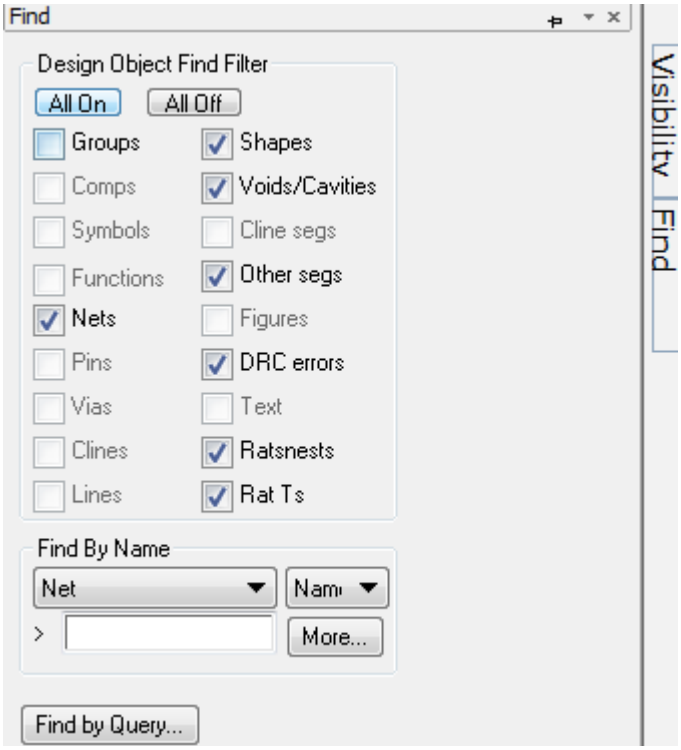
There are several methods available to select an Application mode inside Allegro PCB Editor or APD/SiP.

- *Setup – Application Mode*
- RMB – Application Mode
- Tool Bar Icon
- Lower Banner Field (Adjacent to Super Filter)



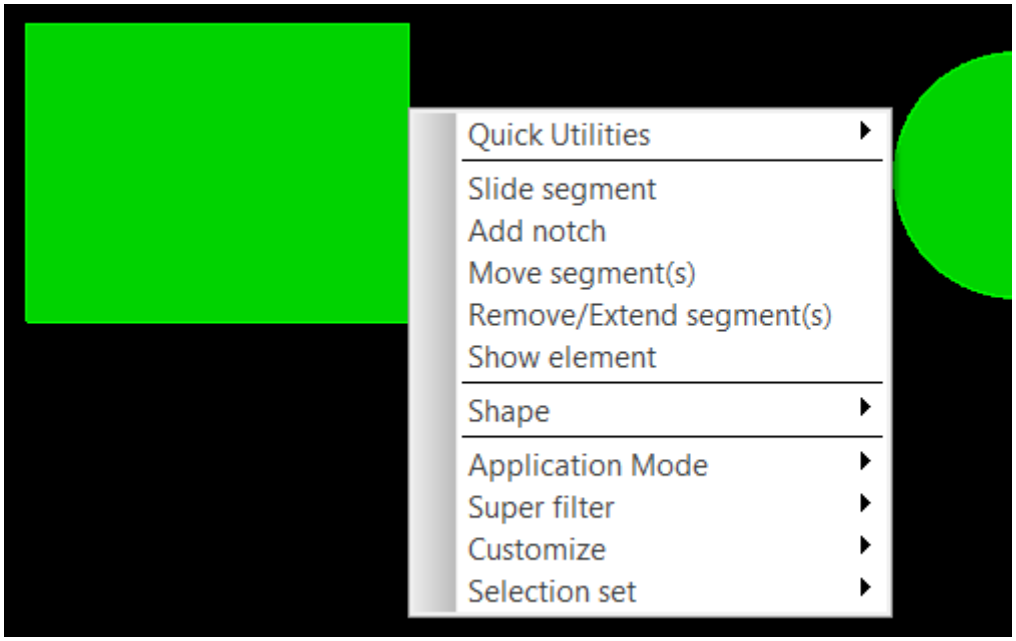
Find Filter Settings

The find filter is limited to the elements shown below to help optimize the editing environment.



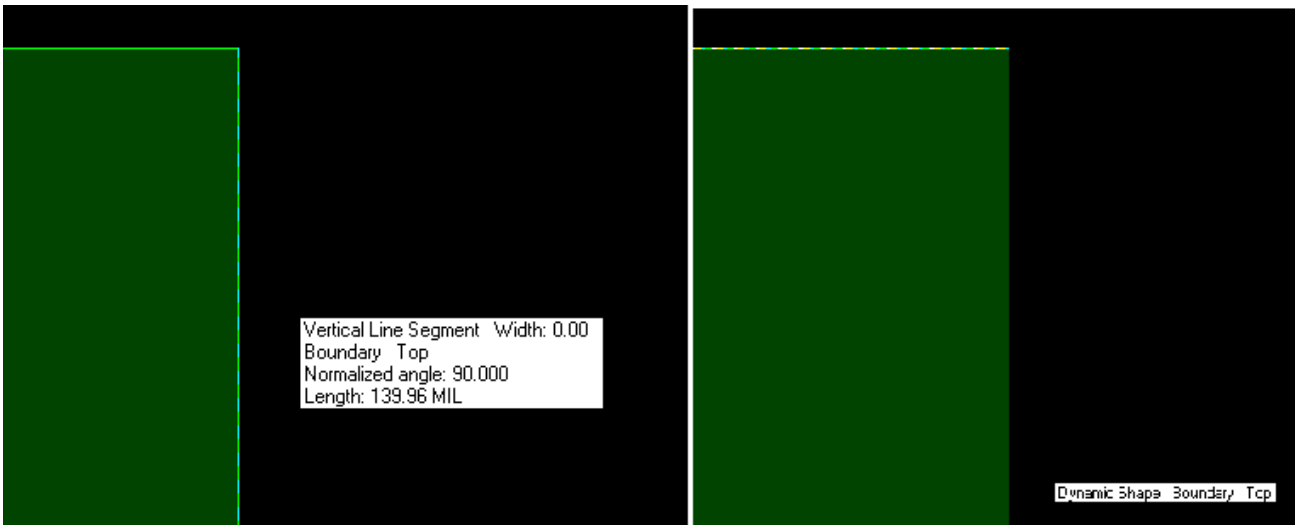
Context Sensitive Menu

Hovering over a shape segment (edge) produces the following context-sensitive menu.



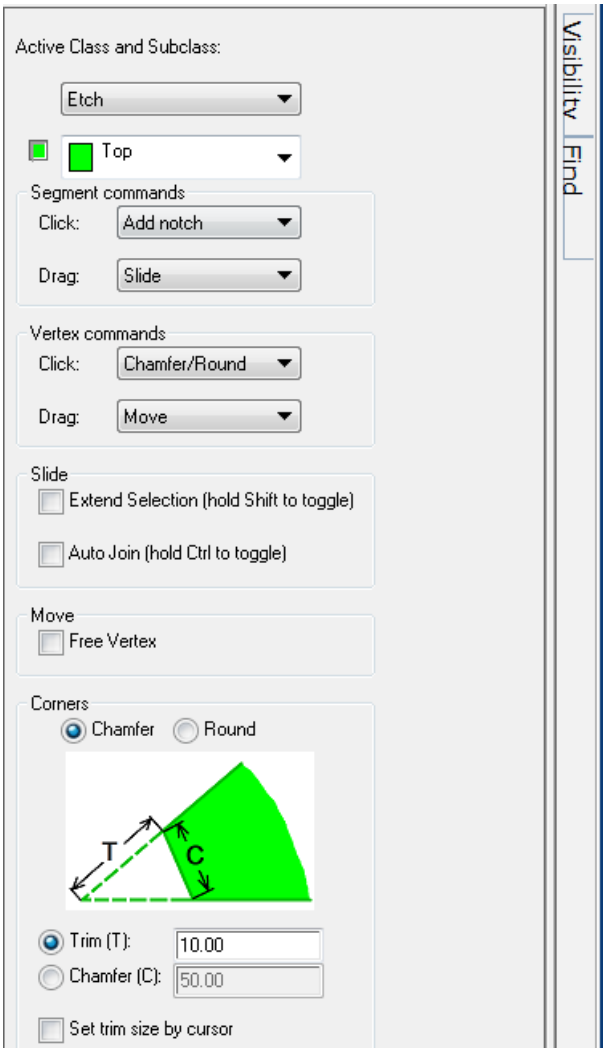
Toggle between elements

Use the TAB key to cycle between elements on your cursor. In the following example, hovering over the shape edge (left graphic) provides datatip info about the line segment. Click the TAB key to cycle to the shape element (right graphic). Context sensitive menus will vary based on the highlighted element.

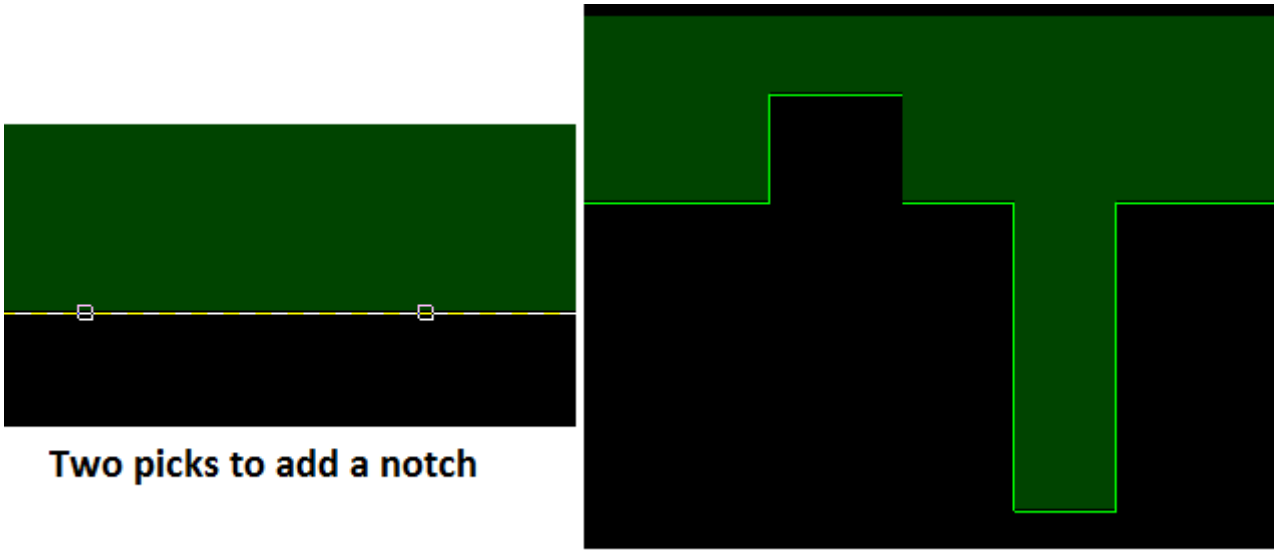


Best Practices for Shape Editing

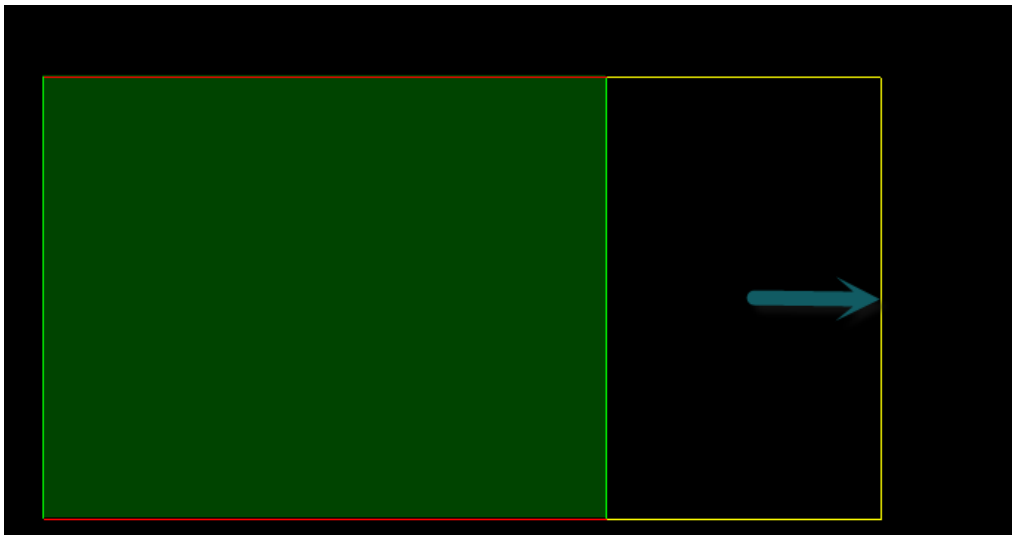
You can customize settings in the *Options* panel for the Click, Drag, and Vertex operations. Based on the settings as displayed in the following image, there is no need to access the main toolbar or top level menus for basic shape boundary editing.



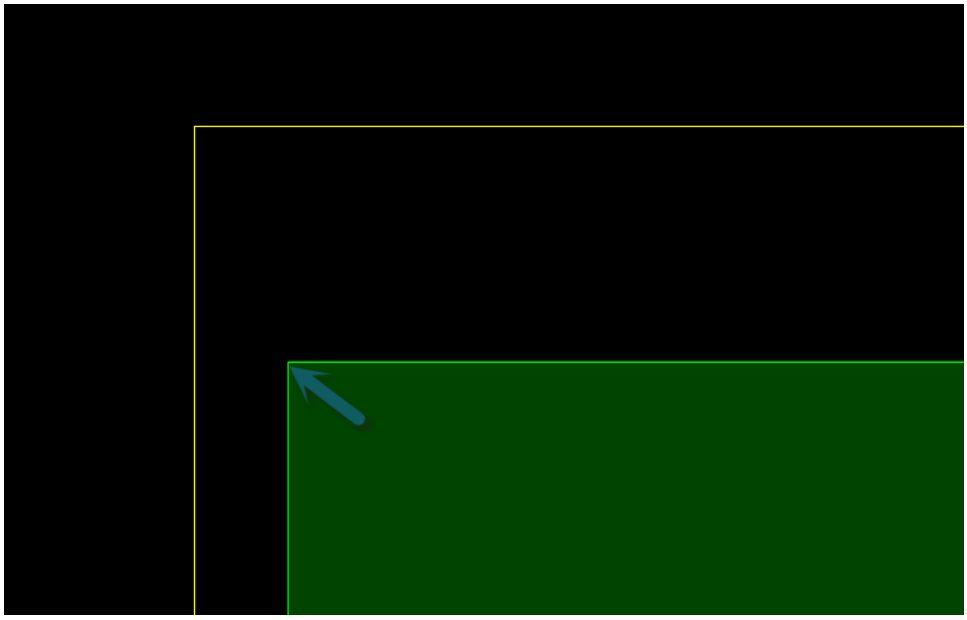
- Two picks on a shape segment result in the creation of an inward or outward notch; based on your cursor movement.



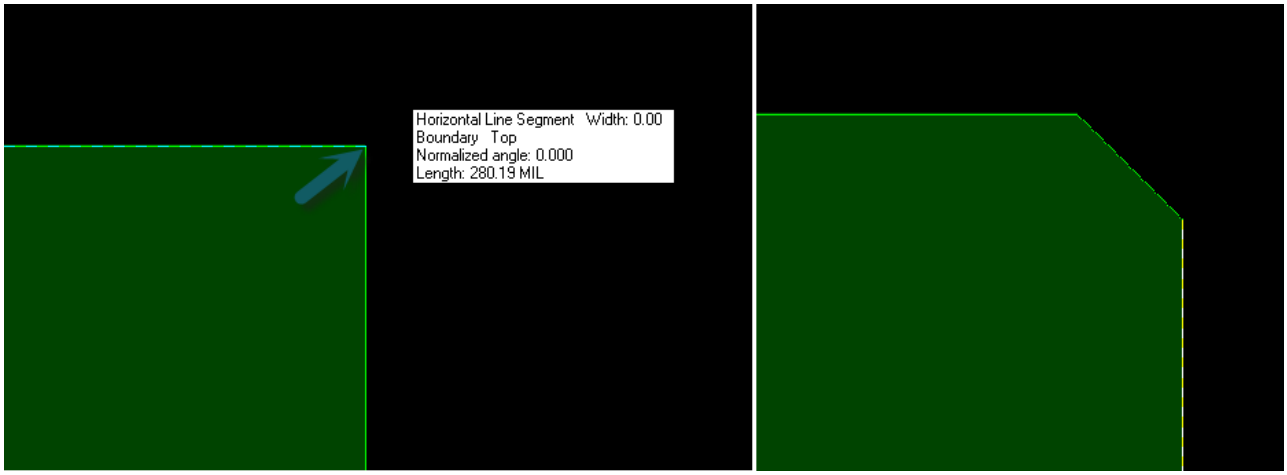
- A long mouse button press while hovering over a shape segment invokes a slide operation.



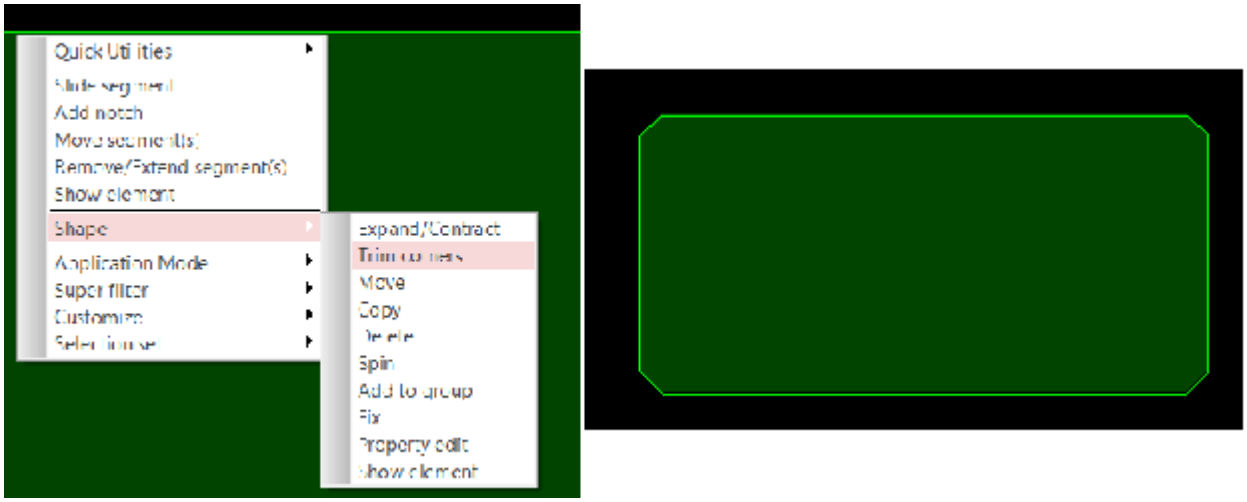
- A long mouse button press while hovering over a vertex location performs a two-segment move operation.



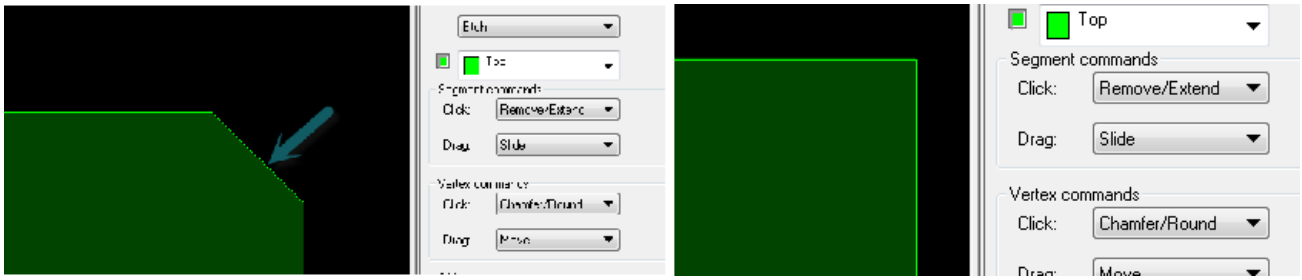
- Clicking on a vertex location results in a chamfer corner trimmed to10 mils (actual segment length = 14.14 mils)



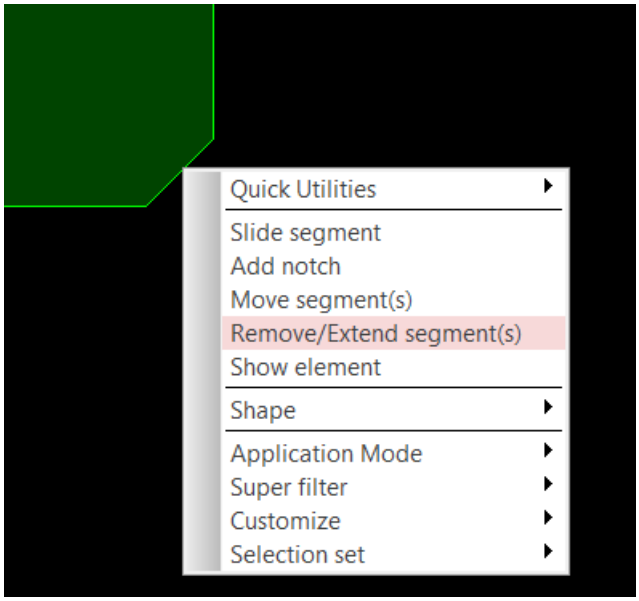
- To chamfer all corners, hover over a shape segment and then right-click to access the Trim corners command. <<The text on the images is not at all clear even after zooming in. This would look awful in the htmls and the PDF."



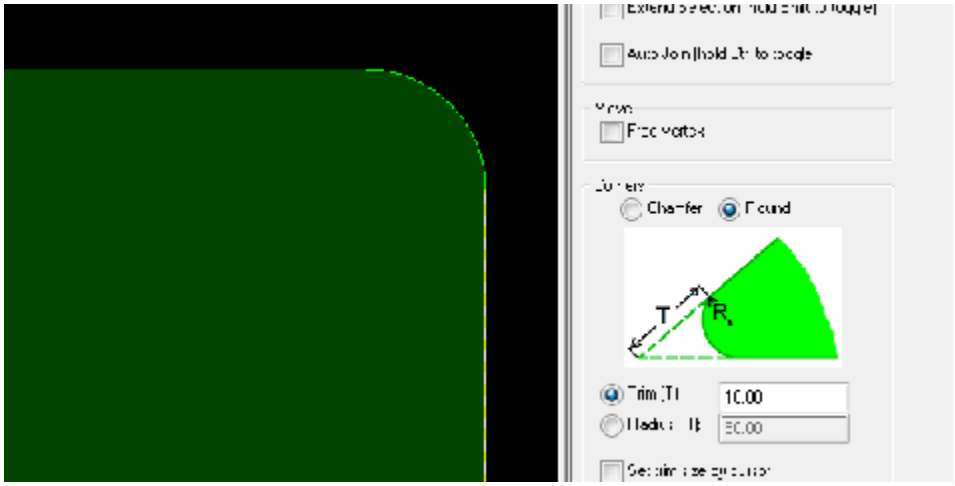
- To convert a corner back to orthogonal, change the *Click* setting to *Remove/Extend* and then select the chamfered segment.



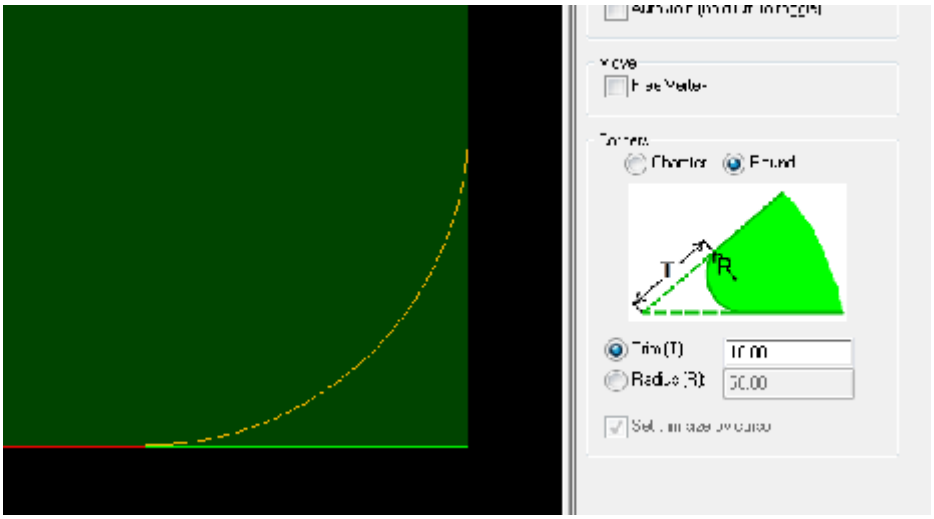
- Alternatively, one can hover over the chamfered edge and use the right-click context menu to access the *Remove/Extend segments* command.



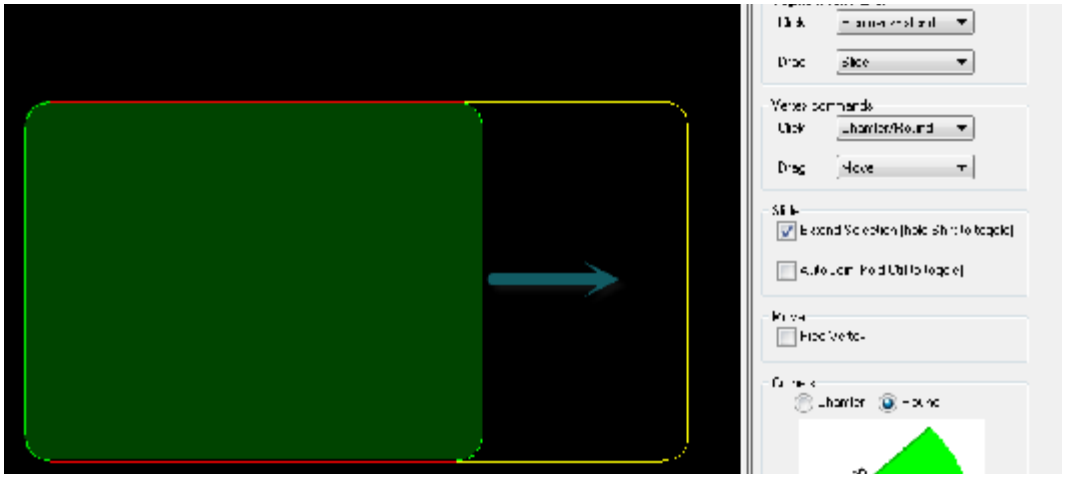
- To round a corner, change the *Corners* setting to *Round* and then select the vertex location.



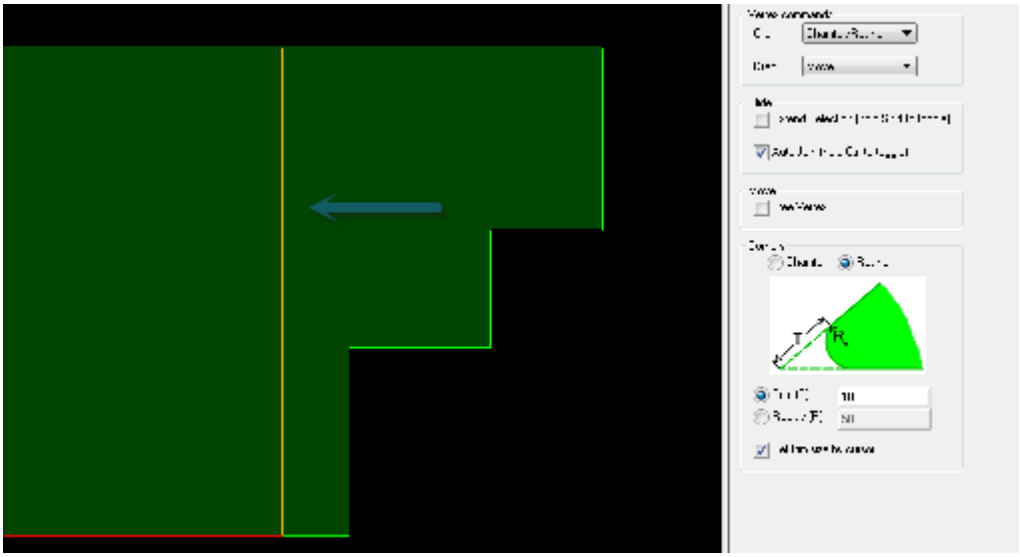
- To adjust a corner using mouse, enable *Set trim size by cursor* option, and then move your mouse to control the chamfer or round size.



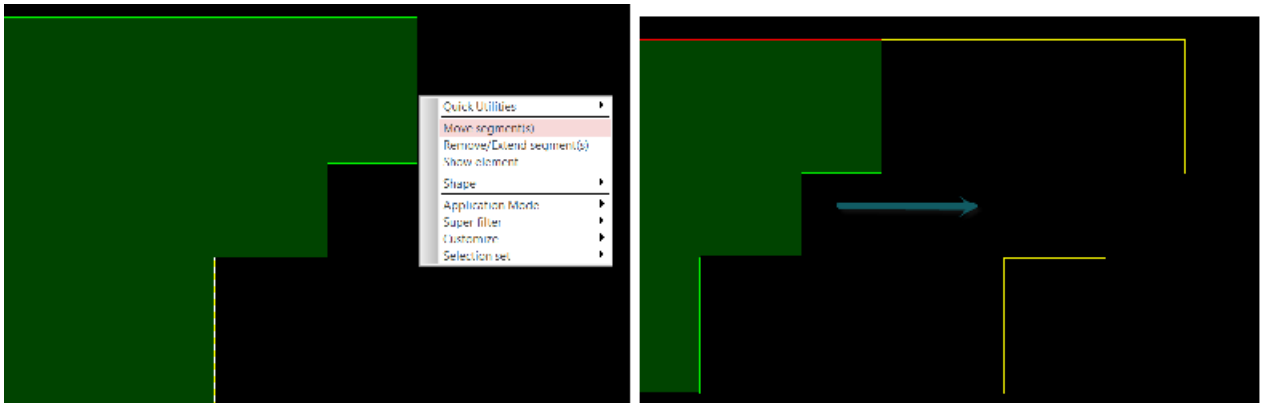
- To slide a shape segment and its chamfered or rounded corners, enable *Extend Selection* option and then click or drag to perform the 3 element slide operation. A similar model is used with the etch edit slide function.



- To join the edges of a multi-edge shape, enable *Auto-Join* option and then slide one of the segments.



- To move and maintain the integrity of the multi-edge side of the shape, press the Ctrl key and then select the three vertical segments. Hover over any one of the highlighted segments and then use the *Move Segments* command.
  - Moving segments is not linear. Use the *ix* command to set a distance. For example, type *ix 100* in command window to move the segments 100 mils to the right.

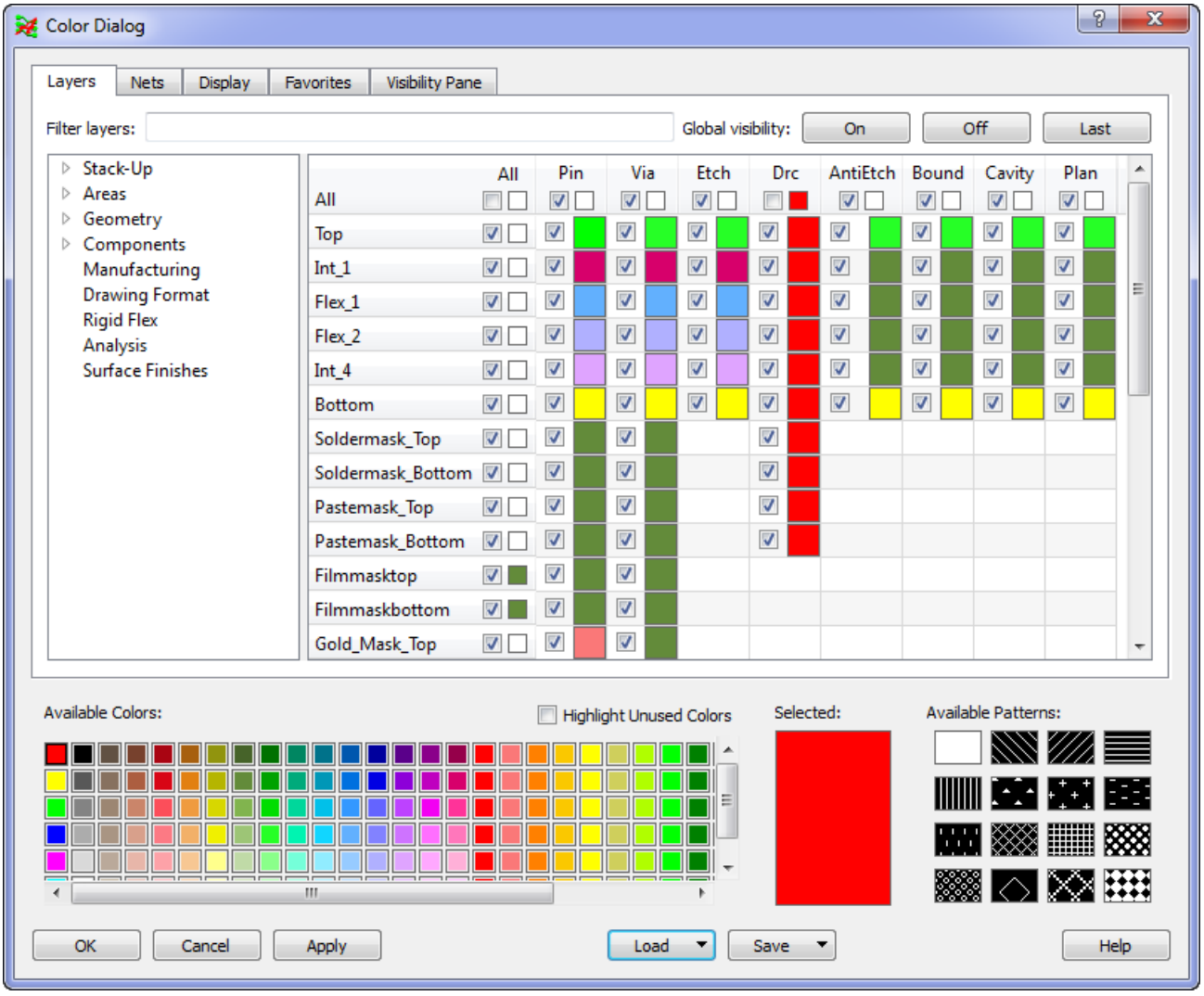


Color Dialog Enhancements

Information is at the heart of every design and as such changes have been made to the Color Dialog that will make it much easier and more efficient for Designers to use.

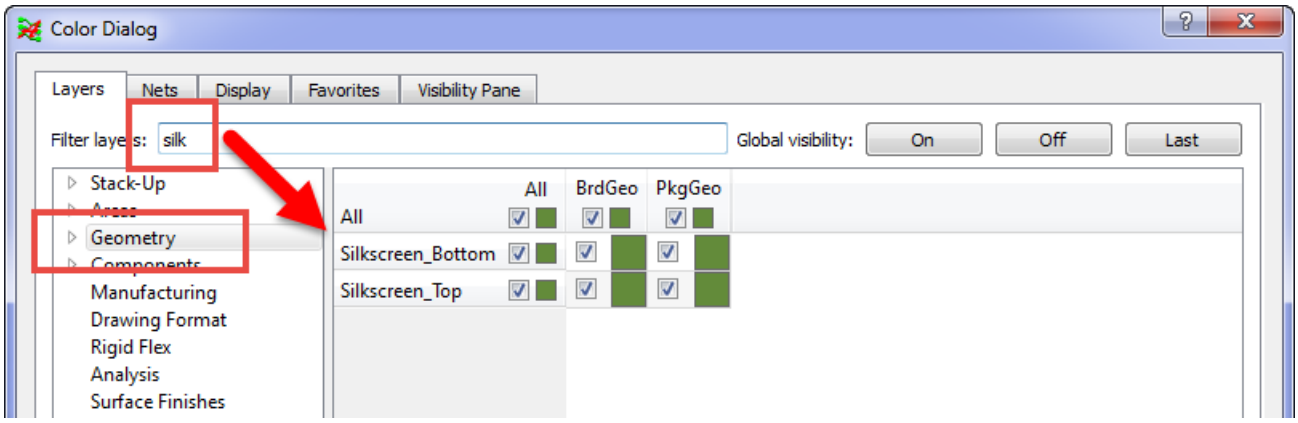
Fresh New Look

The Color Dialog now uses a tabular approach and categorizes the major features into their own tabbed pages named *Layers*, *Nets*, *Display*, *Favorites*, and *Visibility Pane*.



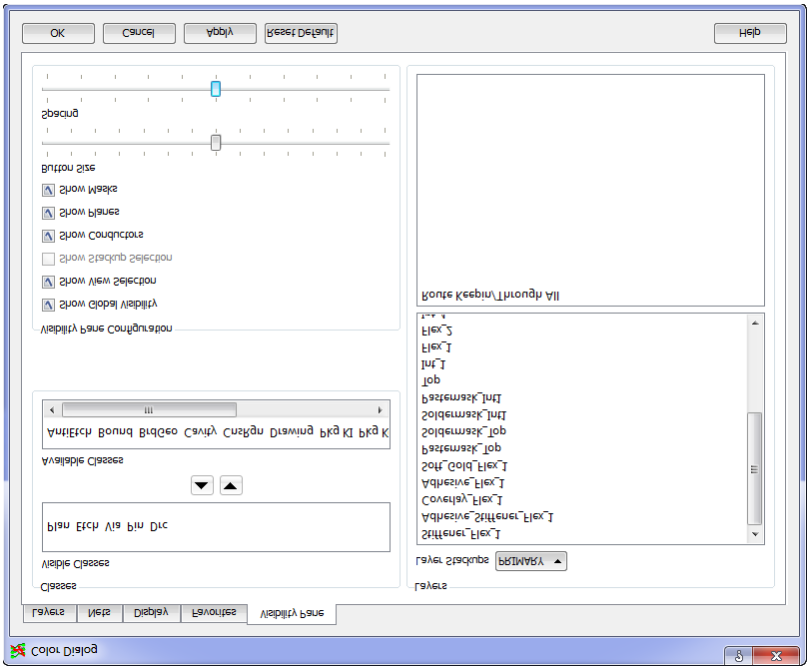
Searching Subclass Layers

The Layers tabbed page has been updated to include a search for specific or groups of subclass layers. The search box is case insensitive and a “*” wildcard is implied both as a prefix and a suffix to the specified text.



Visibility Pane Tab

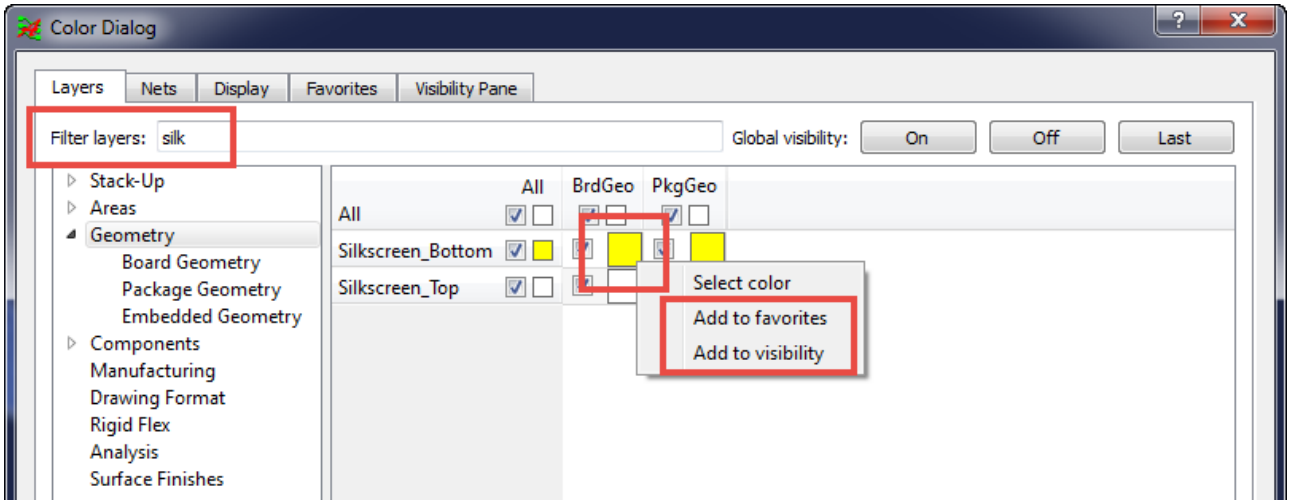
The following image shows the detailed information and options on the Visibility Pane tabbed page.



Viewing Subclasses in Favorites or Visibility Pane

After searching for a specific or a group of subclass layers, right-click and add those subclass layers either to Favorites or to Visibility Pane.

Note: When adding subclass layers to Visibility Pane in a design with multiple stackups, the subclass layers are added to the stackup in view on the Visibility Pane tab of Color Dialog.



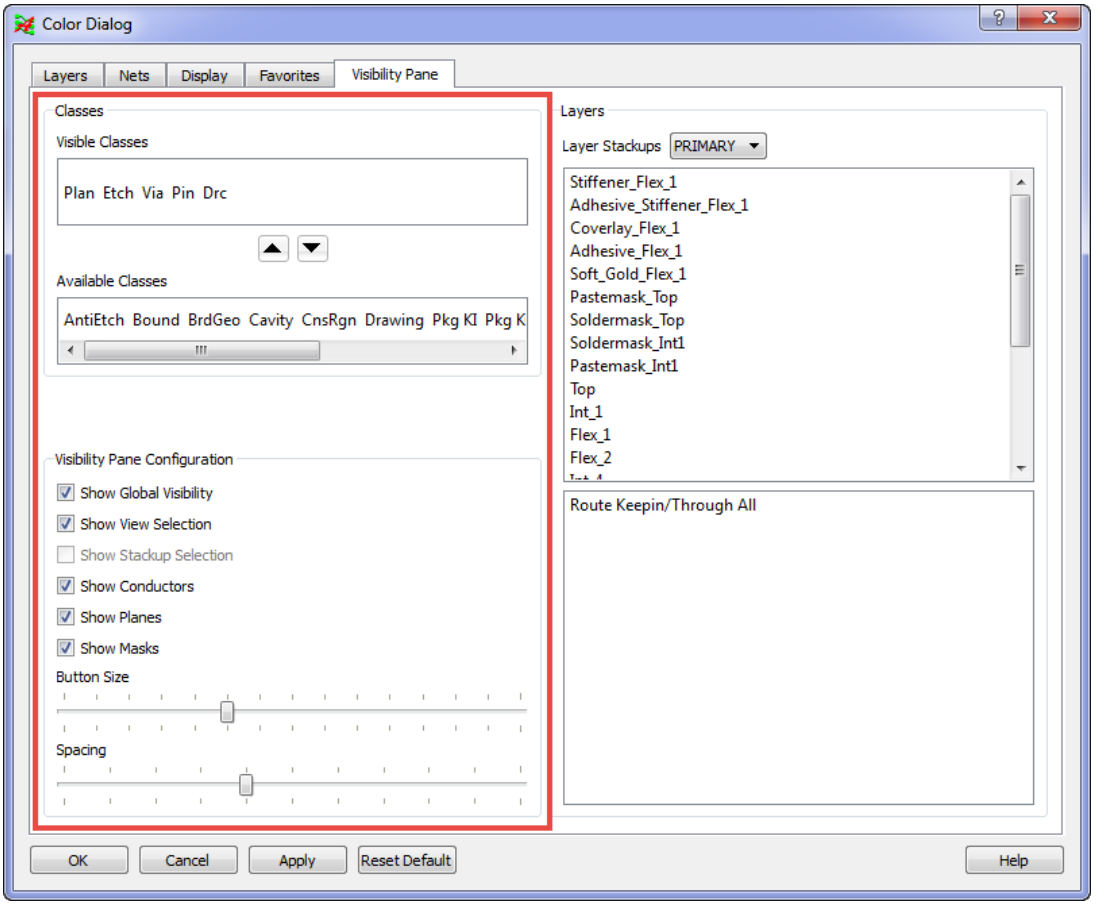
Visibility Pane Refinements

The *Visibility* pane provides quick access and efficient control of the layer content. Instead of a single stackup approach, Visibility Pane now provides quick access to easily configure and view different Zone stackups. This pane now has the added benefit of providing access and control over layers other than the conductor layers. Additionally, you can easily switch to a single layer view and quickly review individual conductor layers.

You can customize the options in the *Visibility* pane from the Visibility Pane tabbed page. Classes added to the Visible Classes section become vertical columns on the *Visibility* pane. In the Visibility Pane Configuration section you can toggle between showing and hiding the parts of the *Visibility* pane. The sliders at the bottom of the form control the size and spacing of the color boxes on the *Visibility* pane.

Configuration settings altered on the left side of the following image are saved as User Environment settings and persist between designs and sessions. Layers added to the right

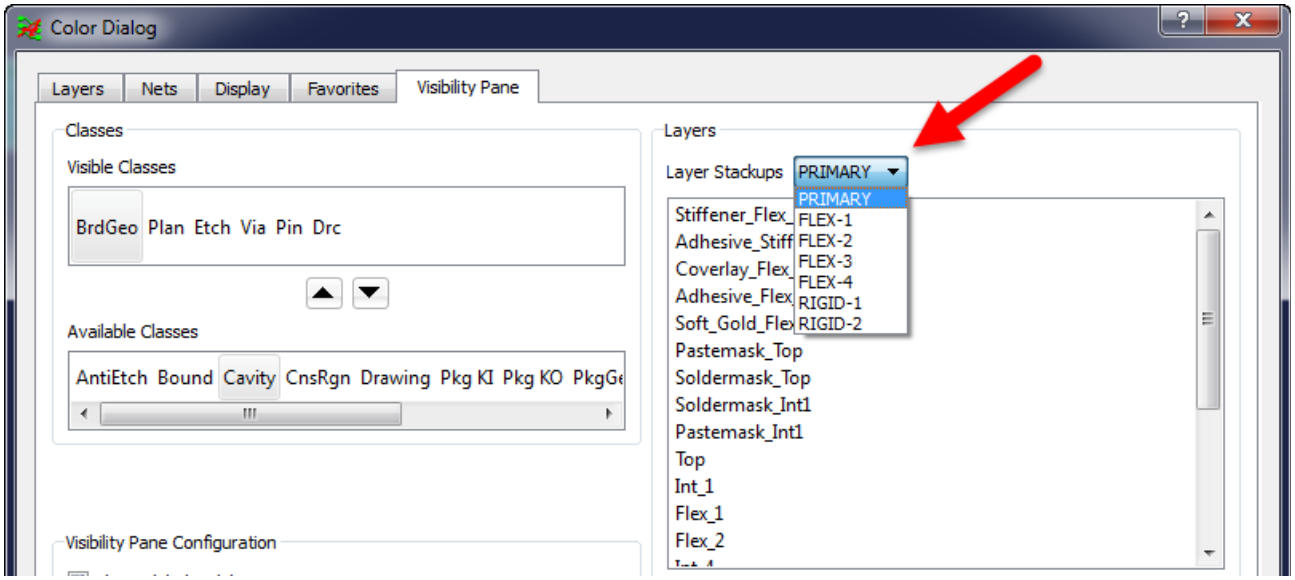
side of the following image are design dependent and are not present on the *Visibility* pane when another design is loaded.



Stackup Customization

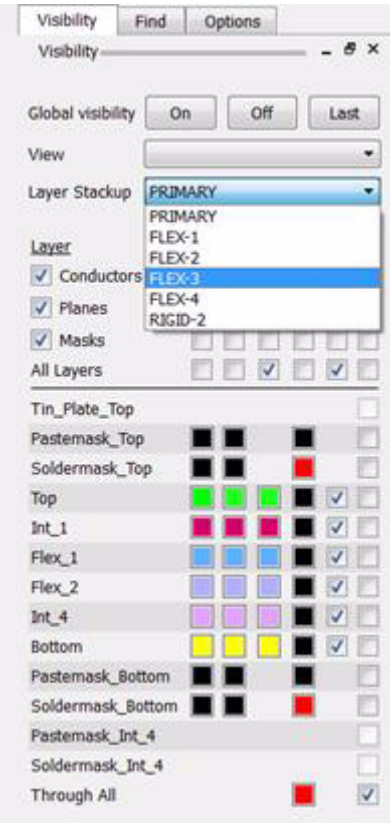
Layer stackups can be independently enhanced with the addition of subclass layers. Subclass layers added from the Layers tab are added to the Layer Stackup in view. The

stackups illustrated in the following image are generated in the Cross Section dialog and are also viewable as individual entities on the Visibility pane on the canvas:



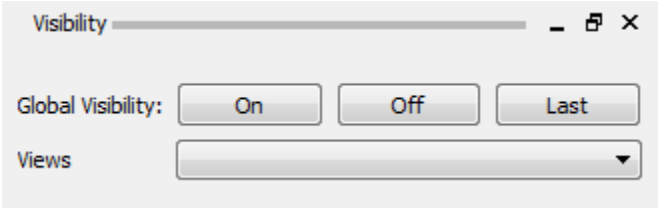
Stackup Viewing

View layers of different stackups independently using the Layer Stackup drop-down list.



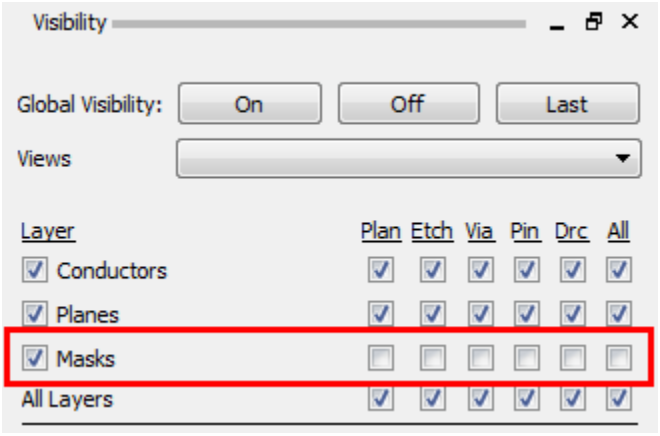
Global Visibility

The ability to globally turn on or off the visibility of elements has been duplicated on the *Visibility* pane. You no longer need to launch Color Dialog for this.



Mask Layers

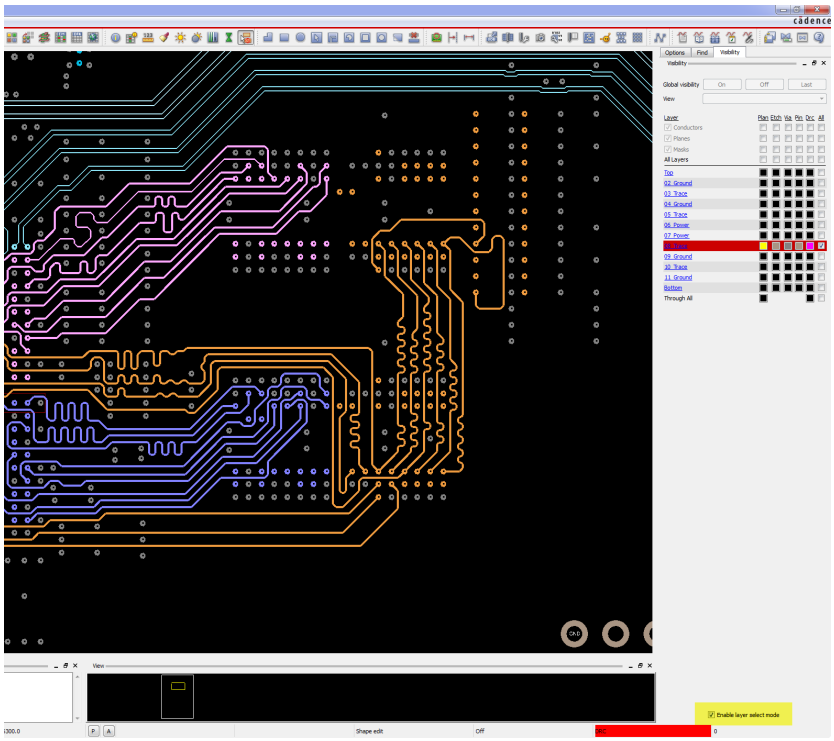
Control of Mask Layers added in the cross section has also been added to the *Visibility* pane.



Layer Select Mode

When the *Enable layer select mode* option is selected at the bottom of the *Visibility* pane, the Conductors layer names change to HTML links. You can click a single link to view the

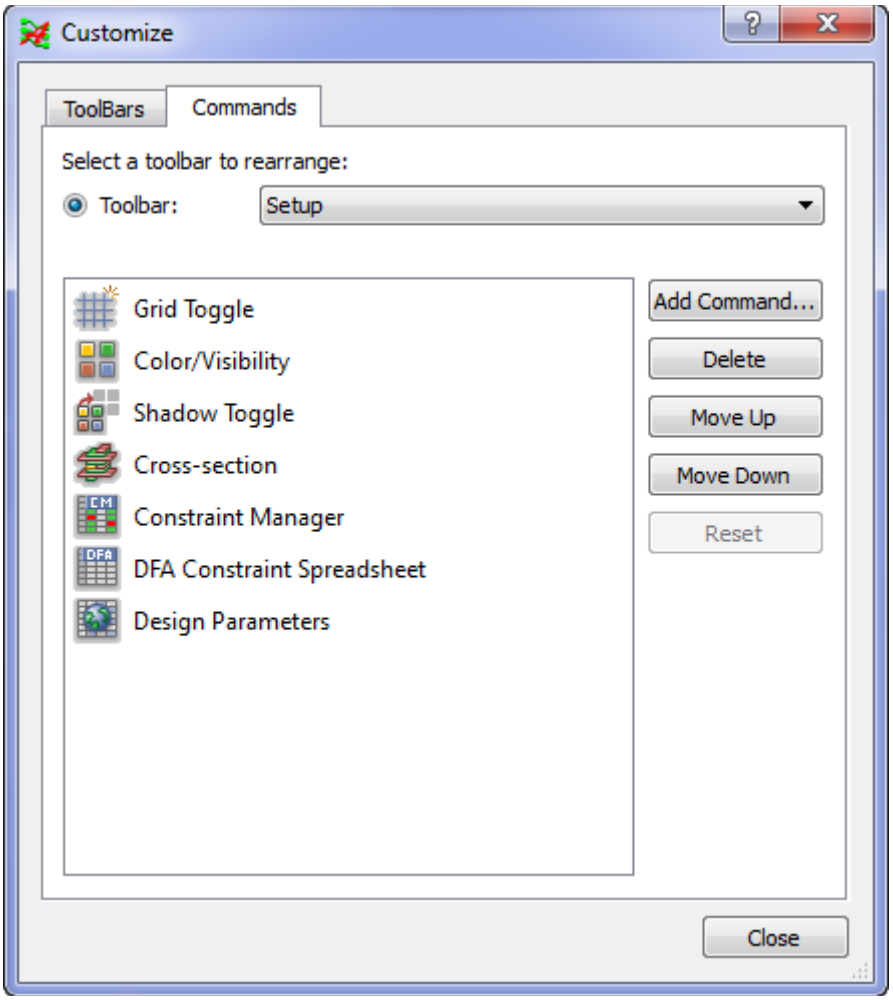
corresponding layer on the canvas or CTRL + click on more than one layers to view multiple layers.



Canvas Enhancements

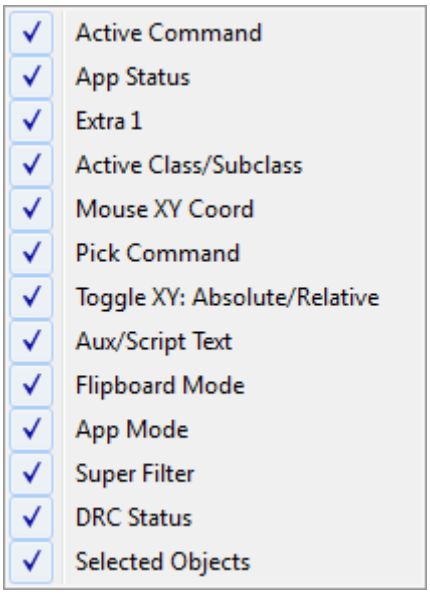
Customizable Toolbars

Toolbars can now be customized and personalized. New, user-defined toolbars can also be added and custom scripts can also be assigned to an icon.



Status Bar – Show/Hide Selections

You can now customize your workspace by showing or hiding the sections along the status bar. A right-click menu along any portion of the bottom status bar now brings up the configurable selection dialog. Select or deselect the sections as required.

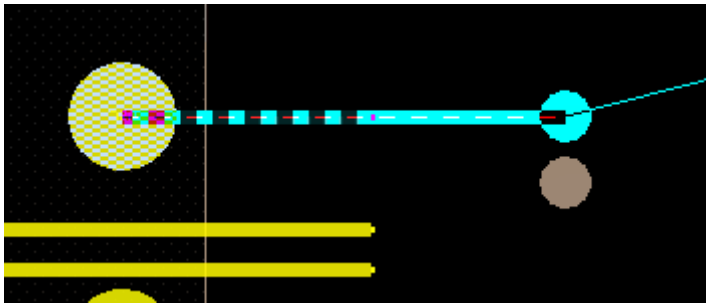


High Speed Interconnect Enhancements

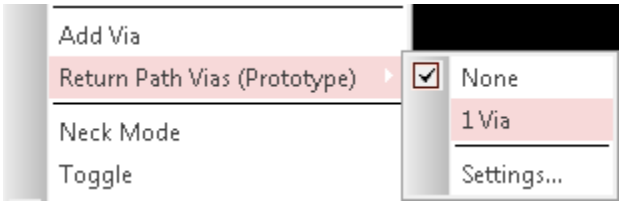
Single Net Return Path Vias

Licensing - Requires Allegro PCB Designer (Highspeed Product Option). This is an Unsupported Prototype.

Return Path Via support for differential pairs was introduced in the SPB16.6-2015 release. Based on customer feedback, this functionality is now extended to support single net routing. To access the functionality, choose *Return Path Vias (Prototype)* from the pop-up menu on right-click from the *Add Connect* command.



Return Path Vias feature is available as a right-click option during Add Connect of a single net. It provides a quick way to add one return path via next to signal via during routing.

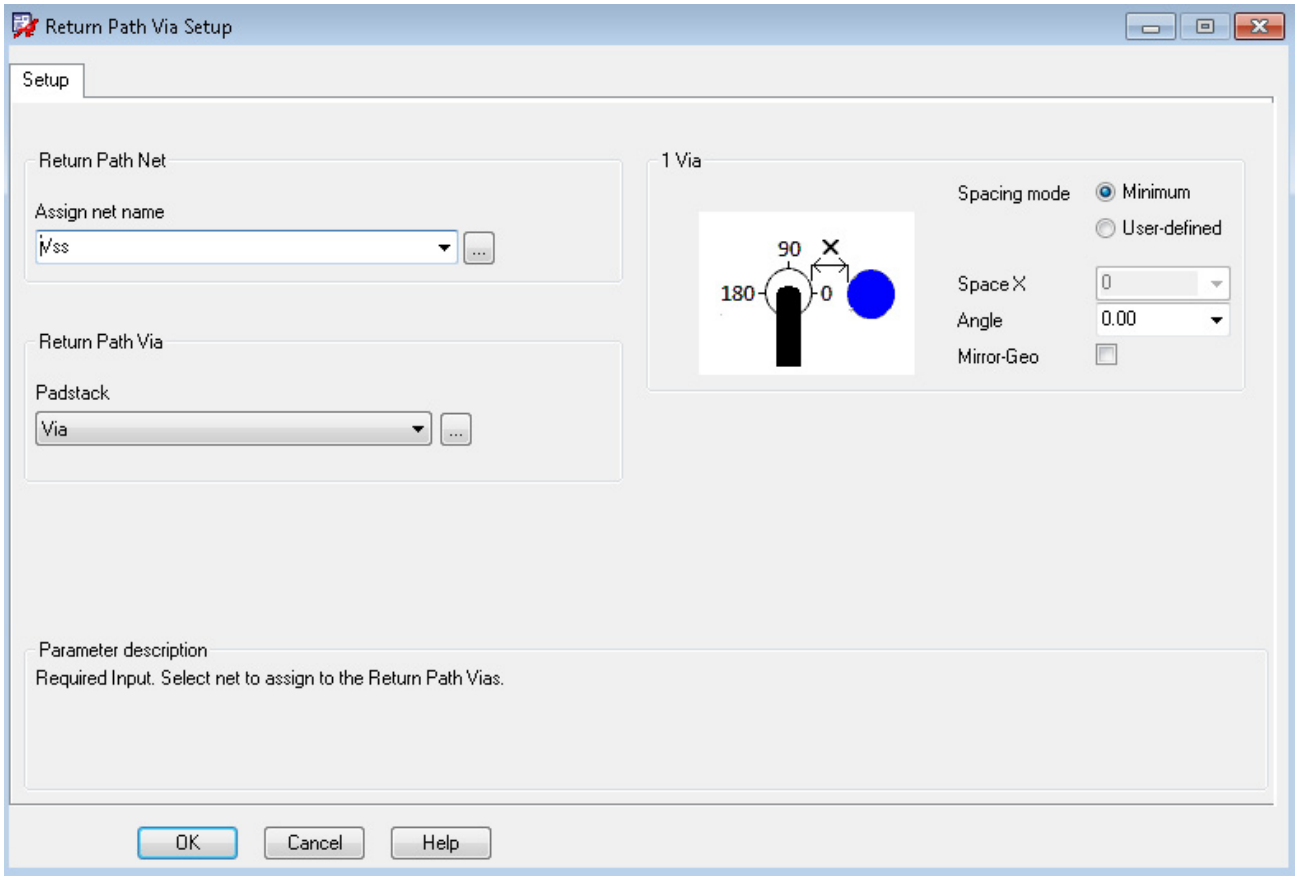


Before selecting one of the *Return Path Vias* options, set up the net and padstack to be used for the return path via. Default spacing is set to minimum.

You can select one of the following Return Path Vias options for a single net:

- *None* – No return path via is added.

- *1 Via* – Adds 1 return path via next to signal via



Tabbed Routing

Tabbed routing is a new routing strategy in which trapezoidal shapes called tabs are added to parallel traces to control impedance in the pin field/breakout region, and crosstalk in open field region. This enables longer trace lengths and use of smaller trace spacing.

Note: This feature requires Allegro PCB Designer (High Speed Product Option). This is an Unsupported Prototype.

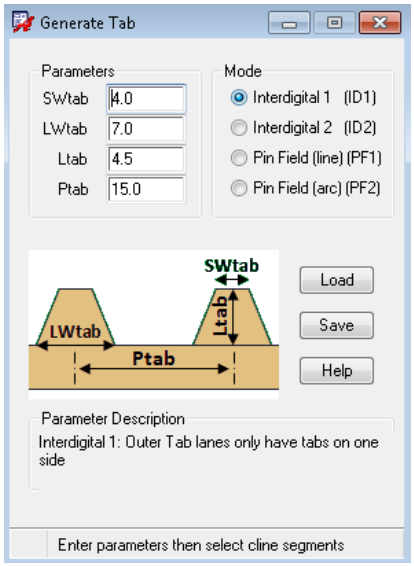
Menu Location for Suite of Commands

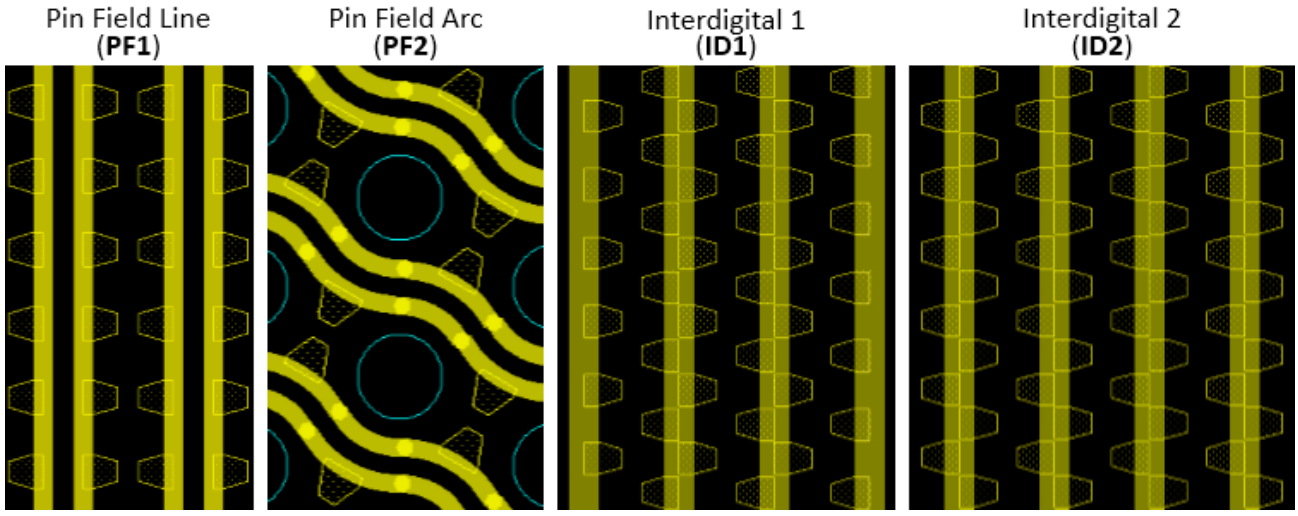
Route – Unsupported Prototypes – Tabbed Routing

- *Generate Tab*
- *Move Tab*
- *Delete Tab*
- *Analyze*

The *Generate Tab* command generates trapezoidal tab shapes on trace segments for controlling impedance and crosstalk. Perform the following tasks to generate tabs:

1. Select the mode.
2. Specify tab size/pitch values under Parameters.
3. Select cline segments to generate tabs.




Pin Field Line
(PF1)
Pin Field Arc
(PF2)
Interdigital 1
(ID1)
Interdigital 2
(ID2)

Via Structures

The `create via structure` command allows you to create two types of via structures – standard and high speed. There is also an option available to automatically export an XML file, which can be used to import/export via structure definition in other PCB/SiP database and Sigrity 3DEM (High Speed only).

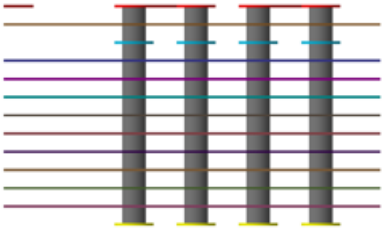
Note: Requires *Standard Via Structure* option and is available with all Allegro layout editors. High Speed Via Structure requires Allegro PCB Designer (*Highspeed Product Option*).

Standard Via Structure

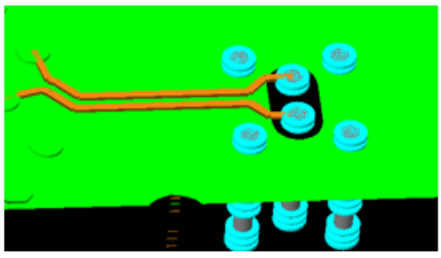
- Menu: *Route – Via Structure – Create – Standard*
- Target Use Model: Single net trace/via structures and Fan-out
- Supported Objects: Traces, Vias
- Connectivity: Need all vias to be physically connected (single net)

High Speed Via Structure

- Menu: *Route – Via Structure – Create – High Speed*
- Target Use Model: Differential pair via transitions with Return Path Vias and custom plane voids
- Supported Objects: Traces, Vias, Static Shapes (no voids), Route Keep out
- Connectivity: Multi net
- High Speed Via structures must be placed similar to components



Standard Via Structure



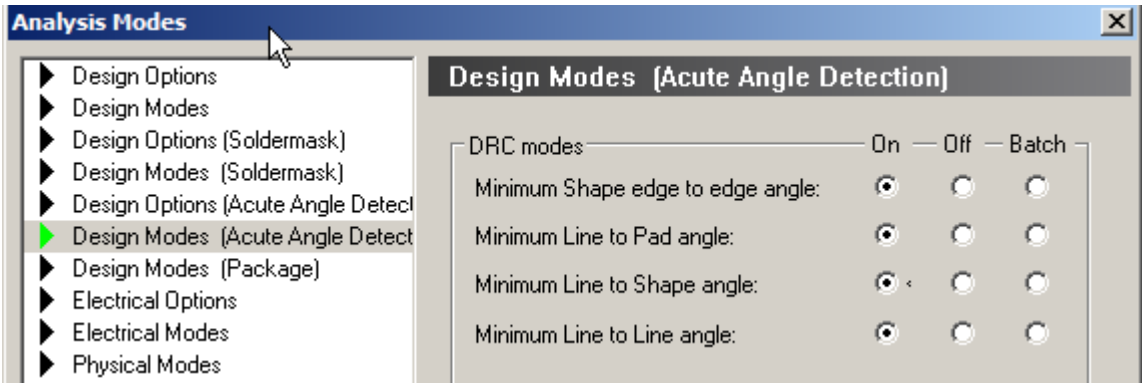
High Speed Via Structure

PCB Editor now has the same via structure use model as Cadence SiP Layout. Via structures are no longer limited for use with *Create Fanout* in PCB Editor. Some new via structure commands added to PCB Editor include:

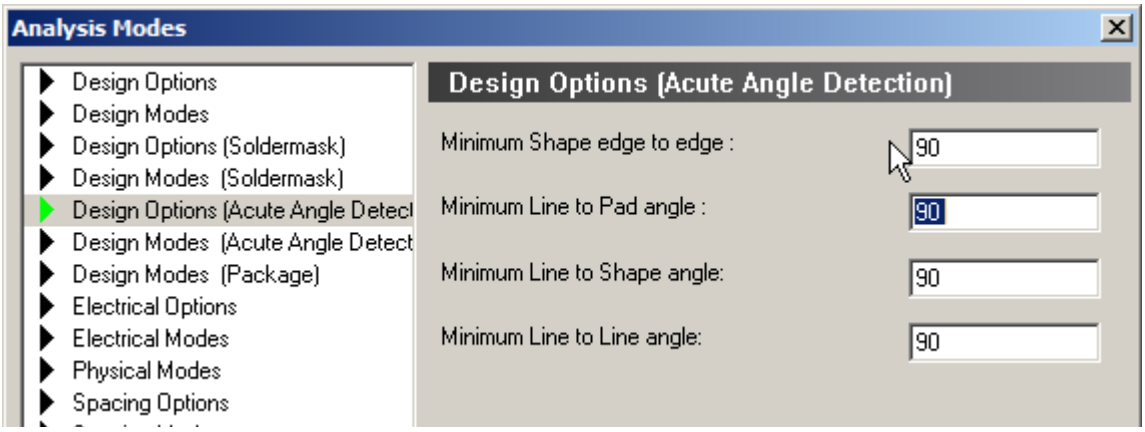
- *Create*
- *Add*
- *Replace*
- *Replace Via with Via Structure*
- *Redefine*
- *Refresh*
- *Disband*

Acute Angle Detection

A suite of four angle based checks are introduced in 17.2 as Design Level DRCs. You can enable acute angle checks using *Setup– Constraints – Modes* menu and then selecting the *Design Modes (Acute Angle Detection)* tab in the *Analysis Modes* form. You can set the DRC mode to *On-line*, *Off*, or *Batch* modes.



Acute angle DRC check values are set using *Setup – Constraints – Modes* command and then selecting *Design Options (Acute Angle Detection)* tab in the *Analysis Modes* form. The default values for this check are set to 90 degrees, but may be set to any angle between 0 and 90 degrees.



When an Acute Angle DRC is viewed, the DRC marker contains the characters *AA* to identify the DRC as an Acute Angle violation.

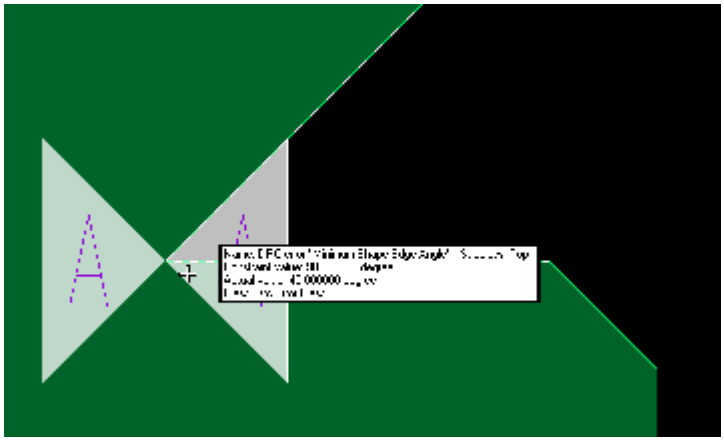
The Acute Angle DRC Checks include:

- Minimum Shape Edge to Edge
- Minimum Line to Pad Angle

- Minimum Line to Shape Angle
- Minimum Line to Line Angle

Minimum Shape Edge to Edge

The copper shape outline has an acute angle of less than the angle specified.



Minimum Line to Pad Angle

Cline to pad entry has created an acute angle of less than 90 degrees.

Minimum Line to Shape Angle

The cline to copper shape intersection has created an acute angle of less than 90 degrees.

Minimum Line to Line Angle

The cline to cline intersection has created an acute angle of less than 90 degrees.

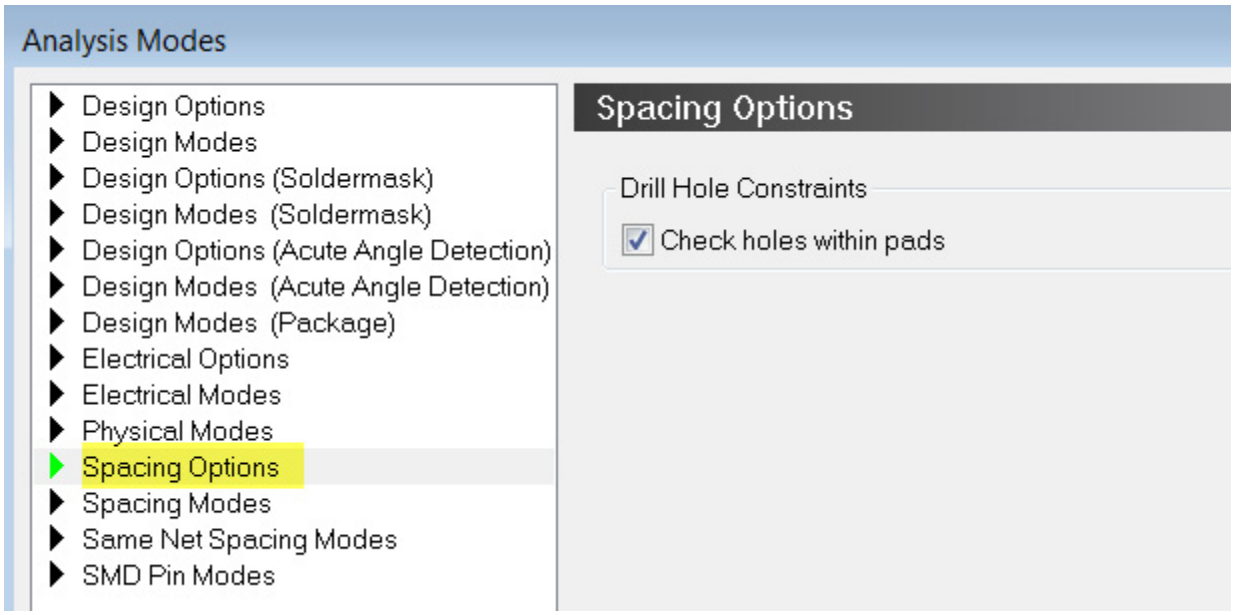
Drill Hole DRC

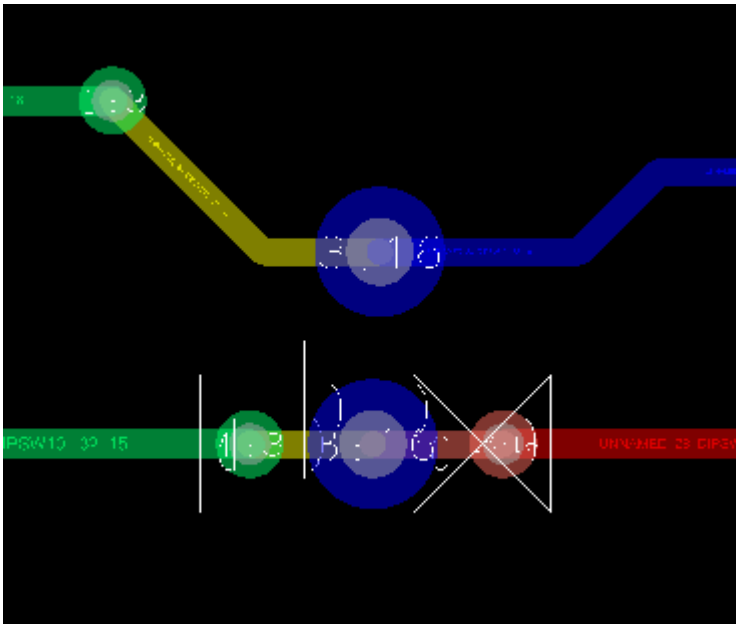
Drill Hole checks were introduced in 16.2 to support the unused pad suppression feature at that time.

In 17.2, a new *Spacing Options* section is added to the *Analysis Modes* menu to host a toggle control for this purpose. The option is labeled *Check holes within pads*.

When the toggle is ON, drill-hole checks are run using the drill hole explicitly. The presence of pads associated with the drill hole is not relevant in this mode of the DRC calculation and the drill is checked whether or not a pad is present.

When the toggle is OFF, the drill-hole checks are only relevant when the pad is suppressed or undefined exposing the bare hole. This is the default configuration and is compatible with previous releases.





IDX Enhanced Features

The 17.2 release exposes enhanced feature support in the EDMD Schema (IDX). These features are supported by the IDX format, but may not be supported by the specific MCAD tool in the your environment.

Important

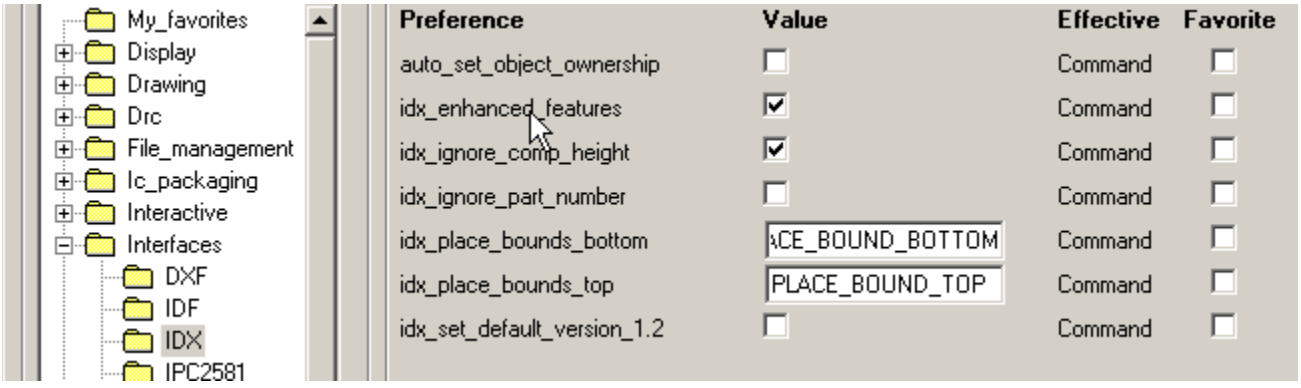
Before enabling these features, verify with your MCAD provider which features are supported by their tools.

The supported enhanced feature set includes:

- User Preference Settings
- IDX Properties
- Component Symbol Support
- User Defined Layer and External Copper layer Support
- Hole/Slot support
- IDX Compare Utility

User Preference Settings

To enable the enhanced IDX features, the user preference setting `idx_enhanced_features` must be enabled in the *User Preferences – Interface – IDX* category. The enhanced features defined in this section should be confirmed with the MCAD vendor before proceeding.



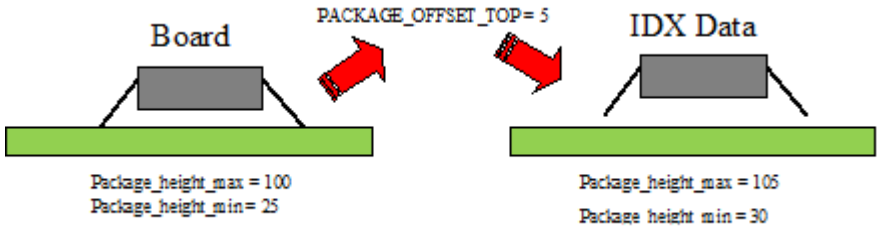
The IDX Out function indicates if the *STANDARD* or *ENHANCED* mode is defined in the user preferences setting in the upper right corner of the export form.

IDX Properties

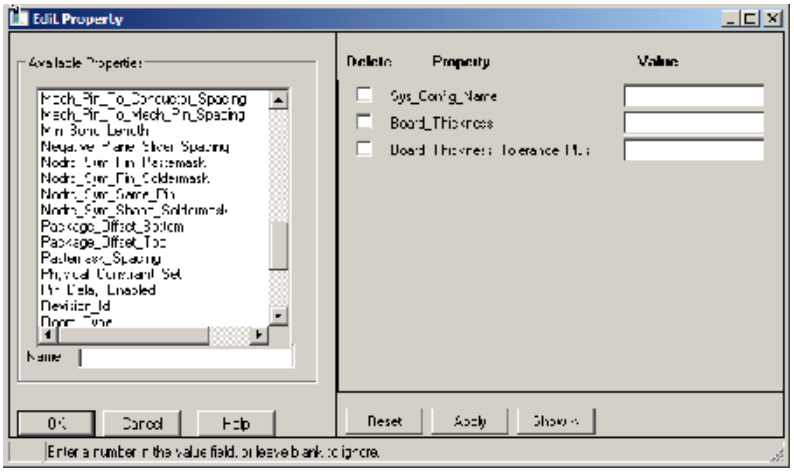
The following new properties were added to support the new or enhanced features for IDX:

- Package_Offset_Bottom, Package_Offset_Top (Board Drawing Properties)

  Each of these properties uses a value that offsets the component height across the surface of the board to typically account for paste mask thickness. The property value is added to the component include, PACKAGE_HEIGHT_MIN and PACKAGE_HEIGHT_MAX, height property or default height values when the exporting IDX. When assigned, the offset is also applied to the Symbols when DRC height checks are active.



The PACKAGE_OFFSET_TOP sets the top offset, and the PACKAGE_OFFSET_BOTTOM sets the bottom placement offset value. The values are independent of each other.



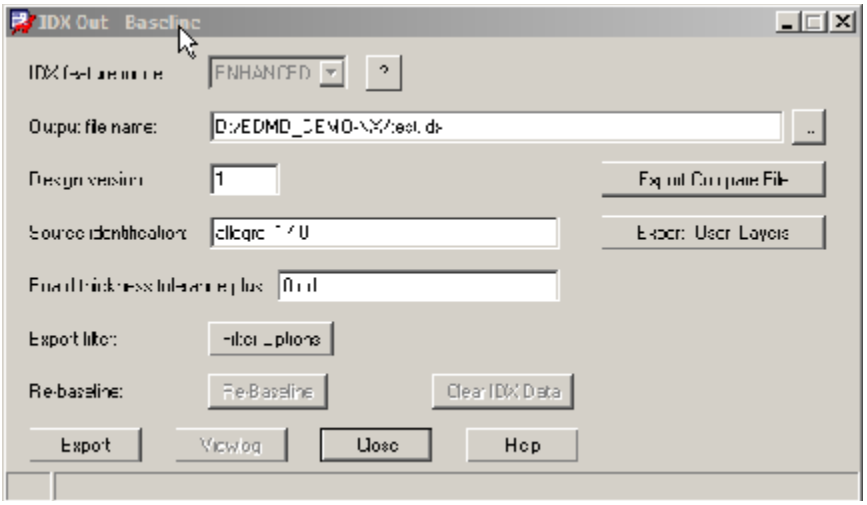
- IDX_OTHER_OUTLINE (filled, non-filled shapes)

  This property can be assigned to any user-defined shape to exchange the shape with the MCAD tool. This property allows a bi-directional exchange of the shape if the user-defined shape is not originally defined in the MCAD tool.

- BOARD_THICKNESS_TOLERANCE_PLUS (Board Drawing Property)

  This property value can be assigned in the IDX Out form. The value defined in drawing units passes a plus tolerance of the overall board thickness as an attribute in the IDX data

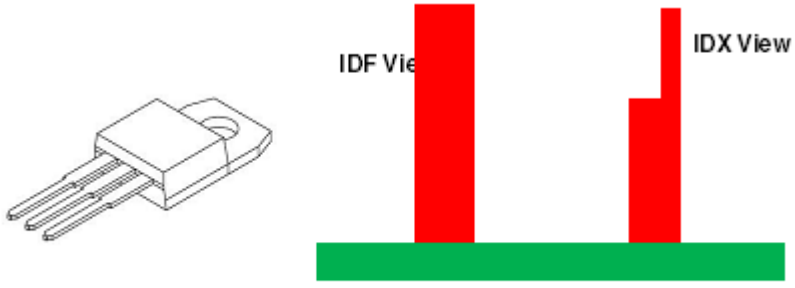
file to the MCAD tool. This value does not impact any data within the board drawing database.



Component Symbol Support

- Multiple Height Export

  Enhanced IDX support for symbols in Allegro PCB Editor 17.2 includes the export of multiple PLACE_BOUND_TOP/BOTTOM defined in the package symbol. Previous exports of IDX (as well as in IDF) combined all package boundaries into one unified geometry, and then appended the maximum height value. For enhanced IDX, each geometry and associated height values are exported individually within the package symbol definition.



- Pin One Identification

  Enhanced IDX support for symbols in Allegro PCB Editor 17.2 includes the export of pin one identification. If a component is exported, and the PKG_PIN_ONE property is

assigned to pin one of the package symbol, the pin location is passed with a pin one attribute to assist in the identification of the primary pin location. The pin one identifier may be used to verify placement orientation between the ECAD and MCAD libraries.

If the package symbol export to IDX does not contain the PKG_PIN_ONE property, the export utility uses a pre-defined selection method to determine the primary pin. The order of pin one selection is defined by the `pinOneCfg.txt` file located in the installation_directory.

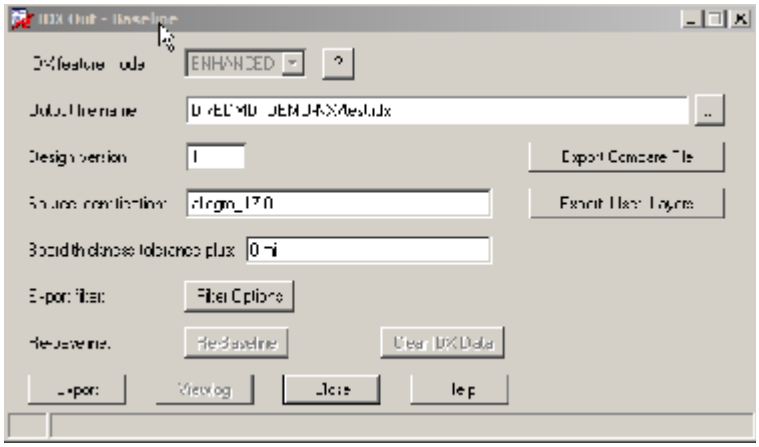
User Defined Layer and External Copper Layer Support

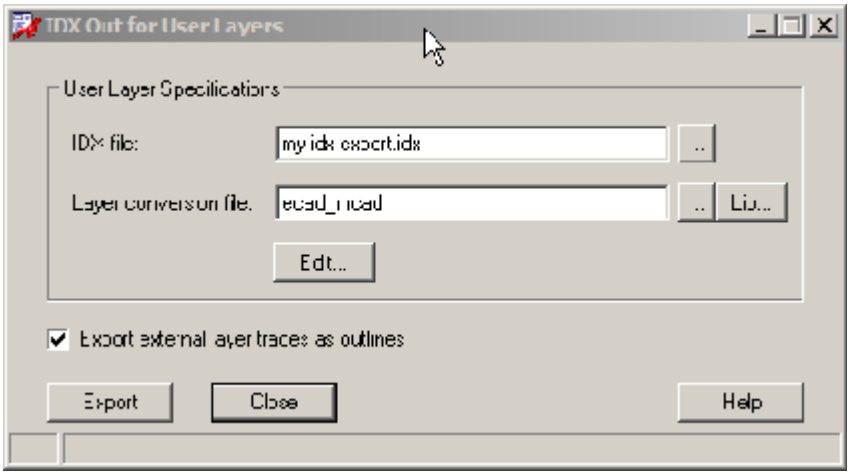
Enhanced feature support for IDX in the Allegro PCB Editor 17.2 release includes the ability to import and export user-defined layers and subclasses.

- User-Defined Layer Export

  Designs often require multiple layer export of different materials and structures which are not represented by conductor or dielectric features in the exported IDX data. Proper

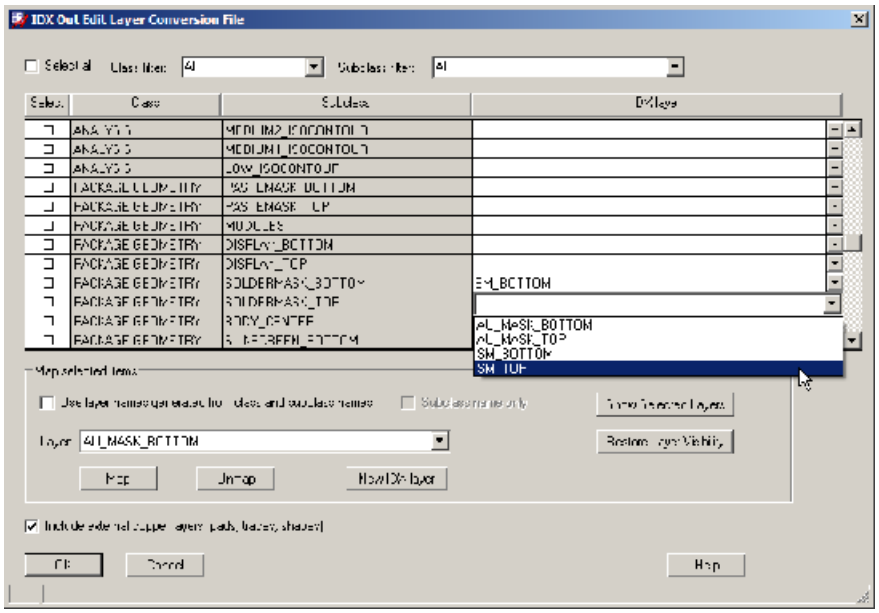
representation of this data requires a mapping feature to identify what Allegro Class/ Subclasses are associated with the MCAD tool set.





One of the most common requirements is the export of traces or etch data to be passed from the Allegro layout to the MCAD tool. Other feature layers, such as adhesive layers, plating layers, and so on are requested as well. The mapping feature available in the IDX Export tool allows you to define Class/Subclasses associated with the MCAD tools

layering requirements. Multiple Class/Subclass layers may be associated with the MCAD layer. The mapping feature is similar to the existing DXF mapping features.



Important

Recognizing that the exchange of etch exported to the IDX file will result in a very large IDX file, and the potential of managing an extreme number of etch objects being altered, the exchange of conductor/etch is driven by ECAD to MCAD, with no collaboration capability.

Also, only those IDX layers which are mapped to the CLASS/SUBCLASS layers are exported to a new baseline IDX file. Specific etch shapes initially created by the MCAD tool may be imported and collaborated upon only if initiated in this manner.

- User-Defined Layer Import

  Import of user-defined layers is facilitated through IDX data using the same mapping tool that is used while exporting. The MCAD layer name defined in the mapping file must match the MCAD layer name in the IDX file. The geometric data contained on that layer is then added to the CLASS/SUBCLASS identified in the mapping file. The layer is

mapped with the first mapped instance found in the `ecad_mcad.cnv` file. MCAD layer cannot be mapped to multiple CLASS/SUBCLASSES

Sample view of a Mapping file:

```
#CLASS!            SUBCLASS!                          IDX_LAYER!
#-------------------------------------------------------------------
BOARD GEOMETRY!
                   SOLDERMASK_BOTTOM!                 SM_BOTTOM!
                   SOLDERMASK_TOP!                    SM_TOP!
PACKAGE GEOMETRY!
                   SOLDERMASK_BOTTOM!                 SM_BOTTOM!
                   SOLDERMASK_TOP!                    SM_TOP!
PIN!
                   SOLDERMASK_BOTTOM!                 SM_BOTTOM!
                   SOLDERMASK_TOP!                    SM_TOP!
VIA CLASS!
                   SOLDERMASK_BOTTOM!                 SM_BOTTOM!
                   SOLDERMASK_TOP!                    SM_TOP!
ETCH!
                   TOP!                               ETCH_TOP!
                   BOTTOM!                            ETCH_BOTTOM!
PIN!
                   TOP!                               PAD_TOP!
                   BOTTOM!                            PAD_BOTTOM!
VIA CLASS!
                   TOP!                               PAD_TOP!
                   BOTTOM!                            PAD_BOTTOM!
#END
```

Hole/Slot Support

Padstacks defined with rounded or rectangle slotted holes are exported as slots in the enhanced capabilities of the IDX Export function.

IDX Compare Utility

The exchanging of ECAD/MCAD data during the design process often requires many files, and many different versions of files. There is a risk of missing the import/export of file data during the collaboration process. An incorrect file might be imported rendering the ECAD and MCAD design going out-of-sync. Based on the IDX collaboration process, the ECAD and MCAD current states can be compared to verify synchronization of the two databases. There are two options in this verification process depending upon the capabilities of the MCAD tools:

- Allegro IDX MCAD baseline import

- Allegro IDX Export for Compare
- Allegro IDX MCAD Compare (Allegro Compare)

  The current state of the MCAD tool is compared with the current state of the Allegro database. The comparison produces a log file and two incremental files if any differences exist. This process requires the MCAD tool to export a baseline file that maintains the current IDX identifiers. The incremental file created represents the differences between the two tool sets. When the differences are imported, you can run the Compare utility again for the final validation.

- Allegro IDX MCAD Compare (MCAD Compare)

  If the ECAD/MCAD databases are to be compared in the mechanical tool, a special baseline file can be created for the current state of the Allegro drawing. When a typical baseline file is created from the Allegro database, all records of past modifications, and special object labeling are reset to new values. Creation of standard baseline data for comparison leads to incorrect results. Allegro can export a baseline specifically for comparison without impacting any of the changed states or history on all previous collaboration since the last baseline. This exported file is targeted for use in comparisons only, and should not be used as a standard baseline.

OrCAD Layout Footprint Libraries Added to PCB Editor Libraries

In release 17.2, OrCAD Layout footprints have been translated and integrated with PCB Editor. These footprints are available in the `<installation_directory>/share/pcb/pcb_lib folder`.

The integrated footprints belong to different categories, some of which are listed:

- Block Connectors
- Ball Grid Arrays
- GLCC
- D-Connectors
- Dimm Edge Fingers
- Dimm Sockets
- DIN Connectors
- DIP 100 (Buttmount and Standard)

- D-Sub Connectors
- D-Sub High Density Connectors
- Edge Connector Sockets
- Future Bus Connectors
- PC/104
- PCI
- Ploar/Friction Connectors (.100 and .156)
- Pin Grid Arrays
- PLCC
- Gull-Wing Quads
- Gull-Wing Bumpered Quads
- Relays
- RF Connectors
- Sbus Connectors
- SIMM Edge Fingers (0.50 and .100)
- SIMM Sockets (0.50 and .100)
- SIP's
- SM Discrete Components
- SM SO Gull-Wing Families
- SM SO J-lead Family
- Telecomm Connectors
- TM Axial-Lead
- TM Capacitors
- TM Cylindricals
- TM Diodes
- TM Discs
- TM Radial-Leaded

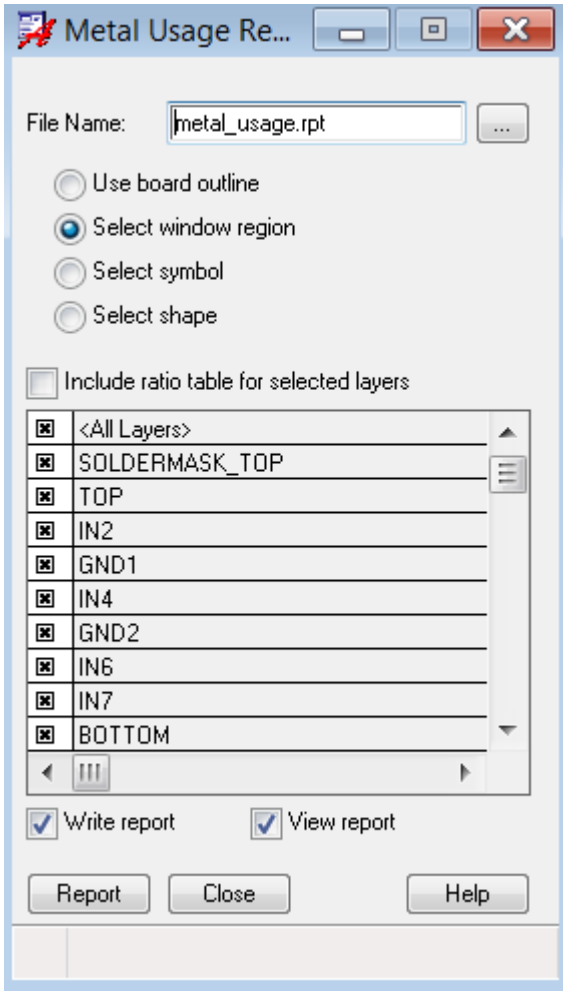
- TO's
- Variable Resistors
- Wall/Shroud Connectors .100
- XT
- ZIGZAG .100 Staggered Rows

Database and Misc Enhancements

- Metal Usage Report
- Refresh Symbol – Maintain Padstacks
- Performance Improvements
- New Variables
- New Properties
- Modified Properties
- Skill Enhancement
- Import Logic Enhancement
- Design Length Enhancement
- Material Name Length Enhancement

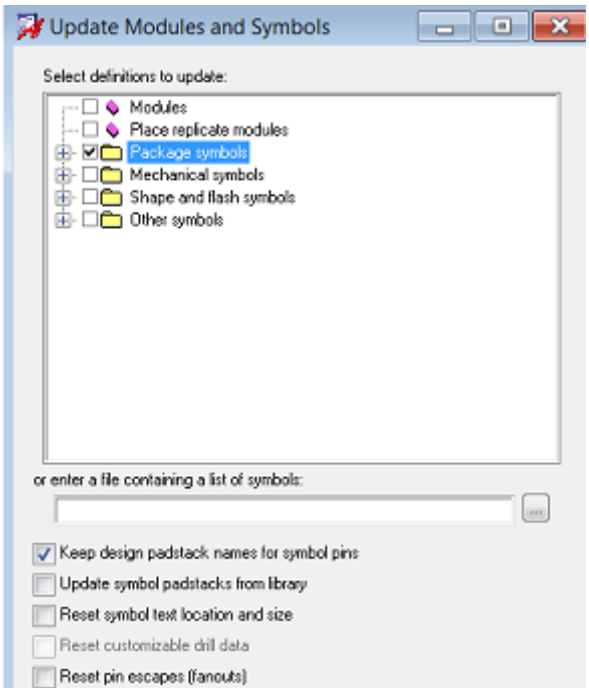
Metal Usage Report

The APD/SiP-based metal usage report is now available in PCB Editor in *Tools* menu.



Refresh Symbol – Maintain Padstacks

A new refresh symbol option, *Keep design padstack names for symbol pins,* is now available to maintain design padstacks. This behavior is also supported by using the `-k` option when running the command in batch.



Performance Improvements

- CPU-intensive applications see a performance gain between 10-20%.
- Import logic (`netrev`) for very large pin count devices (>2k pins) is much faster compare to previous releases.

New Variables

- *`idx_enhanced_features`* - Enables enhanced IDX features.

New Properties

- BOARD_THICKNESS_TOLERANCE_PLUS - Adjusts the overall board thickness in the IDX flow.

- IDX_OTHER_OUTLINE - Allows a bi-directional exchange of the shape if the user-defined shape is not originally defined in the MCAD tool.
- PACKAGE_OFFSET_TOP and the PACKAGE_OFFSET_BOTTOM - Uses a value that offsets the component height across the surface of the board to account for pastemask thickness.
- NO_PCB_BUNDLE - Set on a NetGroup/bus object, it prevents creating/updating bundles and visibility objects. The property is controlled by Constraint Manager – Properties – Ratsnest Bundle Property table, *Disable Automatic Ratsnest Bundle* column. *On* option selected for a group implies that the property is set.
- IGNORE_SHAPE_ISLAND - Applied to etch rectangles or shapes to suppress their reporting in the shape island report or the delete island command.
- BONDFINGER_DRC_DISABLED - Applied at design level in ICP designs (`.mcm` and `.sip`) to disable bondfinger DRC checks.
- DOGBONE_FANOUT - Set to an Allegro component and forces Specctra to apply dogbone fanout pattern to it. This property is usually applied to BGAs with irregular pin matrix.
- PKG_PIN1_ORIENTATION - Used in the IDX flow. This property can be assigned to a pin in the symbol editor. It defines pin 1 to the MCAD system. By default, Allegro PCB Editor uses the `pinOneCfg.txt` to identify pin 1 by its name.
- MARKING_USAGE - Applied to rectangle, filled rectangle, shape, figure, and line. This property is used in IPC2581 Export and indicates the marking usage for the package geometry.
- ASI_MODEL - Applied to component instance and definition, this property is used to pass model assignments to Cadence Sigrity applications through new integrated translator.
- DYN_FILL_XHATCH_CELLS - Controls how aggressive dynamic shapes fill partial crosshatch opens. Normally this is set via the global dynamic shape dialog or on the instance base shape dialog.
- DYN_FIXED_THERM_WIDTH_ARRAY - Allows by layer control of a pin or via's thermal line width. This property suppresses Min Line Width DRC errors for thermal clines in dynamic shapes.
- DYN_OVERSIZE_THERM_WIDTH_ARRAY - Allows by layer control of thermal width overrides. This property specifies the width of the connect lines added as thermal relief. The width of the reliefs should be less than or equal to the width of the hatch line to which they connect.

- DYN_FIXED_THERM_WIDTH_ARRAY - Allows by layer control of a pin or via's thermal line width. This property suppresses Min Line Width DRC errors for thermal clines in dynamic shapes.
- DYN_CLEARANCE_OVERSIZE_ARRAY - Allows by layer control of a pin or vias dynamic shape voiding. This property overrides the value in the *Oversize values* field in the Clearances tab in the Shapes Instance Parameters dialog, and increases the clearance around the specified element. The value is a positive design unit. Negative oversize is not supported.
- REVISION_ID - Set on the root design, symbol definition and padstack. This property is added for future work and currently is not in use.
- ADJACENT_LAYER_KEEPOUT_ABOVE - Applies to pins and vias this property works in conjunction with the adjacent keepout pad type built into padstacks. The property controls the number of layers above the start of a pin or via that a route keepout should be generated.
- ADJACENT_LAYER_KEEPOUT_BELOW - Applies to pins and vias this property works in conjunction with the adjacent keepout pad type built into padstacks. The property controls the number of layers below the end of a pin or via that a route keepout should be generated.
- PINS_ALLOWED - Applies to shapes or filled rectangles that are route keepouts this property permits pins within the keepout.
- NODRC_SYM_SHAPE_SOLDERMASK - Applies to root design, symbol instance and symbol definition. When present, inhibits mask to shape DRC against any shape within a symbol. Suggested model is to assign it in the symbol editor to its design root, so that it inhibits these DRCs when the symbol is placed in a design.
- PIN_GLOBAL_FIDUCIAL - Applies to pin that uses a fiducial padstack. This property indicates that a pin is a global fiducial and is used in IPC25281 output to meet the standard.
- IDX_FEATURE_MODE - Applies to a root design, this property specifies the mode of the IDX export as STANDARD or ENHANCED.

Modified Properties

- DYN_OVERSIZE_THERM_WIDTH - Cannot be applied to pins or vias now. DYN_OVERSIZE_THERM_WIDTH_ARRAY replaces this property for pins and vias.
- DYN_FIXED_THERM_WIDTH - Cannot be applied to pins or vias. DYN_FIXED_THERM_WIDTH_ARRAY replaces this property for pins and vias.

- DYN_THERMAL_CON_TYPE - Can now be applied by layer or layer type.
- DYN_THERMAL_BEST_FIT - Can now be applied by layer or layer type.
- DYN_MIN_THERMAL_CONNS - Can now be applied by layer or layer type.
- DYN_MAX_THERMAL_CONNS - Now applies to subclass design unit array.
- LIBRARY_PATH - Supports padstacks in addition to symbols. If it is not set, either the padstack was created in pre-17.2 Allegro PCB Editor or was created within the design (`brd, mcm, sip` or `dra`).
- NODRC_SYM_PIN_SOLDERMASK - Can now be applied to symbols to suppress soldermask DRCs. The use model is to build it into the footprint - apply at design level in symbol editor.
- NODRC_SYM_PIN_PASTEMASK - Can now be applied to symbols to suppress pastemask DRCs. The use model is to build it into the footprint - apply at design level in symbol editor.
- DYN_CLEARANCE_TYPE - Can now be applied by layer or layer type.
- DYN_CLEARANCE_OVERSIZE - Not supported on pins or vias. DYN_CLEARANCE_OVERSIZE_ARRAY replaces this property.
- VERSION_ID - Can now be applied to padstacks.
- DYN_FIXED_THERM_WIDTH - Not supported on pins or vias. DYN_FIXED_THERM_WIDTH_ARRAY replaces this property.
- VOID_SAME_NET - Can now be supported on etch shapes and etch filled rectangles.
- IC_DESIGN_NET_NAME - Can now support rectangle, fill rectangle, and shape.
- IDX_EXCLUDE - Can now support Generic groups.
- PKGDEF_ALT_STEP_FILE - Can now be applied to component definition and symbol instance defines the mapped STEP model for the package
- PKGDEF_ALT_STEP_TRANSFORMATION - Can now be applied to component definition and symbol instance defines 3D transformation between the mapped STEP model and the package.

Skill Enhancement

New Skill APIs are available, documentation has also been updated to reflect APIs added during the 16.6 QIRs.

Import Logic Enhancement

Xnets now getting dynamically updated when Signal Model changes, that is import logic. As a result makes Xnets outdated.

Design Length Enhancement

The default internal name length for new designs has increased to 255. It was 32 prior 17.x.

Material Name Length Enhancement

Material names length has increased from 19 to 250 characters.

Productivity Enhancements

The following list of features have been moved from the High-speed and Miniaturization product options to the Allegro PCB Editor base product.

- Backdrilling
- Differential Pair Dynamic Phase Control
- Highlight Segments Over Voids
- Spread Lines between Voids
- Via-Via Line Fattening
- Contour Routing

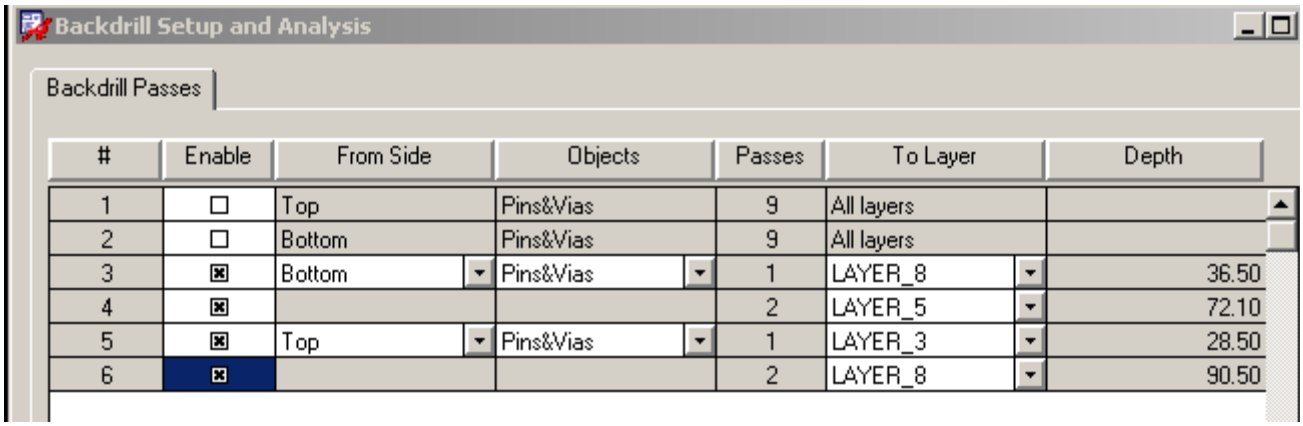
Backdrilling

Today's high-speed serial I/O technology presents new challenges for hardware engineers. Passing high frequency signals over a backplane requires minimizing the effect of plated through hole (PTH) stubs. This can be done by using the full length of the barrel for signal layer transitions, thus keeping stubs to a minimum, the use of buried or blind vias, or through a Board Fabrication process called Backdrilling.

Backdrilling in the Allegro PCB Editor is a flow application. Nets targeted for potential backdrilling require the property `backdrill_max_pth_stub`. The value of this property, which can be applied at the schematic level or inside the PCB Editor, is the maximum allowable vertical stub in units of length.

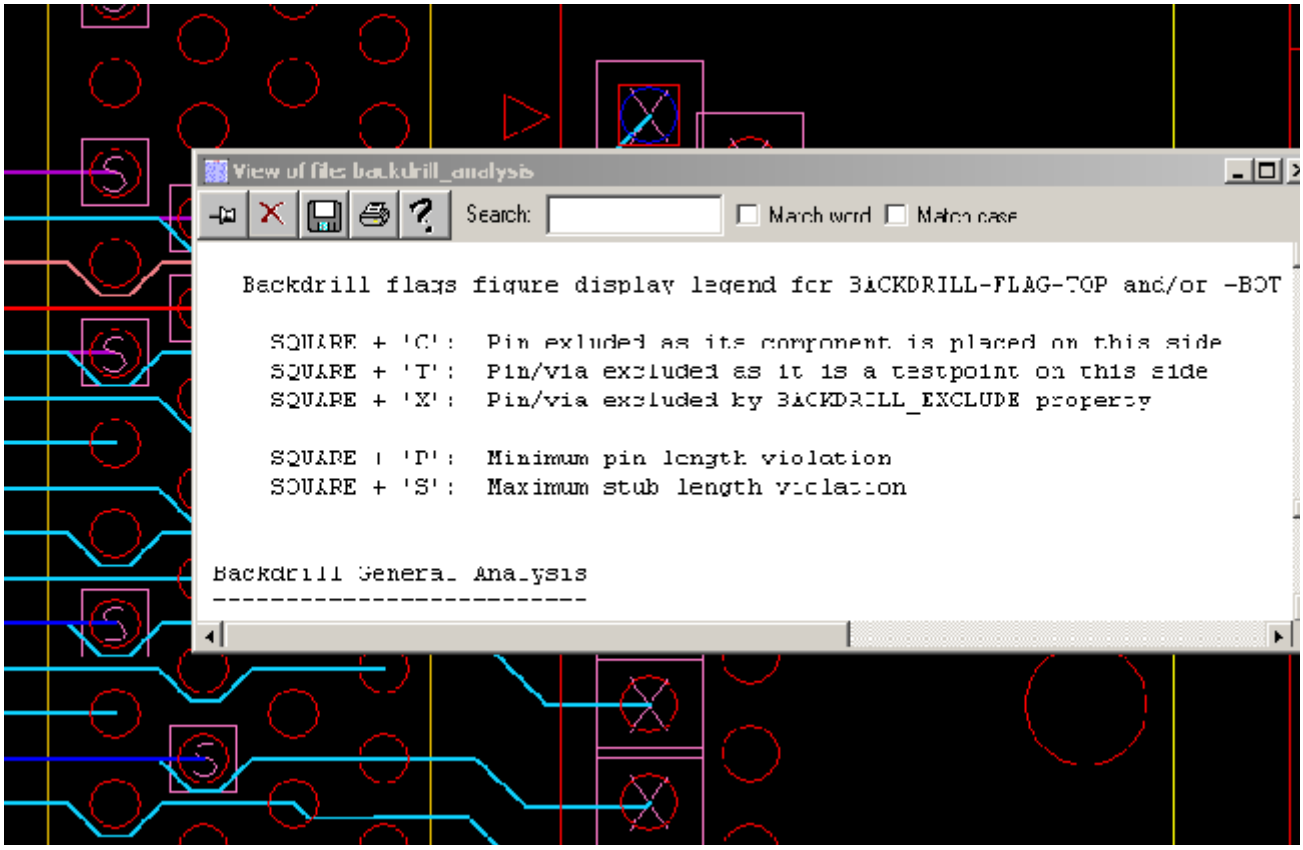
A setup and analysis GUI provides the controls for pass setup and analysis results. Pass setup can be system or user-defined and includes:

- Side of PCB (top, bottom, both)
- Object type (pin, vias, both)
- User Defined Layer Configurations
- System calculated Drill Depth



Graphic feedback in the form of code flags assist in the identification of violations, such as testpoint conflicts or remaining stub violations. A detailed log file provides general analysis information about pass setup, drilling, and remaining violations. Manufacturing output is

enabled by a new option in both the NC Drill and Legend Parameter Forms. Each backdrill pass is represented by a unique drill legend and nc drill file.

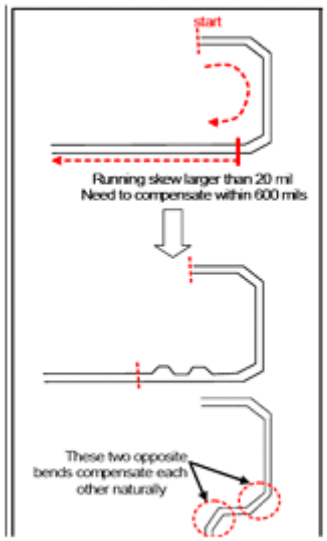


Note: For more information on backdrilling, refer to the Best Practices paper available on the Cadence Online Support website.

Differential Pair Dynamic Phase Control

Differential Pair technology has evolved where more stringent checking is required in the area of phase control. This is evident on higher data rates associated with parallel buses, such as QPI, SMI, PCI Gen 2, DDR, QDR, and Infiniband. The differential pair technology sends opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential in assuring that they function as intended. As the current Static Phase is limited to a one-time check across the entire Driver-Receiver path, a new Dynamic Phase check is introduced that performs phase checks at bend point intervals across the differential pair. The check is designed to meet the guidelines suggesting the path lengths of the true and complement signals within the differential pair must differ by no more than `x mils` along the entire path of the net. If at any point on the net, the skew between true and complement

exceeds `x mils`, this mismatch needs to be compensated within `y mils`. Representative values for `x` and `y` might be `x = 20` and `y = 600`.



Setting the Dynamic Phase DRC

The constraint set associated with differential pairs supports both static and dynamic phases. The margins of each constraint can be set independently using length or time. The Max Length (running skew) constraint is limited to length only.

Uncoupled Length		Static Phase	Dynamic Phase		Min Line Spacing		
Gather Control	Max	Tolerance	Max Length	Tolerance		Primary Gap	Primary Width
	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*
					0.00	0.00	5.00
Include	300.00	5 mil	600.00	20 mil	5.90	6.00	6.00

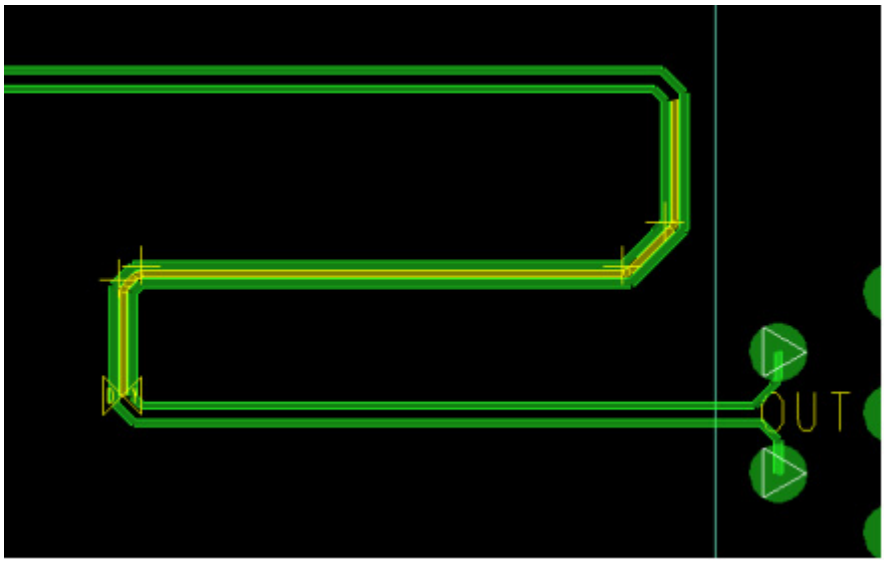
Terminology

- *Static Phase Tolerance*: A one-time check from Driver to Receiver comparing lengths or delay of each member. If a Driver cannot be determined, the check is performed across the longest path of the pair.
- *Dynamic Phase Tolerance:* Etch length of each member is compared at each bend point interval across the Driver-Receiver path of the differential pair. Etch length is always measured back to the Driver pins.

- *Dynamic Phase Max Length:* Also called running skew. When specified, the differential pair is permitted to exceed the phase tolerance constraint for a contiguous etch length of less than or equal to the value of Max Dynamic Phase Violation Length.

Dynamic Phase DRC Graphics

Similar to how uncoupling is reported, a pseudo segment highlights the path of the differential pair that is out of phase. The highlighted segment is placed between the members. A DRC marker (D-Y) is located at the point where the differential pair first goes out of phase with respect to Driver pin location. In other words, the marker is closer in proximity to the Driver, not the Receiver pins. Only 1 DRC marker is located on the differential pair, even if there are multiple instances of phase violations. Cross hair figures are placed at bend intervals and are located on the longer of the 2 members. Hover over the cross hair to get phase mismatch feedback in the form of a datatip.



Driver Pin Display

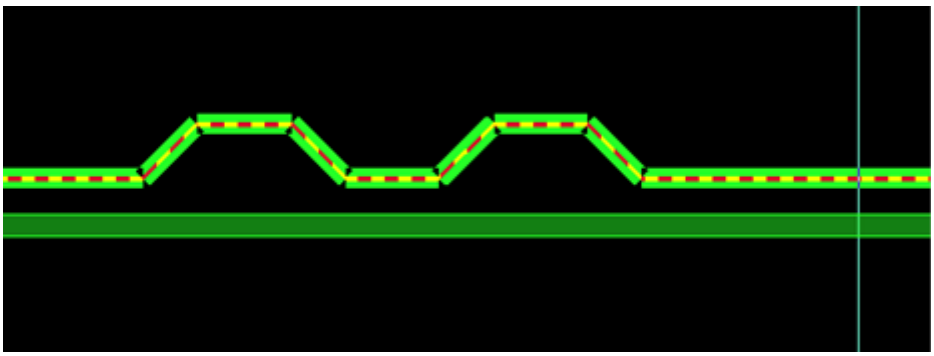
Differential Pair Driver pins can be identified by enabling the setting *Diffpair Driver Pins*. This setting is located in the *Setup – Design Parameters – Display* section. A pin must have its pin use code set to OUT for a Driver symbol to appear.

Note: A pin use code of OUT is not necessary for the Phase DRC to work. The DRC code randomly determines a driver source in an ambiguous situation.

Adding Phase Compensation

One of the methods used to address the phase mismatch involves adding small bumps to the shorter member. This can be accomplished using the *Delay Tune* command. When the command is invoked, adjust the tuning options to the preferred style; select the differential pair route and then right-click to choose *Single Trace* mode to tune the shorter member.

Another method to address phase mismatch involves creating opposite bends as part of the route path. This method keeps the pair coupled in a more natural manner and keeps uncoupling to a minimum.



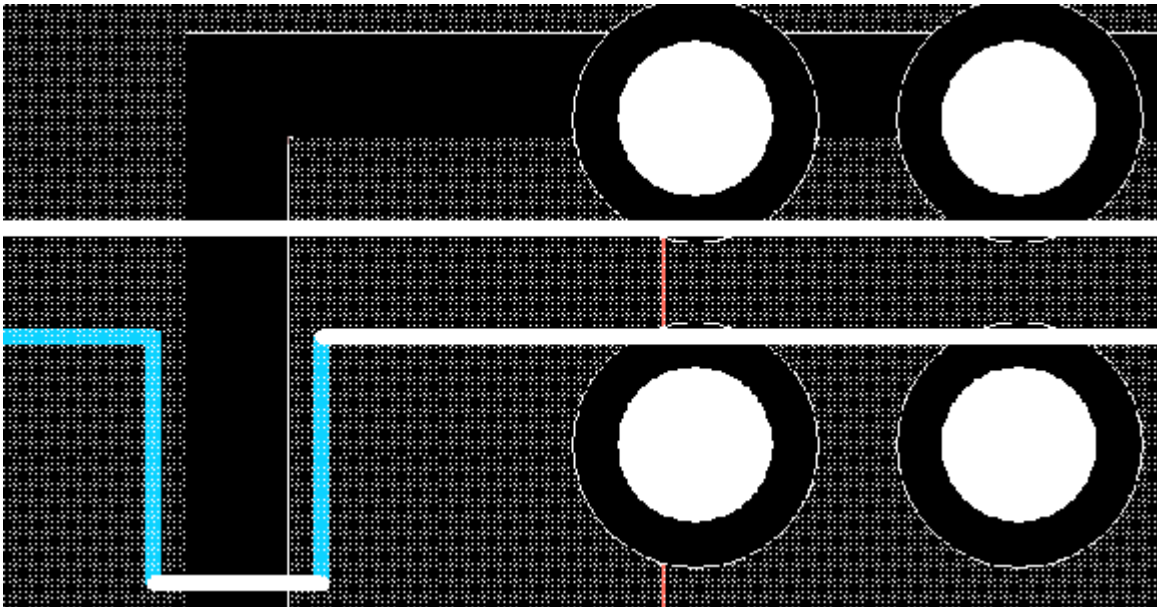
Highlight Segments Over Voids

To ensure a continuous loop of return path current, signal traces must reside over an uninterrupted copper plane. Even traces overlapping pin voids can cause disruption of current. Violations are traditionally detected by visually scanning the design, layer by layer, as a post-route process.

The *Segments Over Voids* command detects cline segments crossing adjacent plane layer voids. These voids can be antipads, split plane gaps, or manually created voids. All segments in violation become permanently highlighted along with the respective void based objects. A descriptive report sorts each violation by layer and differentiates segments crossing voids from ones with partial plane coverage.

A user preference variable, `sov_spacing`, provides global behavior for the spacing criteria used. A negative value allows segments to overlap voids by that distance. This may be necessary to suppress violations in sub 1MM pitch BGAs. A positive value is the minimum allowable spacing to edge of the void. The command is located in the *Display* menu and operates on all layers and logical nets by default; DC nets are not processed. To operate only on the active layer, set the variable `sov_active_only`. To operate only on selective nets,

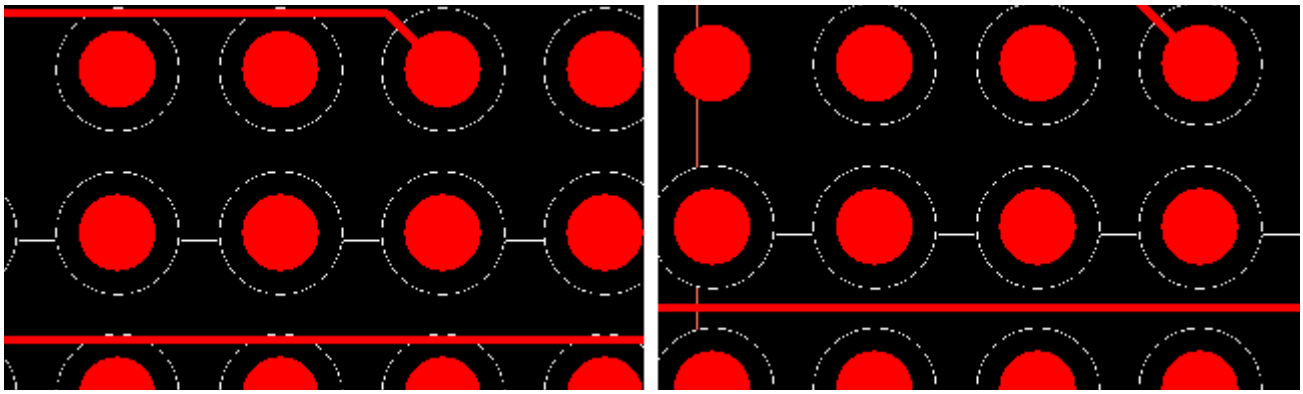
apply the property *sov_check* to the respective nets. The user preference controls are located in the SOV category of the User Preference form.



Spread Lines between Voids

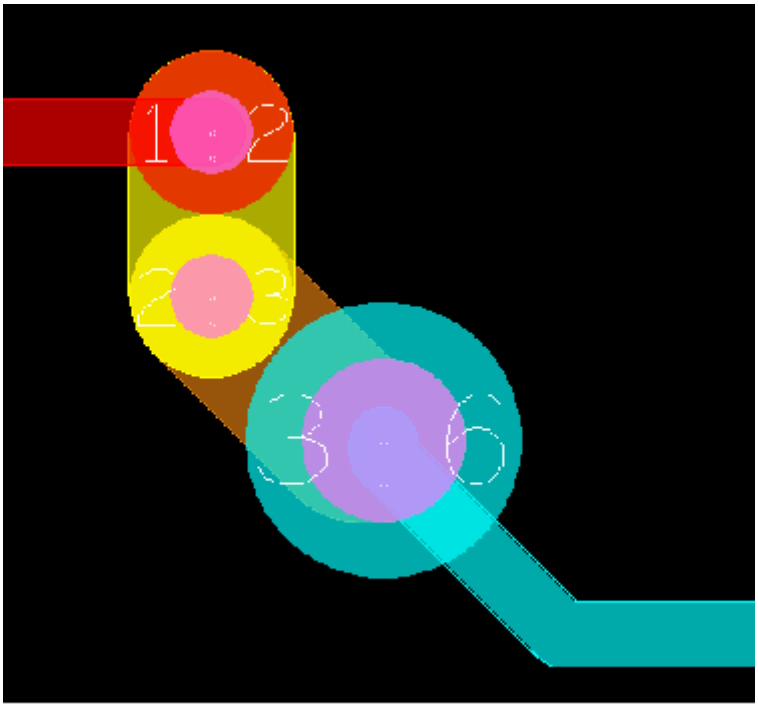
The *Spread Between Voids* command provides a semi-automatic solution to spread channel based clines with respect to adjacent plane layer voids. Used in combination with the new *Segments Over Voids* command, *Spread Between Voids* requires the selection of two pin or via objects that comprise a channel. If the channel consists of a single cline, the cline is centered between the pin/via based objects. If two or more clines make up a channel, the clines is spread evenly away from the adjacent layer plane voids.

The *Spread Between Voids* command is located in the *Route – Resize/Respace* menu. The application works on the active layer and comes with a parameter option, void clearance.



Via-Via Line Fattening

A post route task associated with HDI Design involves increasing the line width between two tangent vias. This is done to remove the acute angle formation at the junction. A batch utility *Via-Via Line Fattening* located in the *Route – Resize/Resize* menu is available to increase line width between vias based on a user-defined edge to edge clearance. The algorithm determines the line width based on the smaller of the two vias. Options are available to waive impedance or the resultant max line width DRCs. It is advised to run this utility near the end of the design process as it is not possible to perform a reset of line width.

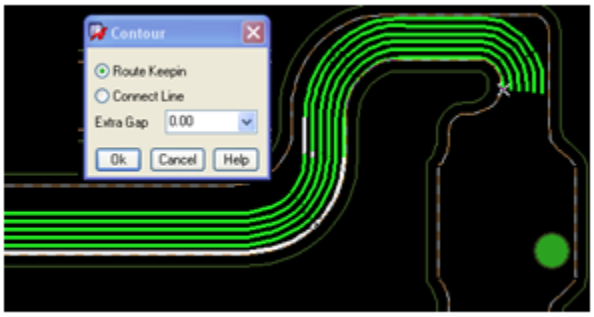


Line Fattening between Tangent Vias

Contour Routing

Routing a bus across the Flex section of a Rigid-Flex design in most cases involves the use of curved corners. Aligning the angle of the route to the corner radius is not always intuitive, especially on non-90 degree bends. Ideally one would like to simply guide the route following the contour of the outline or an existing Connect Line. Available in both single and multi-routing modes, contour hugging locks the current route to either the route keepin or an adjacent cline. When in the *Add Connect* command, use the context-sensitive menu to access the Contour options. An optional *Extra Gap* field is provided to increase the clearance to either contour element. Close the form and select the highlighted element, and

then guide your cursor along the contour element path. Click to release the contour hug and resume normal routing.



RF PCB Enhancements

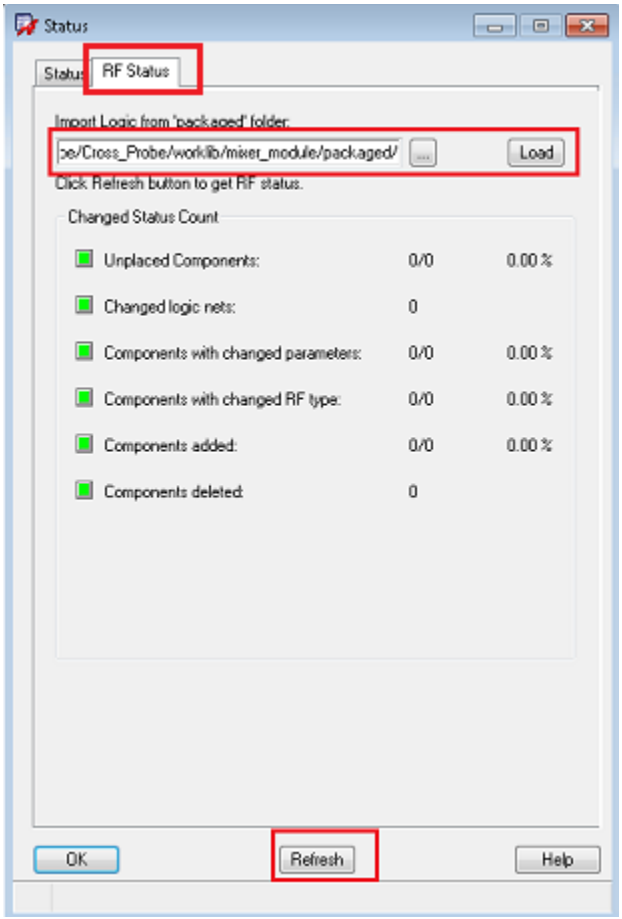
In 17.2-2016 release, several enhancements have been made in RF PCB to increase productivity in the following areas:

- RF Status Display Enhancements
- Clearance Initialization Enhancements
- Cross-probing between Schematic and Layout Enhancements

RF Status Display Enhancements

To view any change in RF components between schematic and layout, the `status` command has been enhanced to display RF Status in the *Status* dialog also.

A new tab *RF Status* has been added to the *Status* dialog, which is visible only if the *RF/Analog* option is enabled.

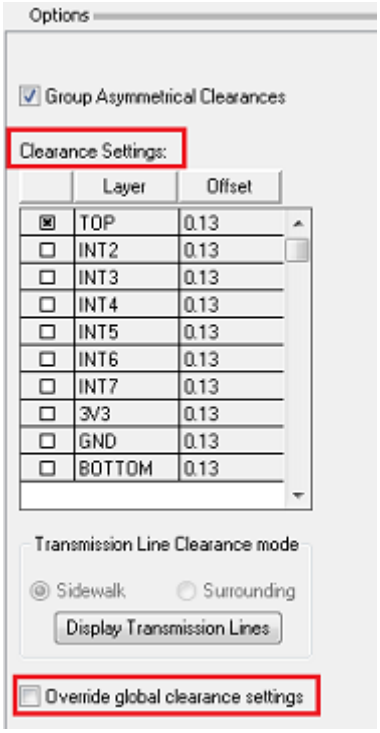


Using this new options, you can compare the schematic and physical design data and view the changes. A detailed report is displayed for every change if you click the color box.

For more information, see *Displaying RF Status* in *Allegro User Guide: Working with RF PCB*.

Clearance Initialization Enhancements

In 17.2, the clearance initialization setup has been integrated with the initialization command. A new option is also provided with the `rf_ac_init` command to enable the editing of global clearance settings.

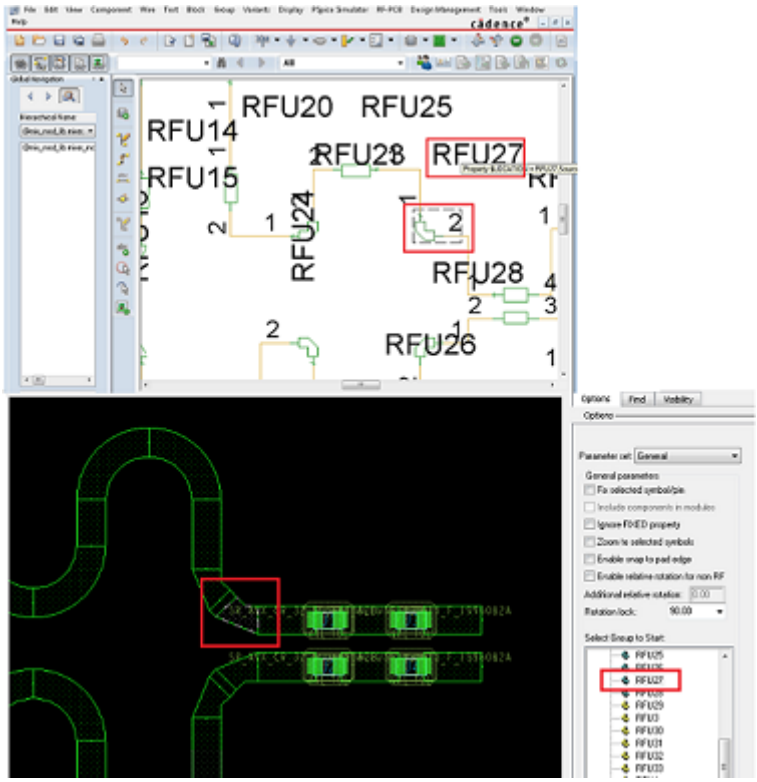


For more information, see *Allegro User Guide: Working with RF PCB*.

Cross-probing between Schematic and Layout Enhancements

The `rf_autoplace` and `rf_change` commands now support cross-probing between the schematic and the layout in the component selection stage.

On selecting a component or pin by clicking at the schematic canvas, the corresponding symbol is also selected in the layout editor and in the *Options* tab.



For more information, see *Allegro User Guide: Working with RF PCB*.

Cadence SiP Layout and Allegro Package Designer (APD)

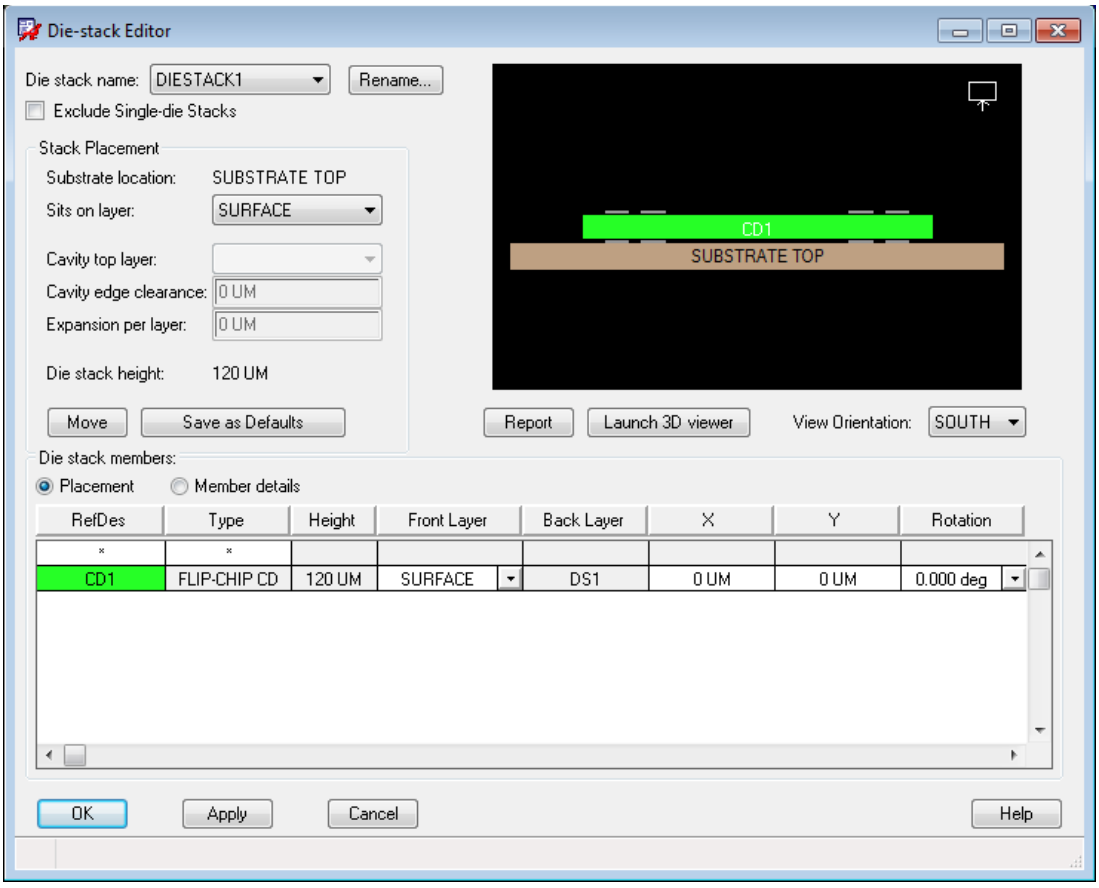
This section describes the new features and enhancements in Cadence® SiP Layout and Allegro® Package Designer (APD) in Release 17.2-2016.

Support for Two-sided Components

In 17.2-2016, you can now easily add die components with pads on multiple layers. The entire flow, starting from the creation of two-sided die components to editing and routing these components, has been updated for a seamless experience.

The following sections explains the major changes that have been made to enable two-sided die component support in the packaging flow.

Die-stack Editor Changes



The Die-stack Editor now displays all die stack members in one dialog window.

Select Placement or Material details to view different types of information about the listed component. For example, selecting placement displays information about height, front and back layers, X and Y coordinates, and rotation. Selecting Material details displays information about conductor and dielectric materials and their thickness.

You can move, delete, or swap components by right-clicking on the *RefDes* column of a component. The pop-up menu items depend upon the component type selected. For example, selecting a spacer allows you to resize the component.

Show Element Changes

Enhancements have been made to the show element feature to support two-sided die components. Now, the Show Element form shows the following information:

- Pad attachment type for all die pins
- *Pad side* field showing *BACK* for back-side pins.
- Back pin layer

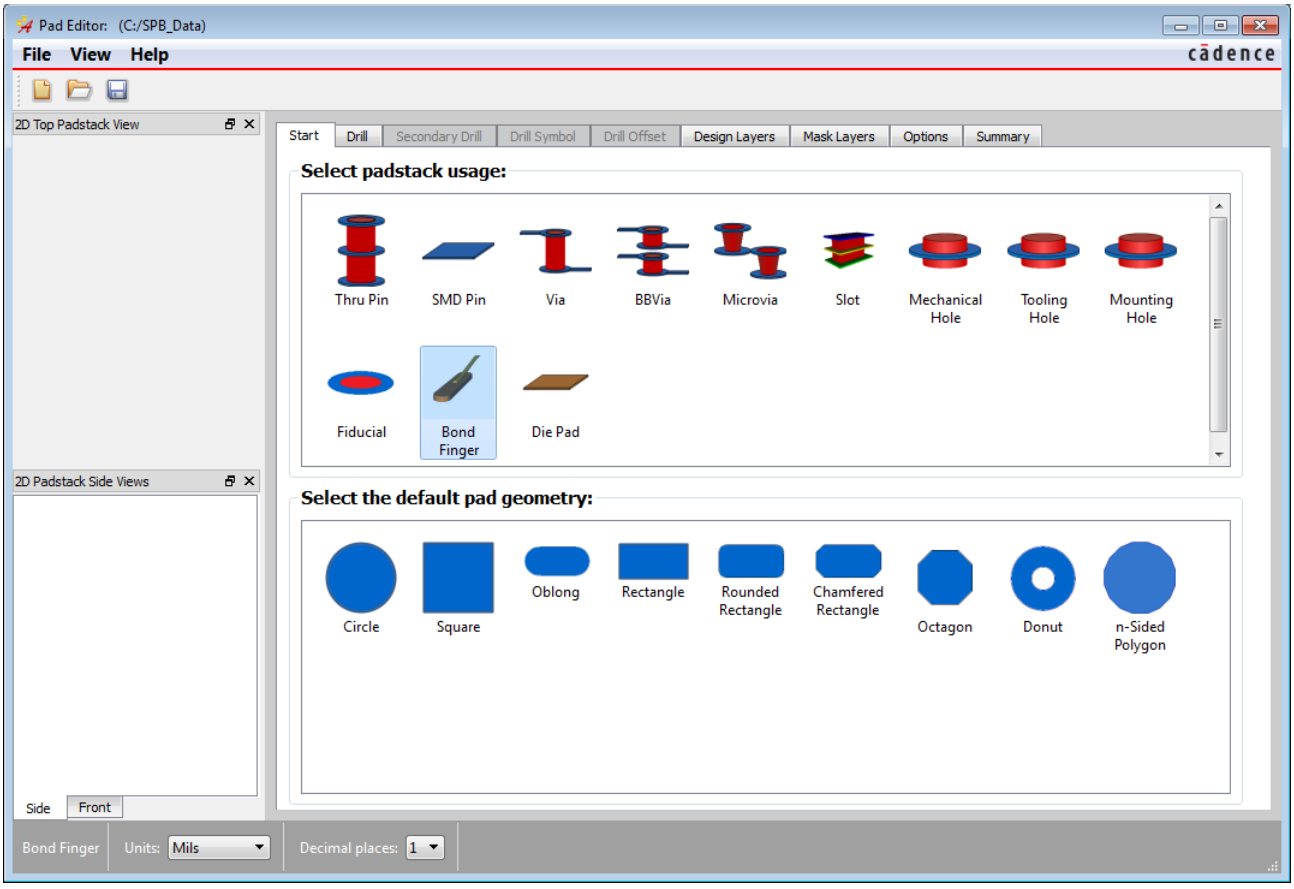
Symbol Edit Application Mode

The Add Pins and Change Characteristics commands have been changed to support two-sided die components. The following two new fields have been added to the Options window pane:

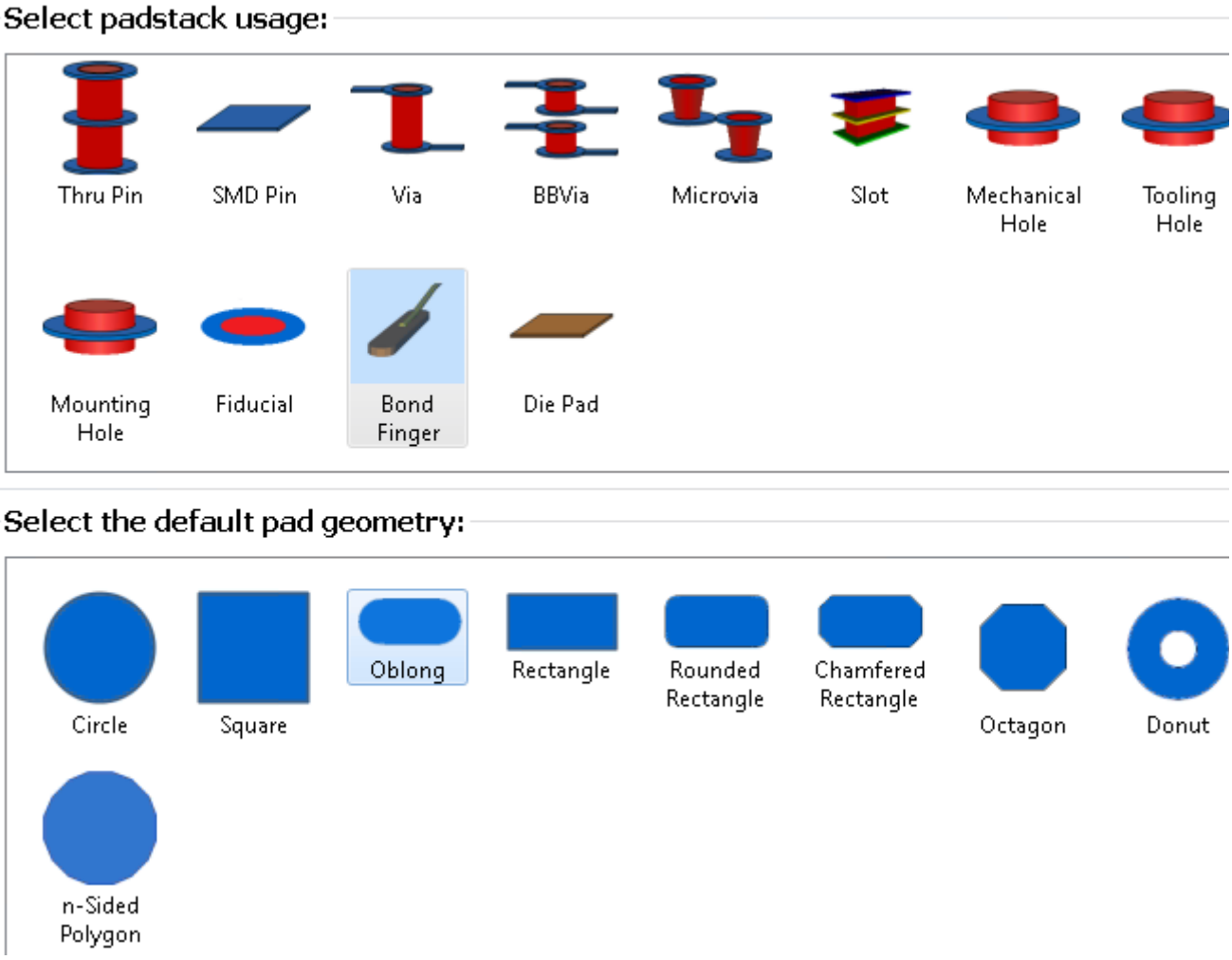
- Pad Type: Shows the pad type for the selected component. By default, pad type is bump for flip-chip and BGA, wire bond for die, and connect for all other components.
- Layer: Lets you change the layer for single layer components to create two-sided components.

Padstack Enhancements

You can use the enhanced flow-driven interface in 17.2-2016 to create and edit padstacks.



First, select one of the multiple padstack types and the default pad geometry in the Start tab.

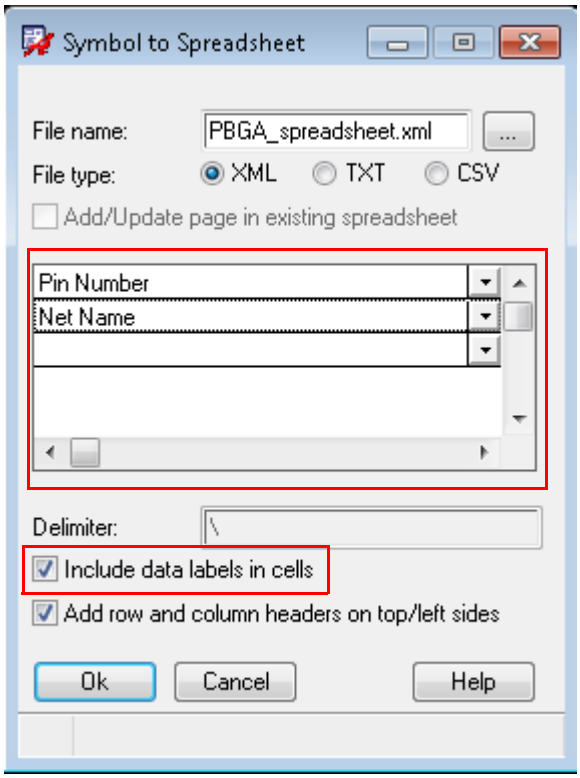


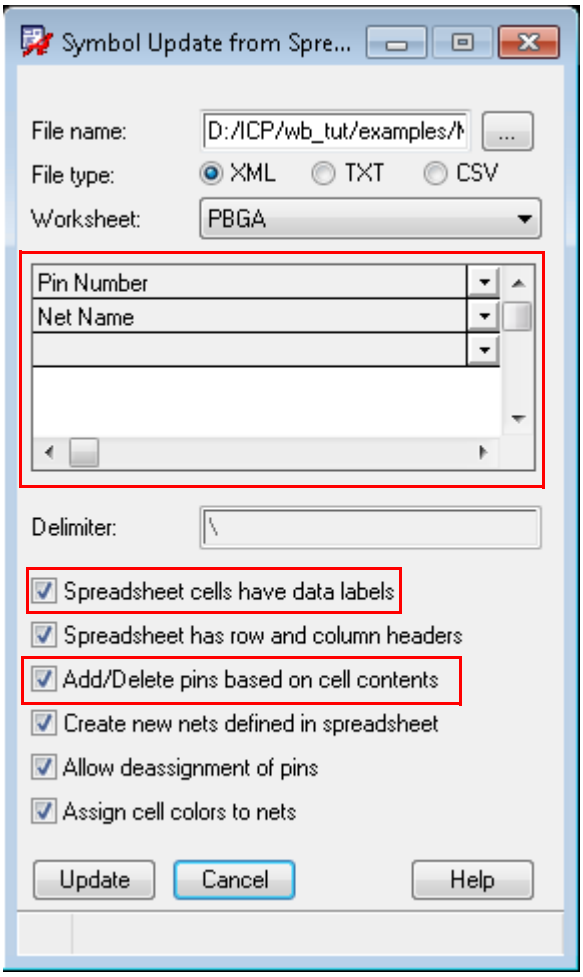
You can then define other relevant specifications, such as:

- Drill parameters in the Drill, Secondary Drill, Drill Symbol, and Drill Offset tabs.
- Pad geometry, shape and flash symbols, width, height, and offsets in the Design Layers tab.
- Up to 32 user-defined mask layers using the new Add Layer window.

Note: For detailed information on the padstack enhancements and changes, see *Allegro PCB Editor: What's New in Release 17.2-2016*.

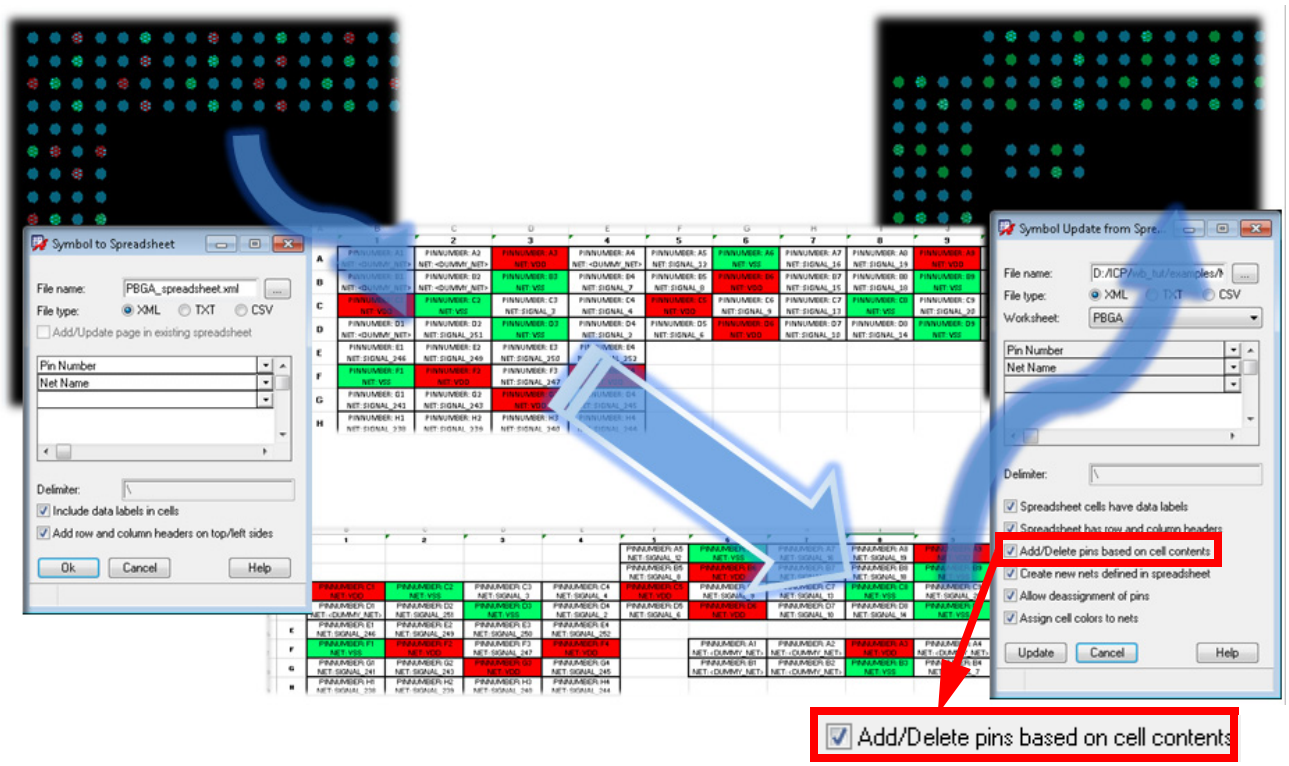
Enhancements in Symbol Spreadsheet





The *Symbol Spreadsheet* (*File – Export* and *File – Import*) feature allows export and import of symbols using spreadsheets. In 17.2-2016, this feature has been enhanced to allow you to add any number of entries using the new grids while exporting a symbol to spreadsheet. While importing a symbol spreadsheet, you can include keywords to automatically configure the resulting file.

Now, importing can add and delete pins from the symbol.



Pins are added to a cell which should be empty, but contains default values based on other pins of the symbol. The cell content is updated with values from the imported spreadsheet. Pins are deleted if a cell is empty but the pin matrix of the symbol contains a pin in that position.

In line with the new two-sided die component support in 17.2-2016, the exported spreadsheet has an additional worksheet for two-sided die components. This worksheet contains information about the back pins.

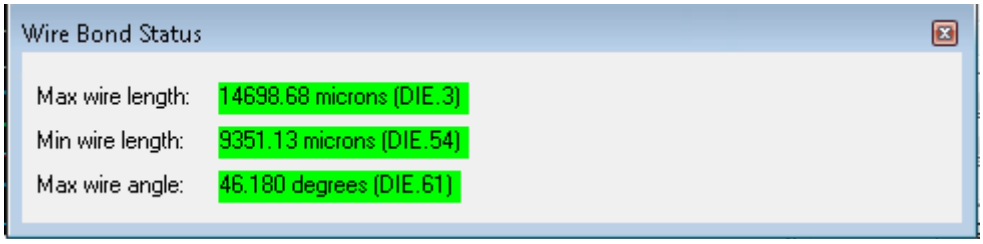
3D Viewer DRC Report Lists Net Names with Conflict

In the 3D Viewer DRC report, the net names for the objects in conflict are now listed. For example, if there is a short between wire bonds, 3D Viewer DRC report lists the issue with the location as well as the conflicting nets–enabling easy debugging by identifying the shorted nets.

DRC Errors

#	X	Y	Z	VALUE	CONSTRAINT	RULE	INPUT 1 NET NAME	INPUT 2 NET NAME
#1	3787.302	2649.850	900.546	0.000	0.001	#1	U32P_6	U31N_6
#2	3787.302	2649.850	900.546	0.000	0.001	#2	U32P_6	U31N_6

Configuring Wire Bond Heads-Up Display

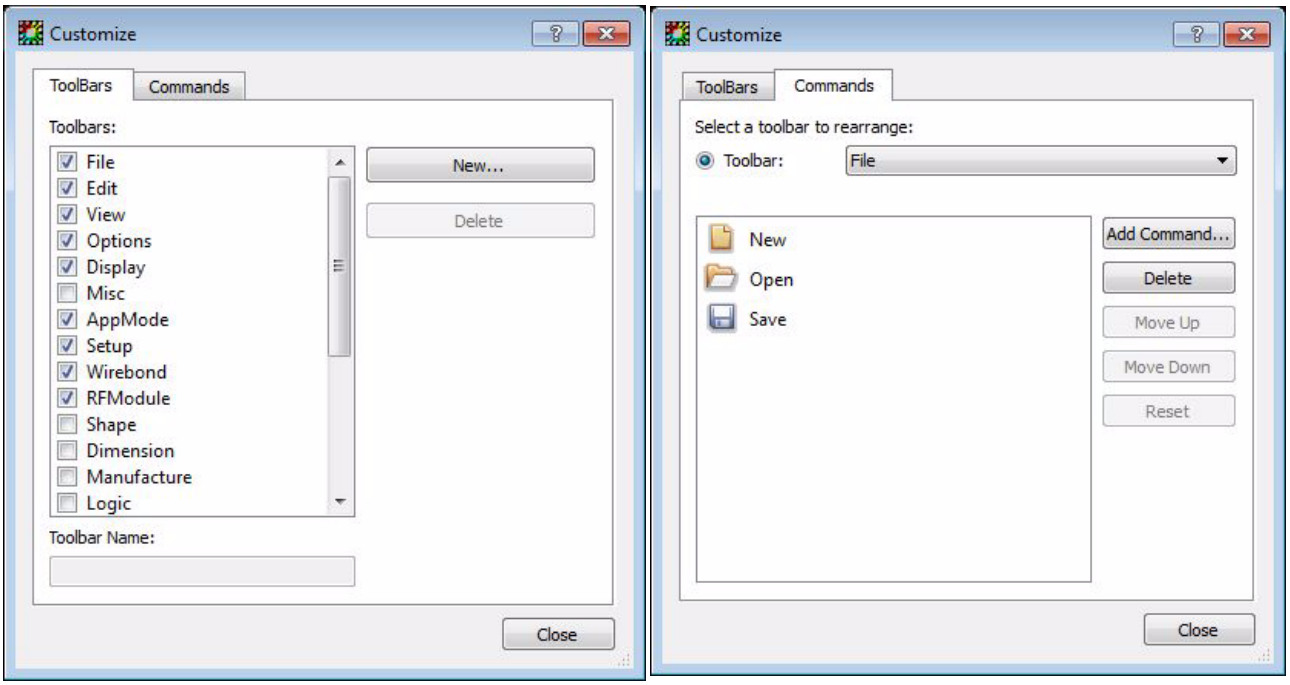


When you push, shove, or move wire bonds, the Wire Bond heads-up display shows *Max wire length*, *Min wire length*, and *Max wire angle*. In 17.2-2016, the three lines will be displayed by default, but you can change the displayed information by setting *wirebond_hud_line_1*, *wirebond_hud_line_1*, and *wirebond_hud_line_1* under *Ic_packaging – Wirebond* in User Preferences Editor.

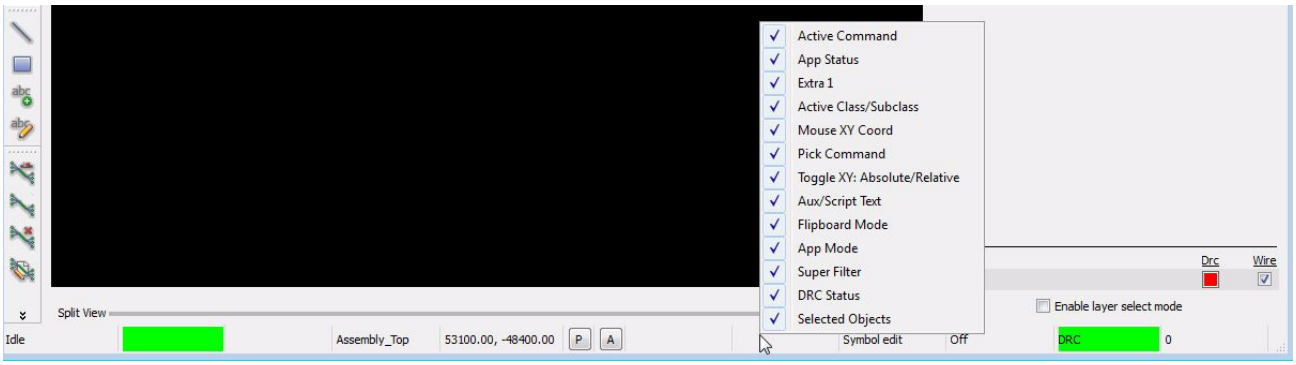
Canvas Enhancements

The canvas enhancements makes it easier to customize and personalize the workspace to achieve higher productivity.

- Customize toolbars with commands and icons of your choice. Choose *View – Customize Toolbar* to open the Customize dialog box.



- Show or hide panes of the status bar. Right-click the status bar and specify the panes you want to hide or show.

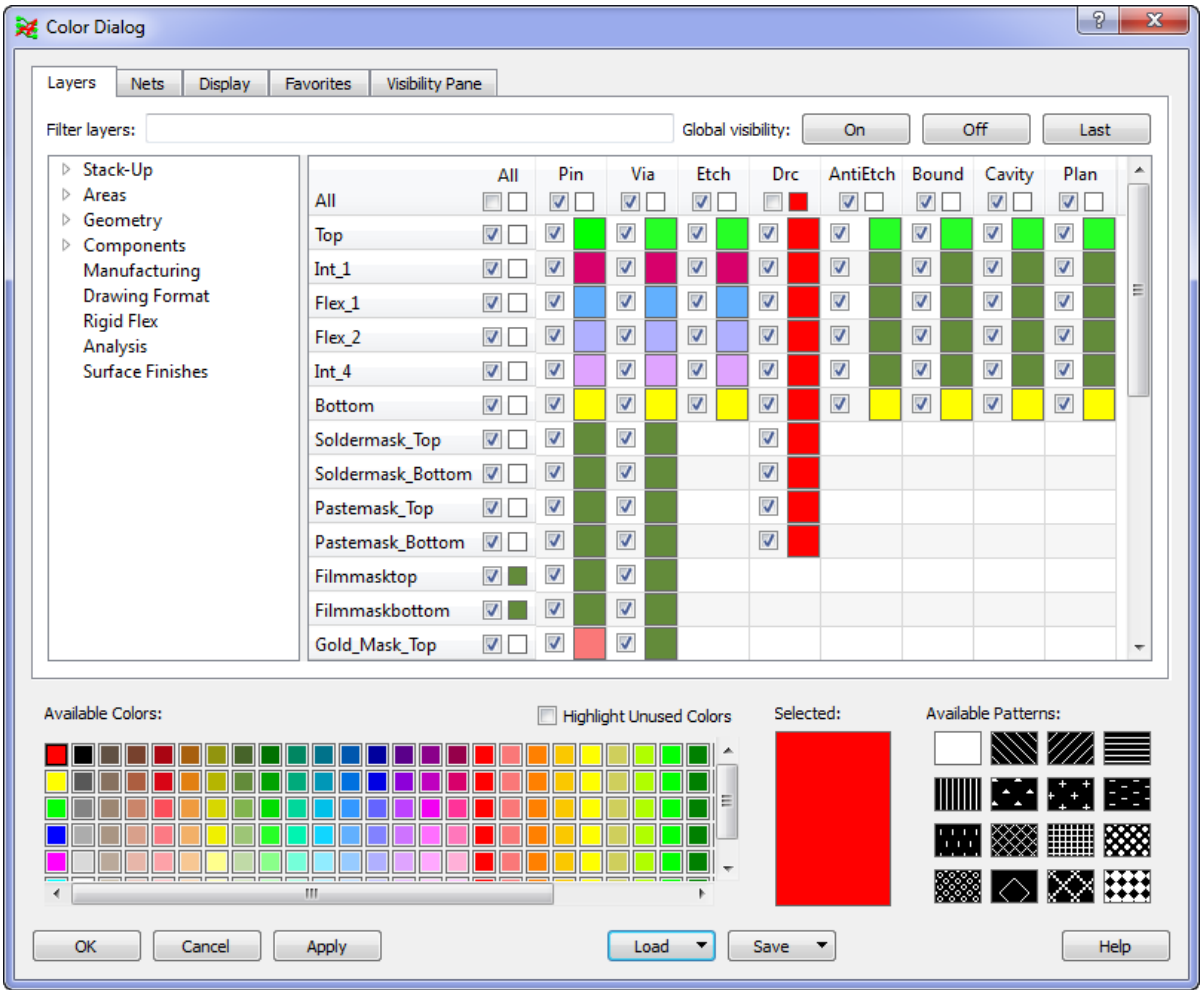


- Move around the information panes and stack them. The information panes are Find, Options, Visibility, Command, and View window panes. Move the panes by clicking along the pane name and then dragging them to a new location in the workspace.

Note: For more information on the canvas enhancements, see the *About the User Interface* section of the *Getting Started with Physical Design* User Guide.

Color and Visibility Enhancements

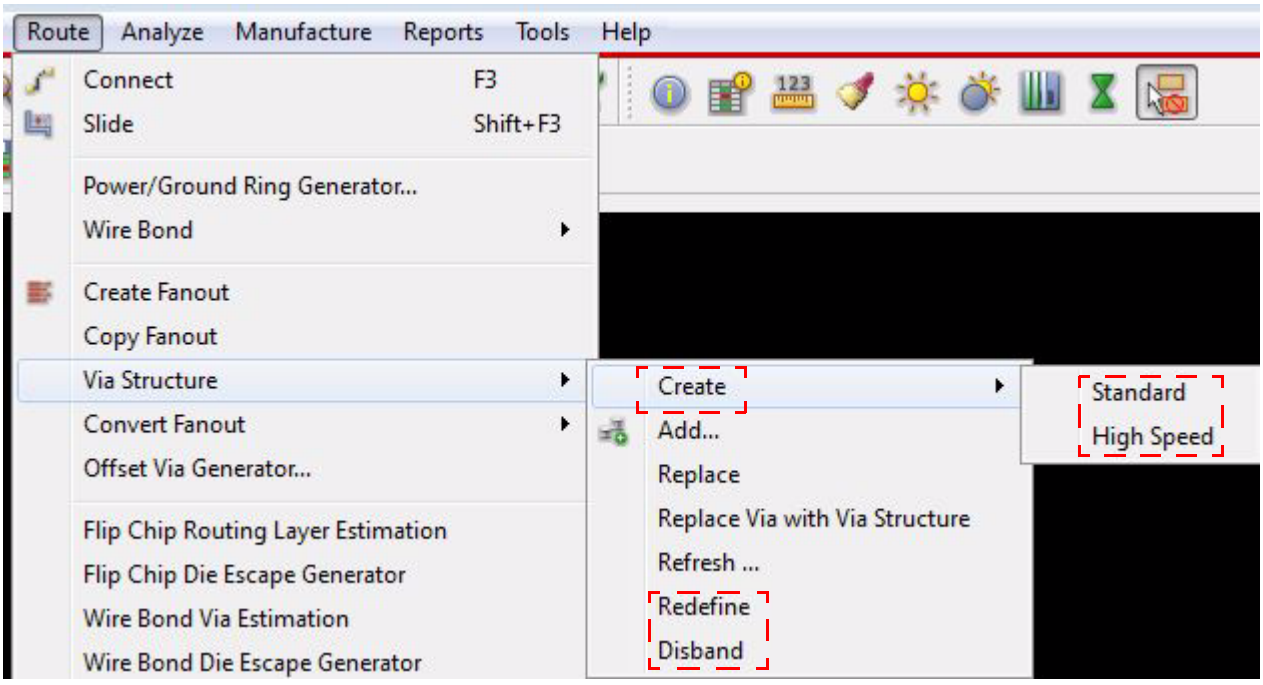
The Color Dialog now uses a tabular approach and categorizes the major features into tabs named Layers, Nets, Display, Favorites, and Visibility Pane.



Note: For more information on the color and visibility enhancements, see the Allegro PCB Editor section.

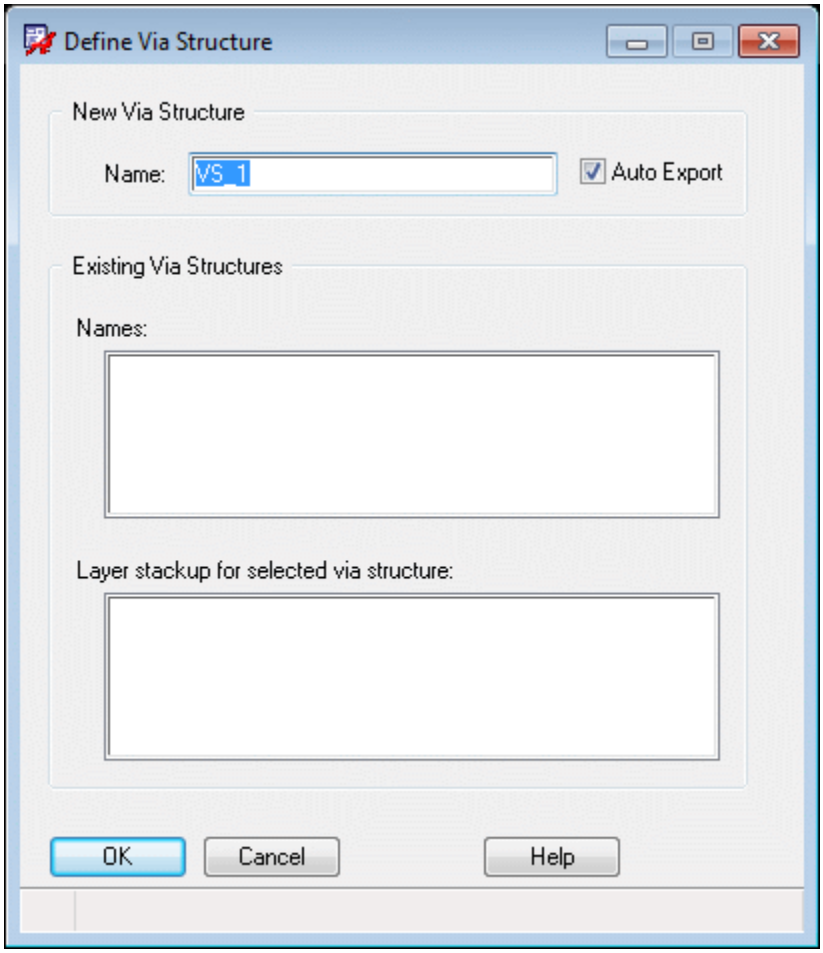
Via Structure Enhancements

The via structures feature has been enhanced with new options: *Create*, *Redefine*, and *Disband*. You can now create two types of via structures, *Standard* and *High Speed*.



- Standard
  - Target Use Model: Single net trace/via structures and Fan-out
  - Supported Objects: Traces, Vias
  - Connectivity: Physically connected single net
  - XML file: Not encrypted (.XML)
- High Speed (Requires *Cadence SiP Layout XL*)
  - Target Use Model: Differential pair via transitions with return path vias and custom voids
  - Supported Objects: Traces, Vias, Static Shapes (no voids), Route Keep out
  - Connectivity: Multiple nets
  - XML file: Encrypted (.eXML)
  - Allegro PCB/SiP – Sigrity Integration

A new option, *Auto Export* (selected by default), is available to automatically export an XML file which can be used to import or export via structure definition in other Allegro PCB/SiP databases and Sigrity 3DEM (High Speed only).



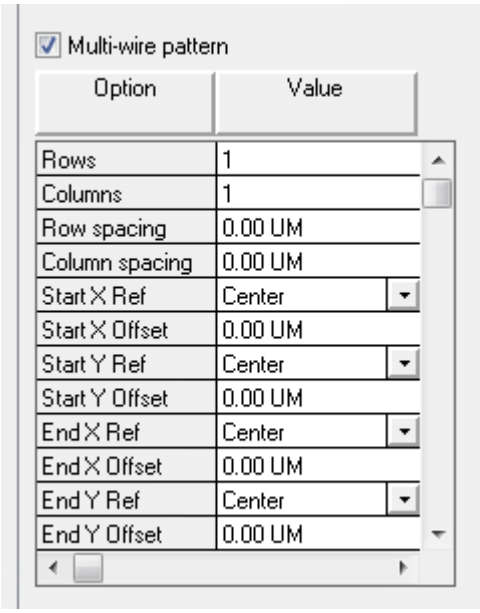
The *Redefine* command lets you select a modified via structure instance and update definition of all placed instances to match the selected instance.

The *Disband* command lets you select via structures and convert into their component cline parts.

In addition, now you can lock a via structure from the right-click pop-up menu (*Lock Via Structure*) to avoid unintentional changes. You can also unlock a via structure (*Unlock to Edit*).

Note: For more information, see the *Creating and Using Via Structures* section of the *Defining and Developing Library* User Guide.

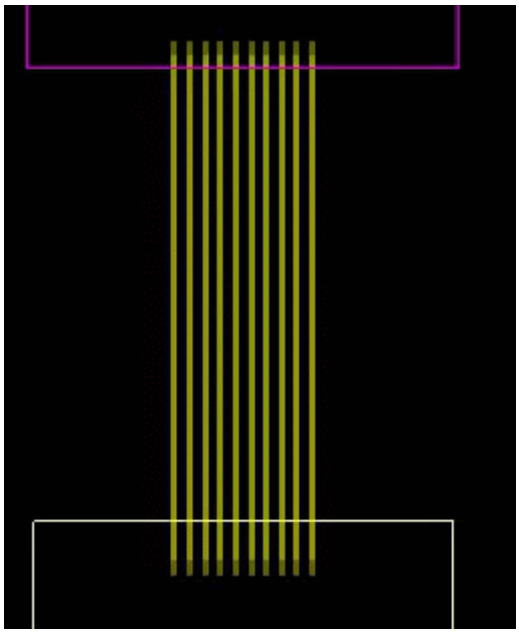
Adding Arrays of Bond Wires



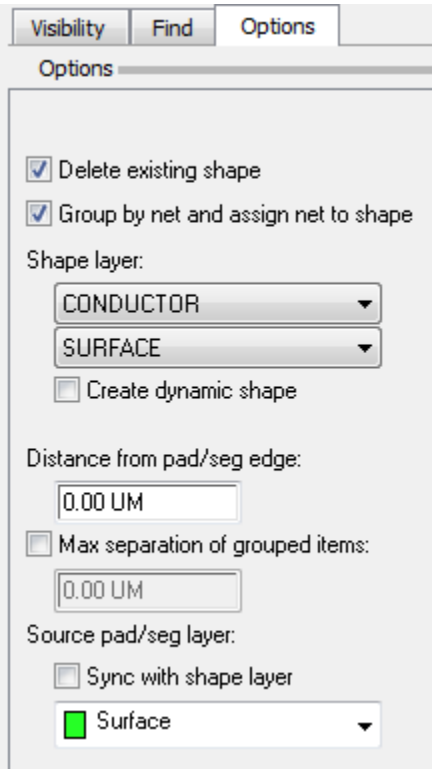
You can now create arrays of bond wires for high-current devices and redundancy by using the *Route – Add/Edit Non-Standard* command.

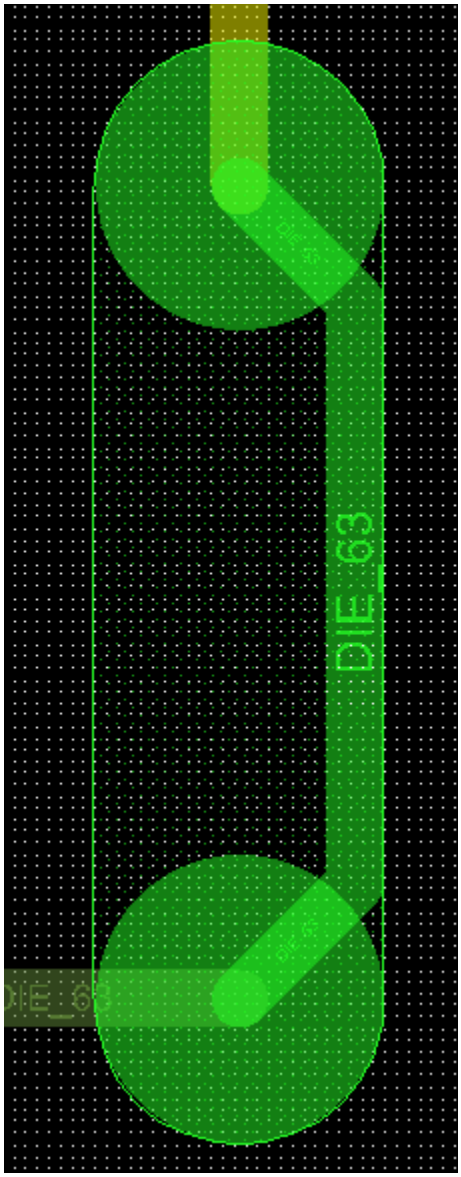
Enable the *Multi-wire pattern* option in the Options pane and then define the array using the two-column grid. You can define rows that define a set of wires, columns that define the number of wires in each set of wires or row, spacing between wire sets and wires within each set, and the start and end by setting offsets and specifying references.

For example, the following image illustrates a bond wire array consisting of two rows and ten columns.



Creating Bounding Shape





You can now create a convex hull around a set of selected pins, vias, fingers, or cline segments using the *Create Bounding Shape* option of the *Shape* menu.

Including Scribe Dimensions of Dies

You can now include scribe dimensions in extent/size information as well as in exported dies.

By selecting the *Unscribed size* option in the *Export Die Text-Out Wizard Header Information* page of the Die Text Out wizard, you can specify whether the extents or size information exported for the die includes scribe dimensions.

Similarly, in the *Subtract scribe size from die extents* option of the APD2AIF dialog box you can select whether to include scribe dimensions for exported dies.

Including Wire Length Summary in Wire Bond Report

Material ordering becomes easier because of the *Show wire length totals* option of the Wire Bond Reporting dialog box. This dialog now includes a summary table of total wire lengths broken down by material and wire diameter.

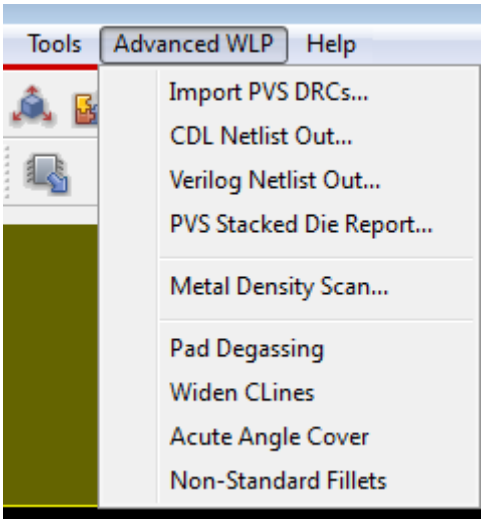
Including Data Type in Subclass Name while Importing Streams

You can now ensure unique mapping of objects for easier intelligent database creation during *Tools – Convert* and also during compose die from geometry. While importing a stream, set the Include data type option of the Stream In Edit Layer Mapping dialog. Setting this option includes the data type as part of the subclass name. The format of the subclass name is `<subclass>_<data type>`.

Unsupported Prototype Feature: Advanced WLP Capabilities

You can explore the unsupported prototype feature that provides various advanced wafer-level-chip-scale-package capabilities in addition to the already existing capabilities in SiP Layout. To access and explore these options, select Advanced WLP as a product option while launching SiP Layout XL.

Access the features from the *Advanced WLP* menu.



Allegro Sigrity PI and SI

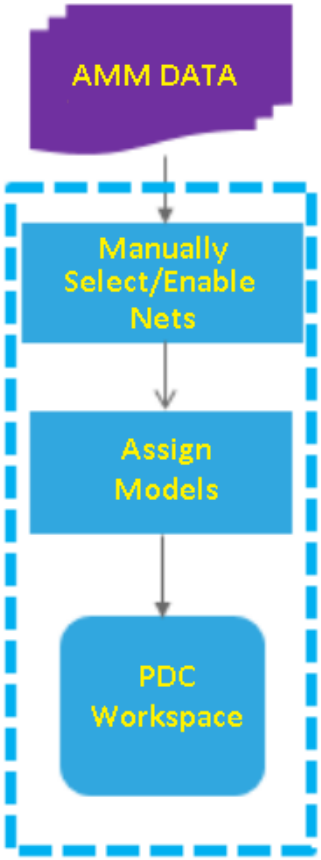
Allegro® Sigrity™ PI and Allegro® Sigrity™ SI include the following new features and enhancements in release 17.2-2016.

Allegro Sigrity PI

Enhancements in AMM Integration with PowerDC

Using pin-based Analysis Model Manager (AMM) helps you achieve the IR drop setup automation in PowerDC for assigning models and creating VRM/Sink components. In Release 17.2-2016, AMM is tightly integrated with PowerDC. The main tasks in the AMM-PowerDC workflow include:

- Preparing AMM data
- Manually selecting power/ground nets
- Assigning models to the selected nets
- Automatic creation of workspace



For AMM-based model assignment, the following functions are available in PowerDC:

- Automatic matching devices with model names
- Manually assigning models, if required
- Displaying instances or models
- Cross-probing between the Model Assignment dialog and PowerDC layout
- Exporting or importing mapping information
- Displaying model status indicator
- Sorting of instances or models

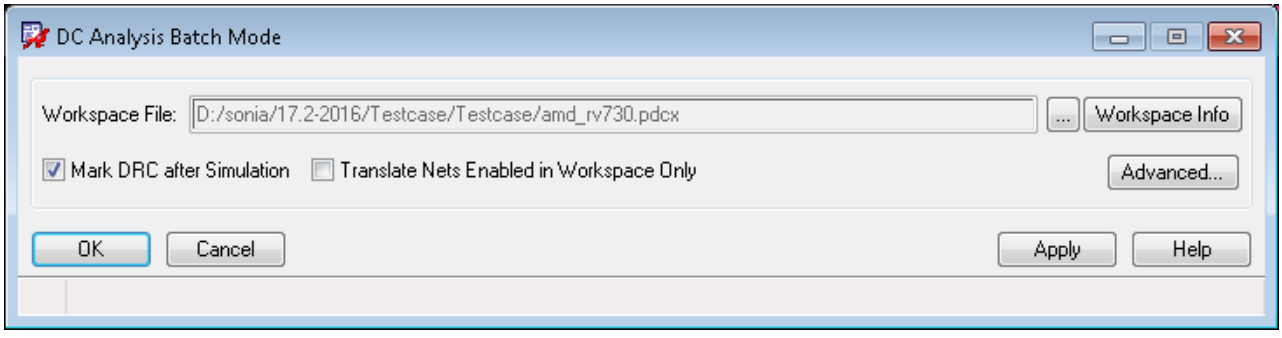
For more information, see the *PowerDC User Guide* in Sigrity 2016 installation.

Running DC Analysis in Batch Mode

A new method provided in PI Base enables you to run DC analysis in the Allegro layout environment, without launching the PowerDC user interface. You specify a workspace that includes all the settings for the simulation. An HTML report is generated and displayed after the simulation.

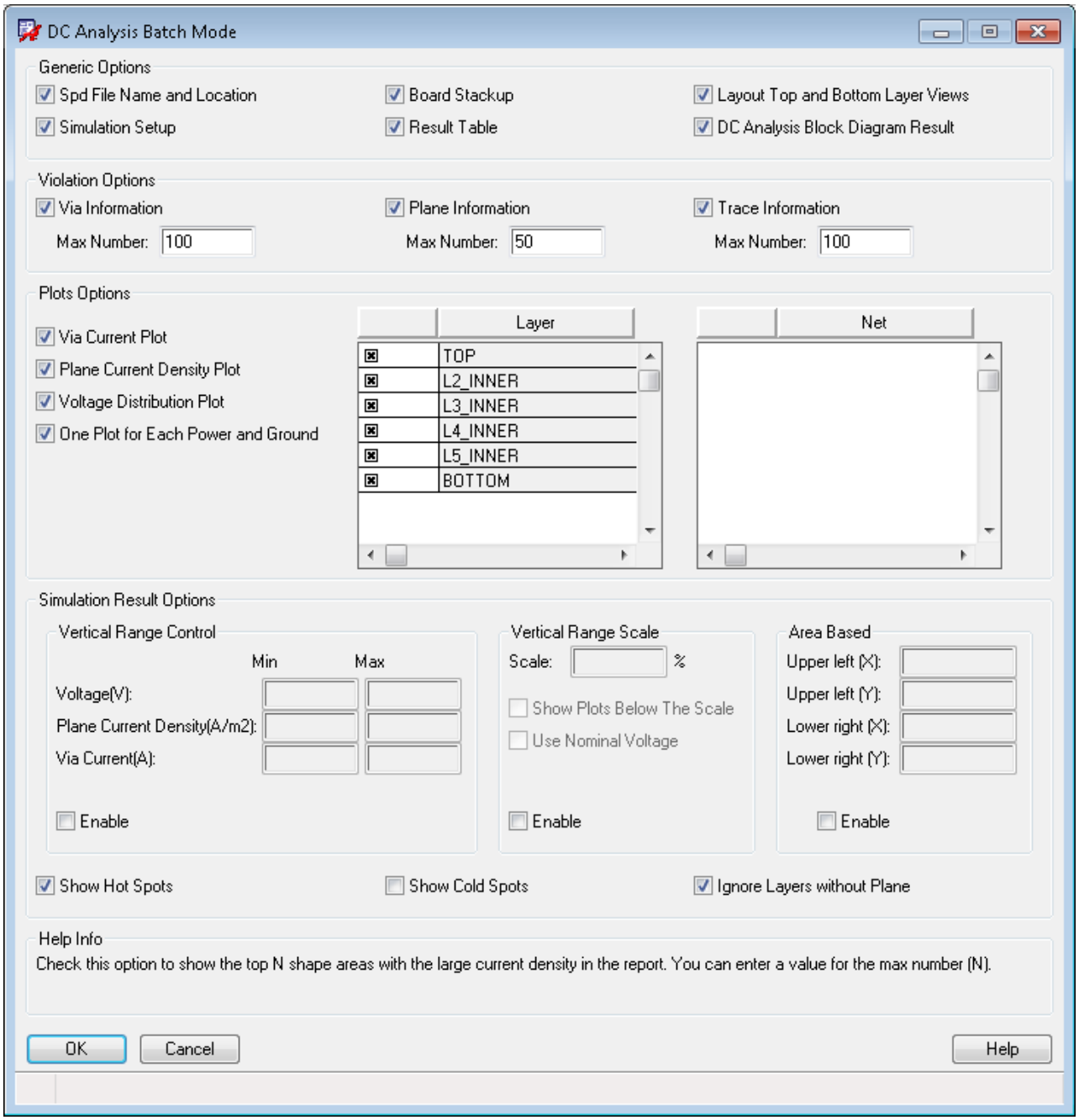
Key features include:

- Cross-probing between the report and the Allegro layout
- DRC marks can be back annotated to the Allegro layout
- Workspace settings can be reused
- An option is provided to control the nets to be translated from the workspace



Advanced Options to Control DC Analysis Report

There are new options to generate specific distribution plots in the DC analysis report. You can set these options in the DC Analysis Batch Mode – Advanced dialog:

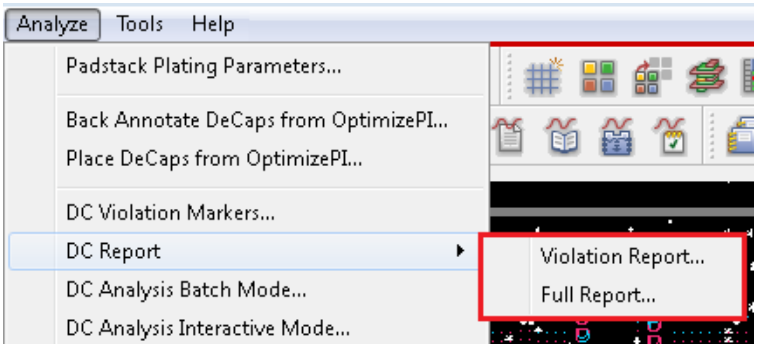


For more information on DC analysis in batch mode, see *Allegro Sigrity PI Flow Guide*.

DC Analysis Reports

DC Analysis reports are now available from the new *Analyze – DC Report* menu:

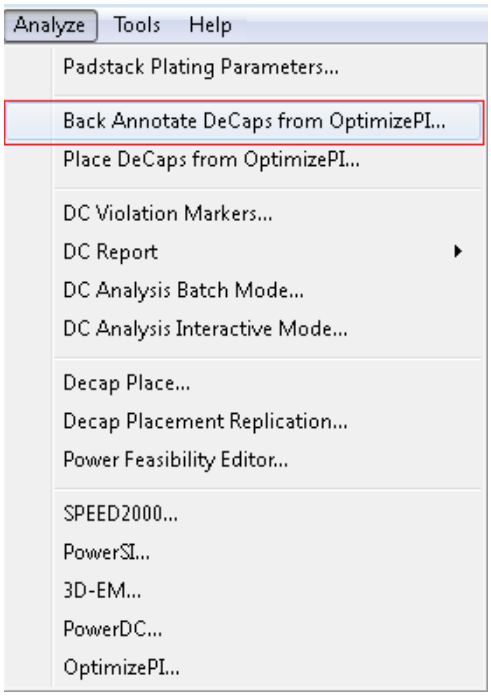
- Violation Report
- Full Report



For more information on DC analysis reports, see *Allegro Sigrity PI Flow Guide*.

Decap Backannotation from OptimizePI

In OptimizePI, you can remove decaps from an existing design, replace decaps, or add new decaps (for EMI decaps). All these changes need to be backannotated to the Allegro layout. In Allegro Sigrity PI, a new menu command, *Analyze – Back Annotate DeCaps from Optimize*, is added to help you backannotate the updated information in OptimizePI to the Allegro layout.



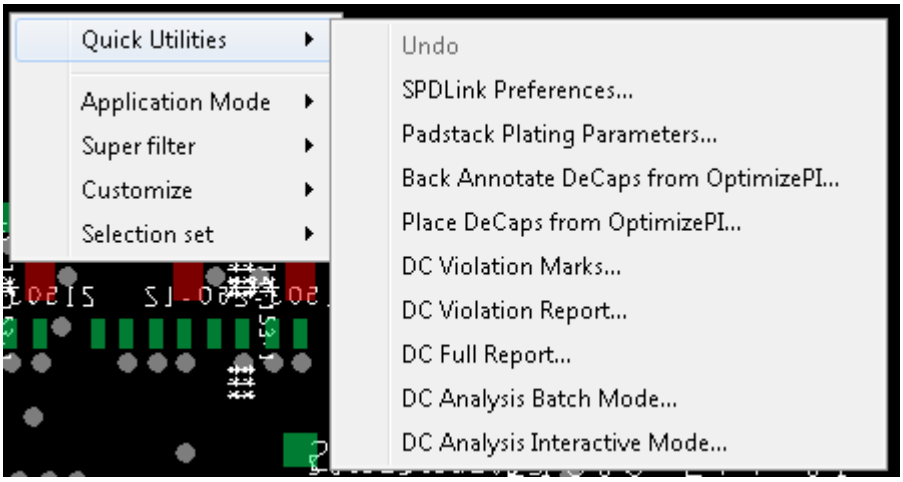
Run the simulation in OptimizePI, export scheme data, and generate netlist for backannotation. In Allegro Sigrity PI, use *Analyze – Back Annotate DeCaps from OptimizePI* to update decap information in the Allegro layout.

For more information, see *Allegro Sigrity PI Flow Guide*.

Miscellaneous Enhancements

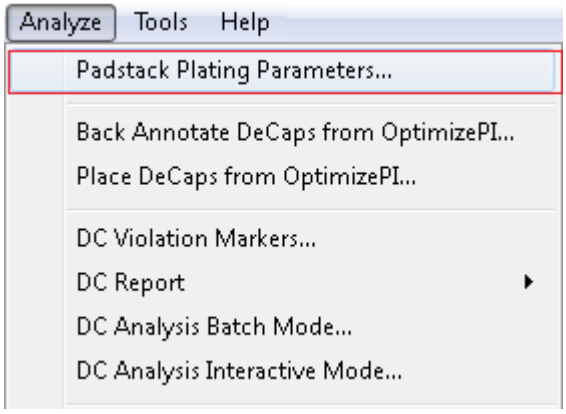
Commands Available in the Application Mode

All the Allegro Sigrity PI commands are now available from the Power Analysis application mode.



Padstack Plating Parameters

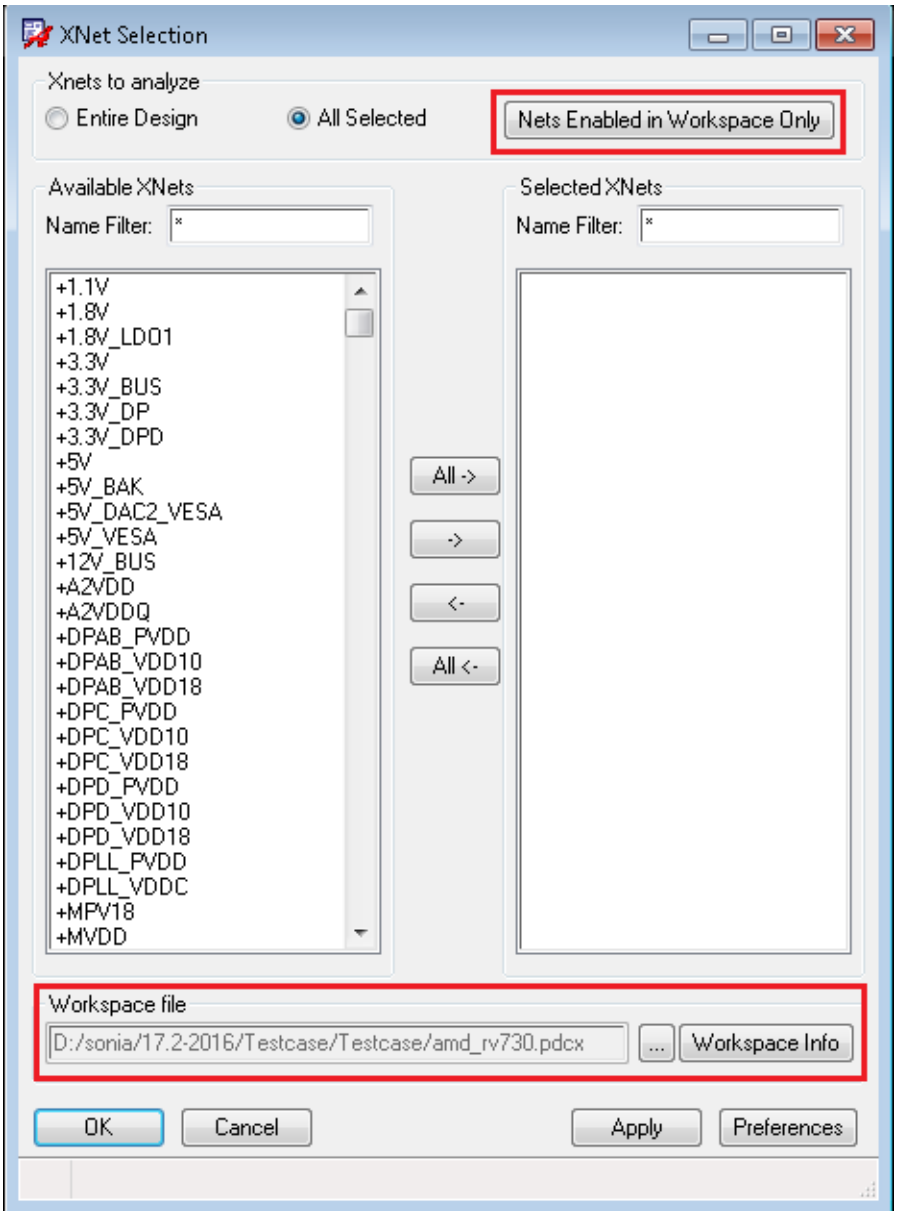
A new menu available from the *Analyze* menu helps you edit padstack plating parameters.



The resultant Padstack Plating Parameters dialog lets you import or export padstack plating parameters.

Net Selection from Workspace

When you run DC Analysis in the interactive mode, the Xnet Selection function now provides you the option to select only those nets which are enabled in the workspace. You need to select the workspace file before you click the *Nets Enabled in Workspace Only* button.



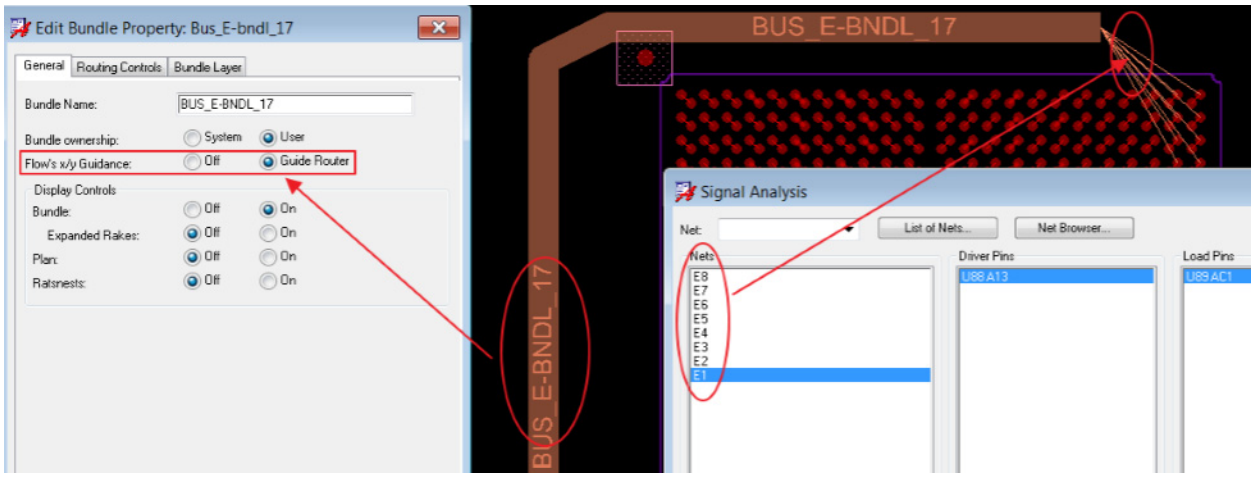
Allegro Sigrity SI

Support for Flow Planning

The Flow Planning functionality supported in Allegro PCB SI and Allegro PCB Editor is now available in Allegro Sigrity SI as well. The main function of Flowplanning is to drive routing. Functions such as creating bundles provide a simple and effective way to clean up the view of an unrouted design with jumbled ratsnest lines.

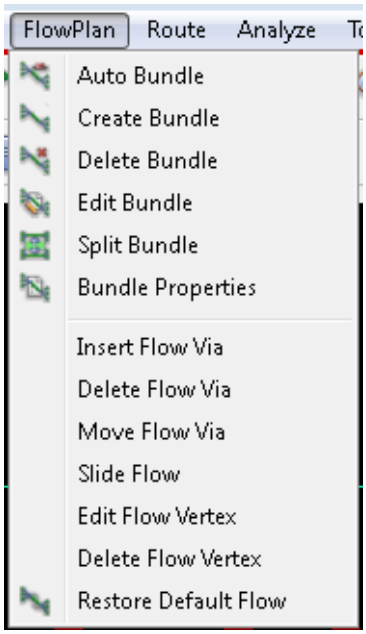
The additional feature in Allegro Sigrity SI is that the length of any flow can be taken into account for unrouted interconnect. An unrouted interconnect is simulated based on one of the two scenarios:

- If the net is a member of a bundle and the bundle is set to *Guide Router* for the *Flow's x/y Guidance* property, instead of the manhattan distance, the length of the flow is used and the Percent Manhattan setting in the Analysis Preferences dialog is ignored.

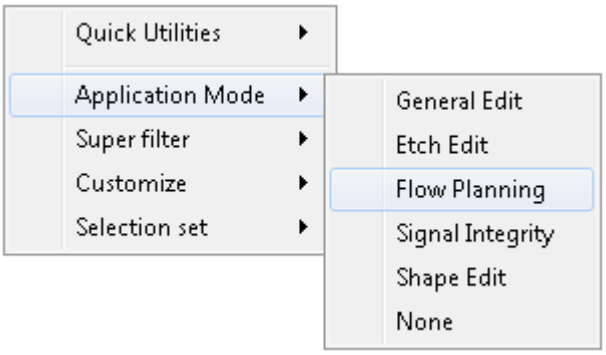


- If the net is not a member of a bundle or if the *Flow's x/y Guidance* property for the bundle is set to *Off*, the manhattan distance is used and the Percent Manhattan setting is applied.

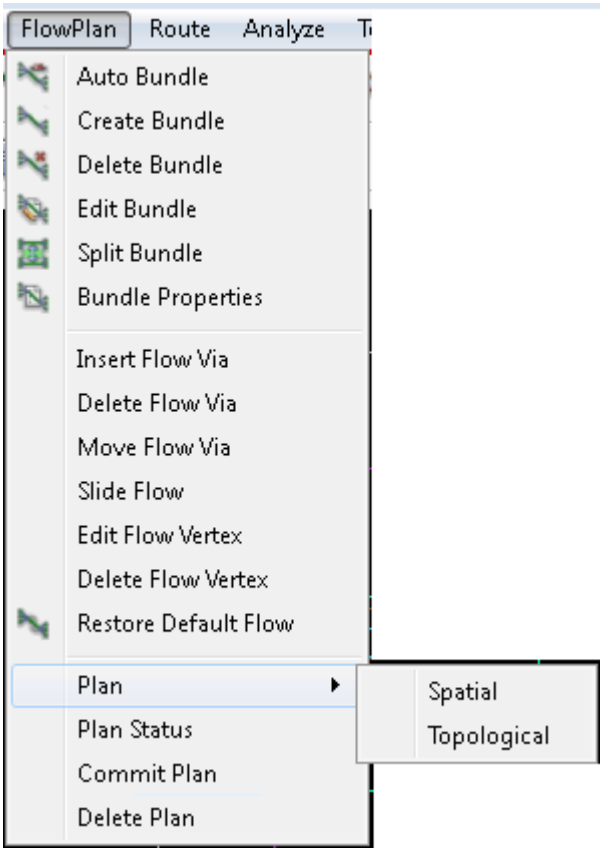
You can access the flow planning functionality from the *FlowPlan* menu. The commands are also available in the *Flow Planning* application mode.



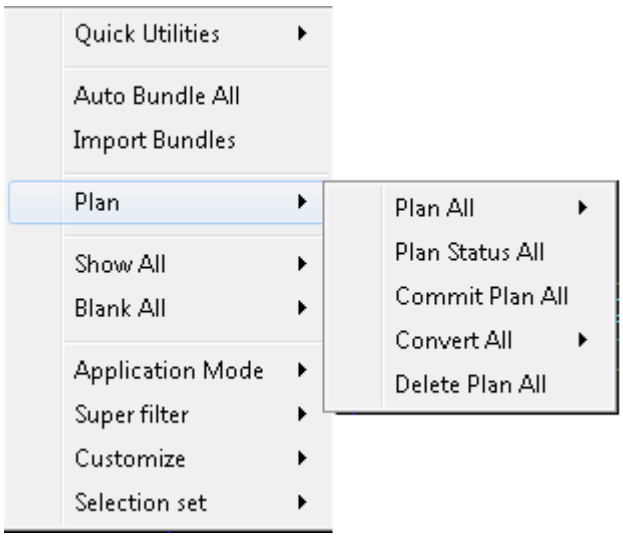
FlowPlan menu
without the Design Planning option



Flow Planning Application Mode



FlowPlan menu
with the Design Planning option



Flow Planning commands in the
Application Mode
(with the Design Planning option)

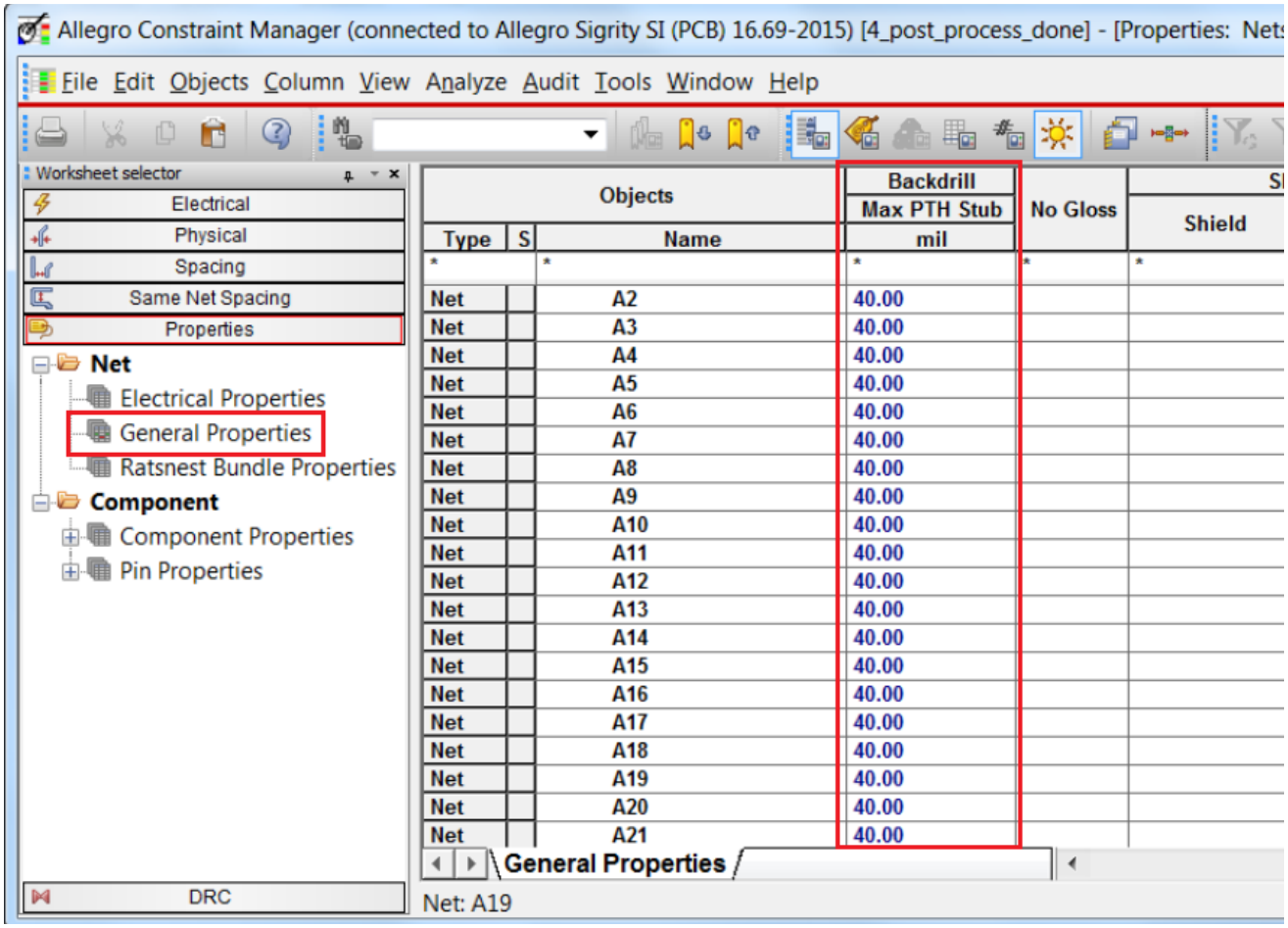
For more information on FlowPlan and its commands, see the following help documents:

- *Allegro User Guide: Working with Global Route Environment*
- *Allegro PCB and Package Physical Layout Command Reference* in Cadence Help.

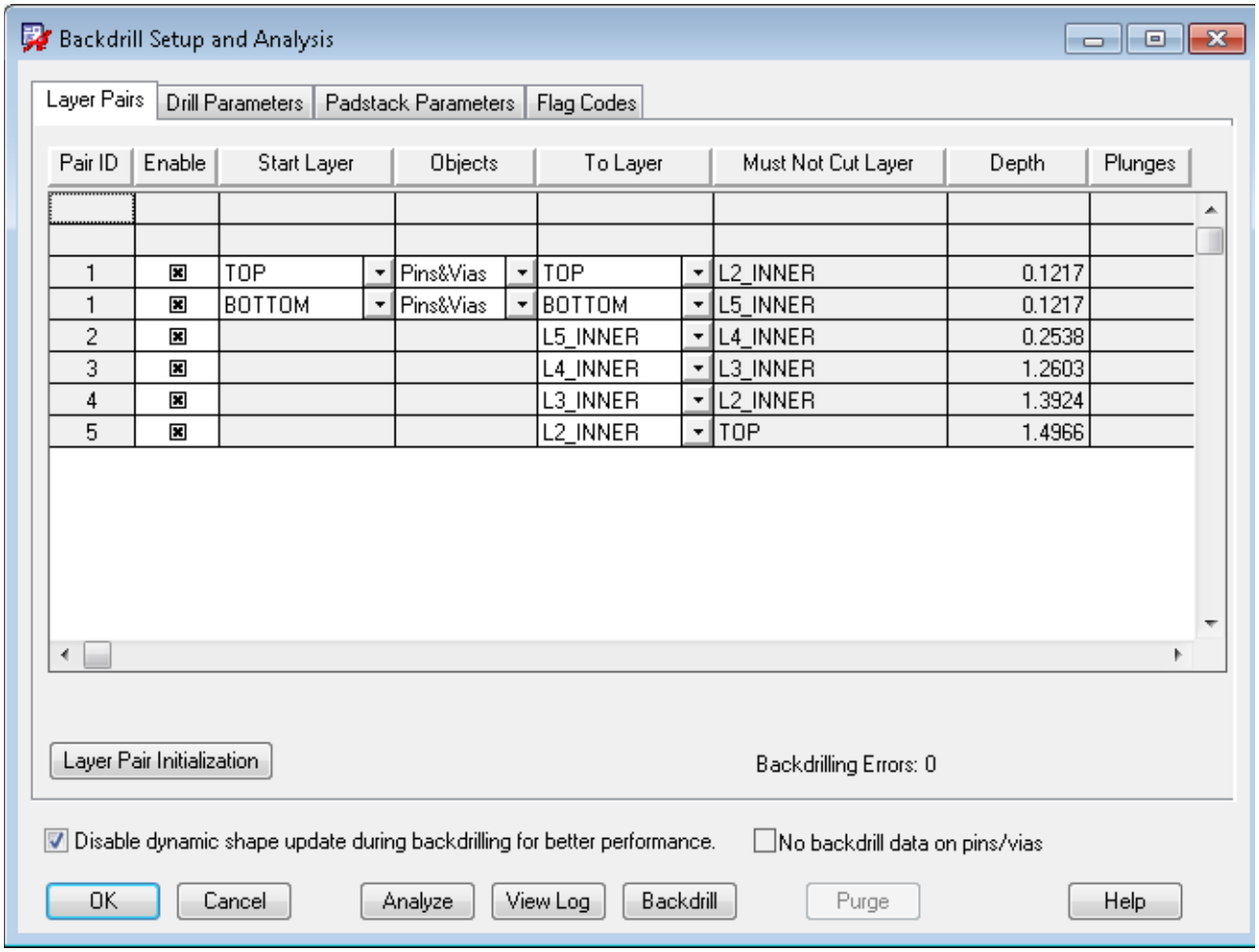
Backdrilling Solution for Allegro Databases

Backdrilling information can be translated to Cadence Sigrity applications based on settings and properties in the Allegro layout database. The solution is only available in the new integrated translator and not from SPDLinks. The process uses a combination of the `BACKDRILL_MAX_PTH_STUB` net property and settings for the Backdrill Setup and Analysis command.

The net properties can be accessed in Constraint Manager in the *Properties > Net > General Properties* worksheet



In Allegro PCB Editor, the *Manufacture – NC – Backdrill Setup and Analysis* command can be used to control the backdrill layer combinations. The default setting is to backdrill from the Top and Bottom layers to All layers.



In Allegro PCB Editor, the Backdrill application has undergone significant enhancements in this release. For more information, see *Allegro PCB Editor: What's New in Release 17.2-2016*.

Allegro Design Entry HDL

Allegro® Design Entry HDL includes the following new features and enhancements in 17.2-2016 release.

Enhancements in Allegro Design Publisher

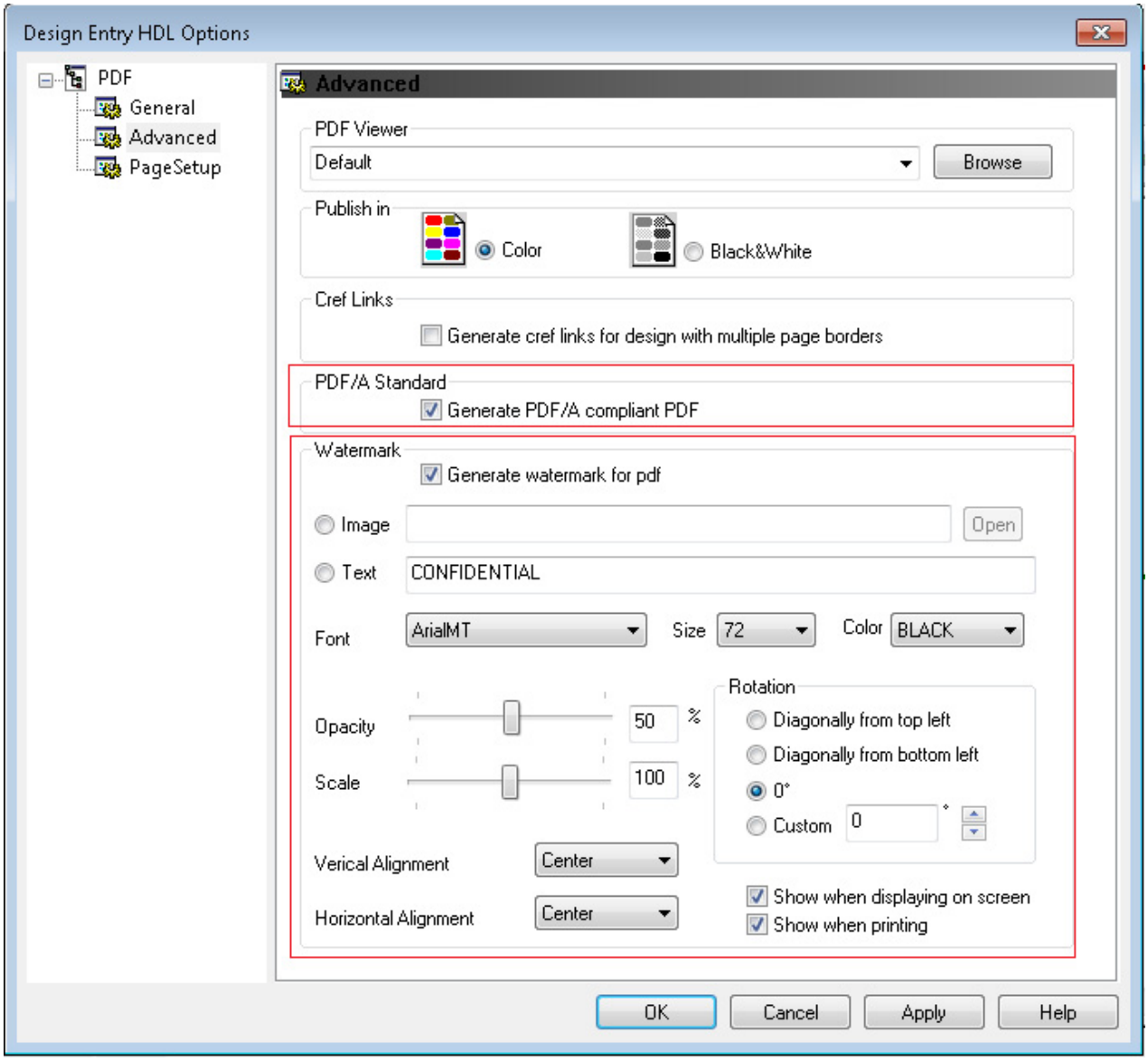
Allegro Design Publisher includes the following enhancements:

- **Watermark Support**

  When generating PDF from Design Entry HDL, you can now add watermarks to the PDF document. The Watermark section can be configured from the PDF Publisher setup. You can specify whether you want to view the watermark only in the print version or in the PDF document as well.

■ PDF/A Support

Allegro Design Publisher now allows you to generate archived PDF (PDF/A) files that conform to the PDF/A-1b standard.



For more information, see the *Setting up Advanced PDF Options* section in the *Exporting Schematics to PDF* chapter of *Allegro Design Publisher User Guide*.

Constraint Manager Database Changes

In the 17.2 release, the Constraint Manager (*.dcf) file format has changed. The *.dcf file, which was a text file earlier, is now a single file in binary form. This change enables better performance of the Constraint Manager database. For details, see *Allegro® Design Entry HDL – Constraint Manager User Guide*.

Allegro FPGA System Planner

Allegro® FPGA System Planner includes the following new features and enhancements in release 17.2-2016:

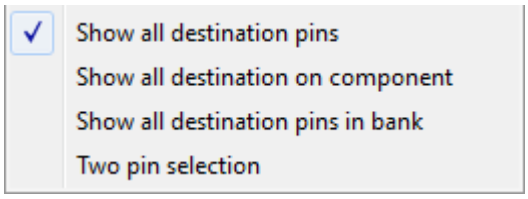
Enhancements in FSP - Allegro Integration Flow

Swapping Pins and Bundles

You can swap pins and bundles across multiple custom connectors. For example, if a bundle is connected to instances U1 and U2, you can now swap the pins of U1 with the pins of U2. You can also continue to use the existing auto pin swap features such as rake order optimization.

Manual Pin Swap Command

The Manual Pin Swap command is enhanced and provides you options as illustrated:

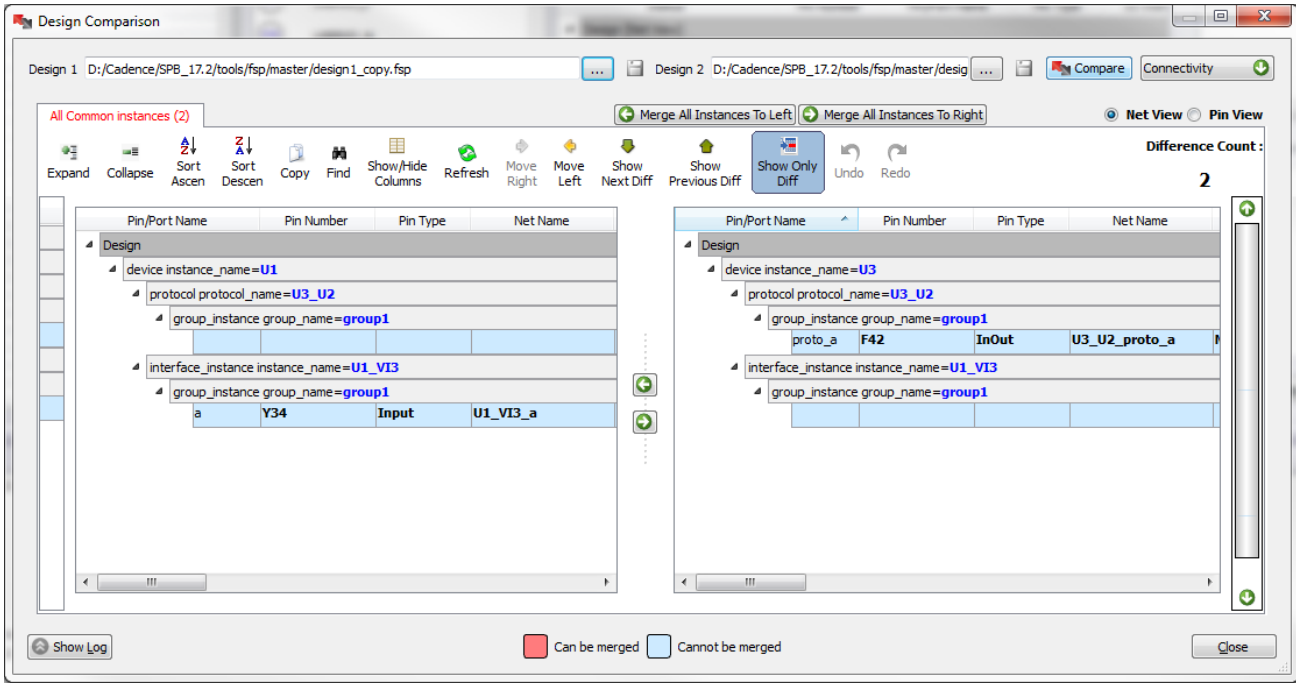


Support for Multiple FSP Designs

In the FSP - Allegro Integration flow, you can now work with multiple FSP designs and integrate them into your master design.

GUI Enhancement

The Design Comparison dialog box displays design information in an instance tree view structure.



Allegro EDM

Allegro® Engineering Data Management (EDM) includes the following new features and enhancements in release 17.2-2016:

Enhancements in Design Management Solution

The Allegro Design Management solution includes the following new features and enhancements in release 17.2:

- Page-level Design Management Support
- Allegro Design Management Integration in Design Entry HDL
- Data Management Support

For details, see *Allegro Design Management User Guide*.

Page-level Design Management Support

With release 17.2, page-level management for flat designs is supported in Allegro Design Management. Multiple designers can now work in a team-design environment on a flat design and manage designs at the page level as well as at the constraint view level.

Important

Page management is not supported for cache-enabled designs.

Allegro Design Management Integration in Design Entry HDL

In this release, design management is seamlessly integrated with Allegro Design Entry HDL. All design management operations are now available from within DE - HDL, eliminating the need to use a separate tool to manage objects.

You can now view the status of a design from within DE-HDL using the dashboard. You can also use the DE-HDL hierarchy viewer and menu options to quickly manage team design operations.

Allegro Design Management helps you:

- Prevent unintended modification of a design by controlling access to projects
- Provide version control and version history for all design changes
- Manage design modifications from multiple sources/sites
- Facilitate communication/notifications among the design team
- Maintain the design data at a central location

- Integrate all design components into a released design

Data Management Support

Data management is now supported in DE-HDL. You can use this new feature to create project teams and assign users at the project level, allowing designers to work on projects to which they are added as team members. All design projects, whether in Allegro Design Management or DE-HDL, can be stored in a managed location. This helps you exercise greater version control, and ensures adherence to company-wide data storage policies.

Hierarchical Split Symbol Support

The Allegro EDM flow includes end-to-end support for hierarchical split symbols, from library import to using symbols in the design flow including the team design flow. You can import, create, and manage hierarchical split symbols in the Allegro EDM component database.

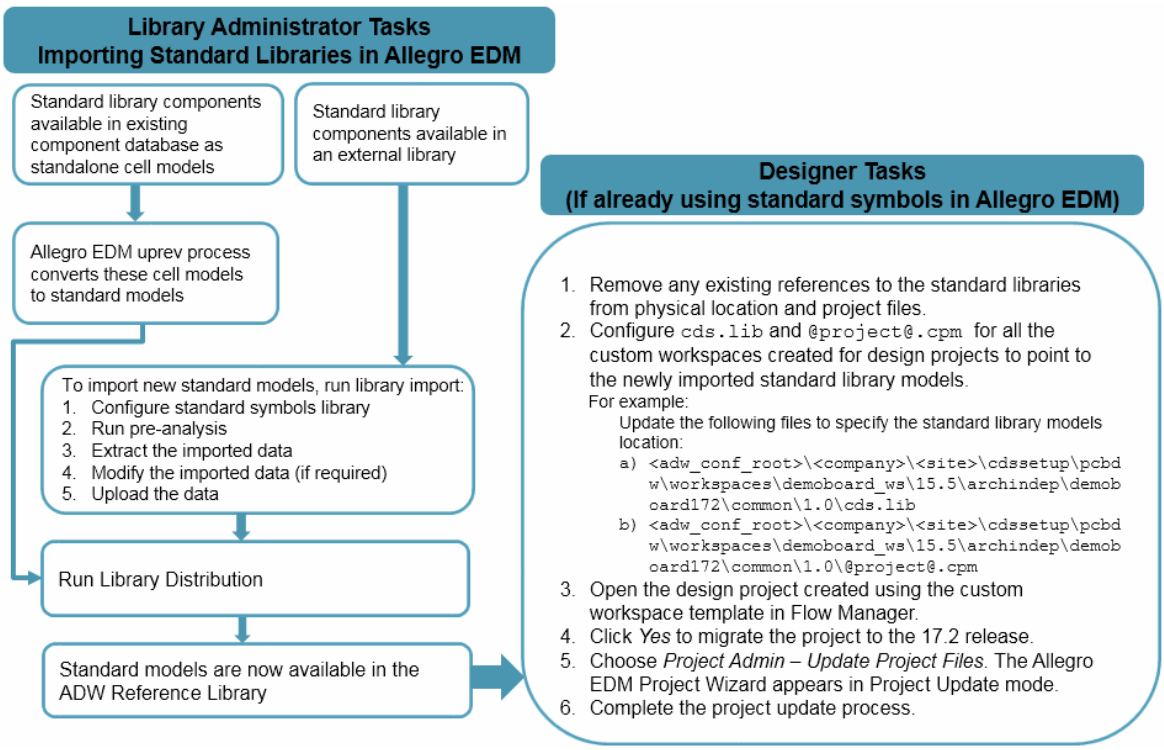
Standard Library Support

Component libraries that contain standard symbols are now supported in Allegro EDM. You can configure and import these symbols as standard models into Allegro Library Manager.

- Prior to this release, these symbols were used in the component database as standalone cell models. With this enhancement, the Allegro EDM uprev process (`adw_uprev` run while migrating to the 17.2 release) converts these cell models to standard models.
- To import new standard models, perform the following tasks:
  a. Configure standard models.
  b. Run pre-analysis.
  c. Upload library data.
- If you are using standard models in Allegro EDM projects, you need to update the design projects to manage these standard models.

For detailed information, see *Allegro EDM Library Import User Guide*.

The following diagram illustrates the standard library support flow.



Allegro Constraint Manager

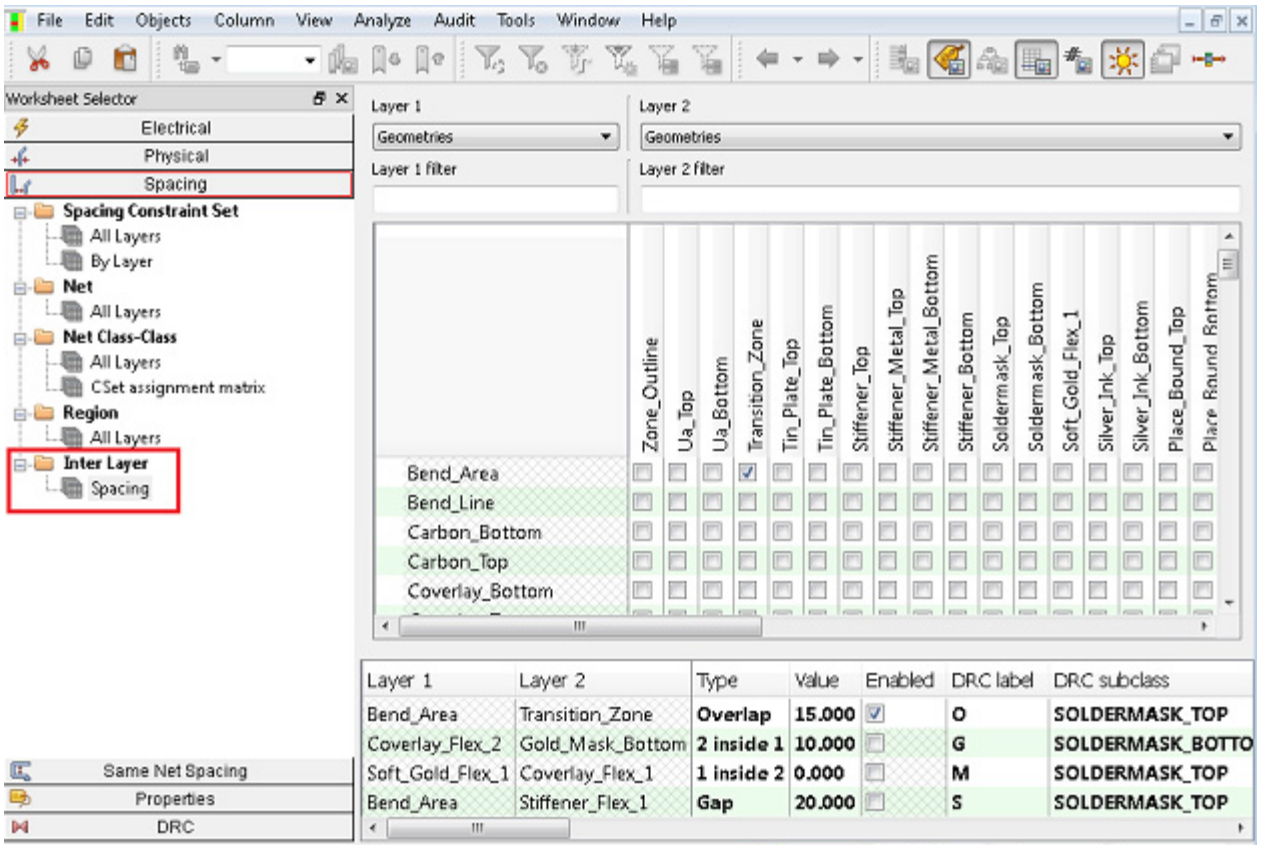
Allegro® Constraint Manager includes the following new features and enhancements in release 17.2-2016:

Inter Layer Spacing Constraints

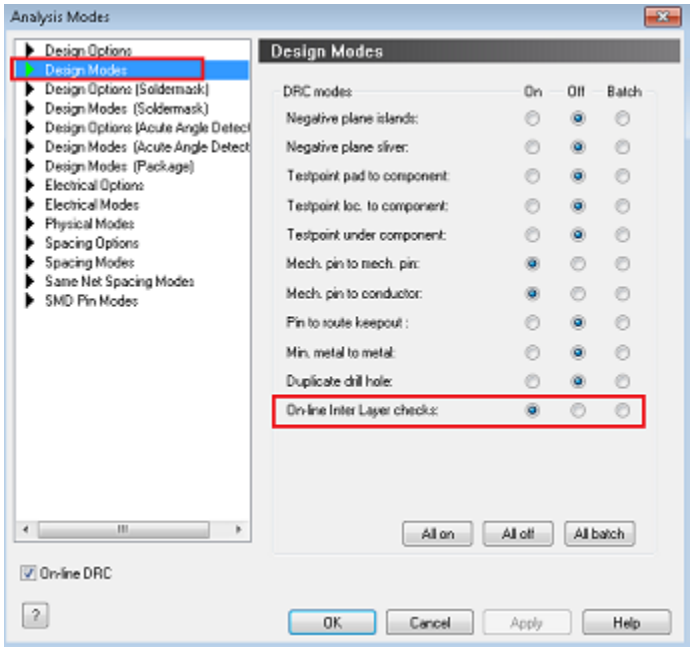
A new workbook, *Inter Layer* spacing, has been added in the *Spacing* domain, that compares geometries on two different subclasses. These checks are used for Rigid Flex designs, as well as single or multi-layer designs.

Inter Layer checks provide a new way of checking mask to mask and mask to other geometry types, and help in detecting errors earlier in the design to manufacturing cycle.

Inter Layer window displays a matrix of subclasses and a rule table. You can enable these constraints between two subclasses and analyze the result in PCB Editor.



To enable the inter layer checks, set the On-line Inter Layer checks as *On* in the *Design Modes* tab in the *Analysis Modes* dialog.

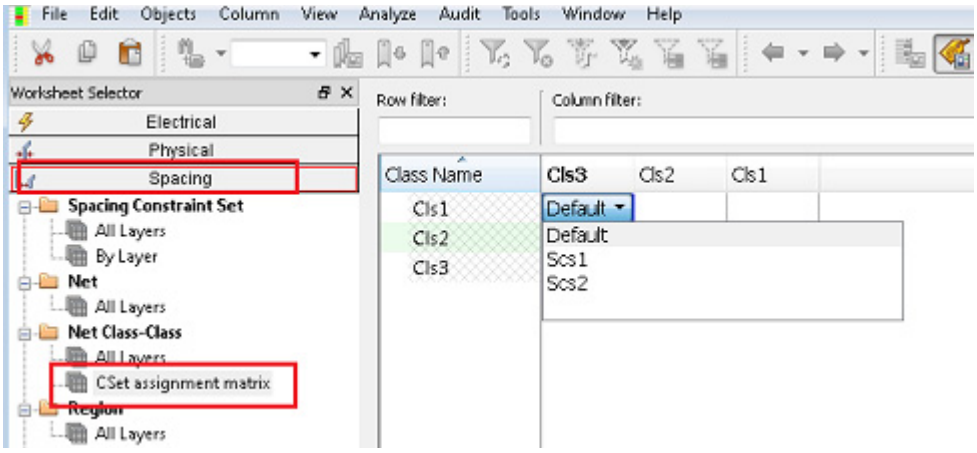


For more information on Inter Layer Spacing, refer to Inter Layer Spacing Checks in *Allegro Constraint Manager User Guide*.

CSet Assignment Matrix

A new *Cset assignment matrix* workbook has been added in the Spacing domain. This eases the process of creating and updating class-class relationships between Net Classes in the Spacing domain.

Select an SCSet in a cell to define the class-class relationship for that row and column.



For more information, refer to the *Creating Spacing Class Class* in *Allegro Constraint Manager User Guide*.

GUI Enhancements

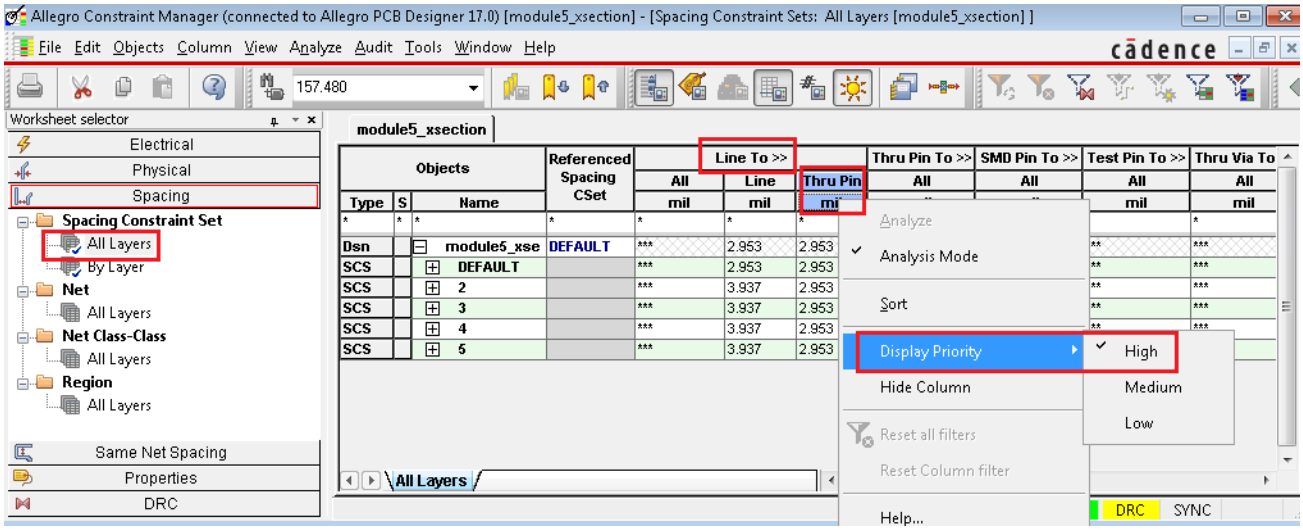
- Column Display Priority
- Super Attribute ALL
- Object Group Types
- Hierarchical Layer Support
- Alternate Rows Background Color
- Constraints Grouping in Spacing and Same Net Spacing Domains
- Show Group Members
- Improved Constraint Difference Report UI
- Drag and Drop Group Membership

Column Display Priority

In 17.2, Constraint Manager is enhanced to provide column display control for customizing worksheet appearance. A new command *Display Priority* lets you set the level of column display as high, medium, or low.

If the columns have different display priorities, the column headers are displayed with >>(show more) or << (show less) options. Double-clicking the column header either expands or collapses all the columns. The columns with high priority will always be displayed. Column hiding is still supported and a hidden column is not visible when cycling through the display priorities. You can see a hidden column using right-click customization commands in the Worksheet Selector or by using the *View – Show All Columns* command.

In the following figure, the display priority for the *Line to Thru Pin* column is high and the column is visible. The *Line To* column header with Show More option shows that other columns are hidden.

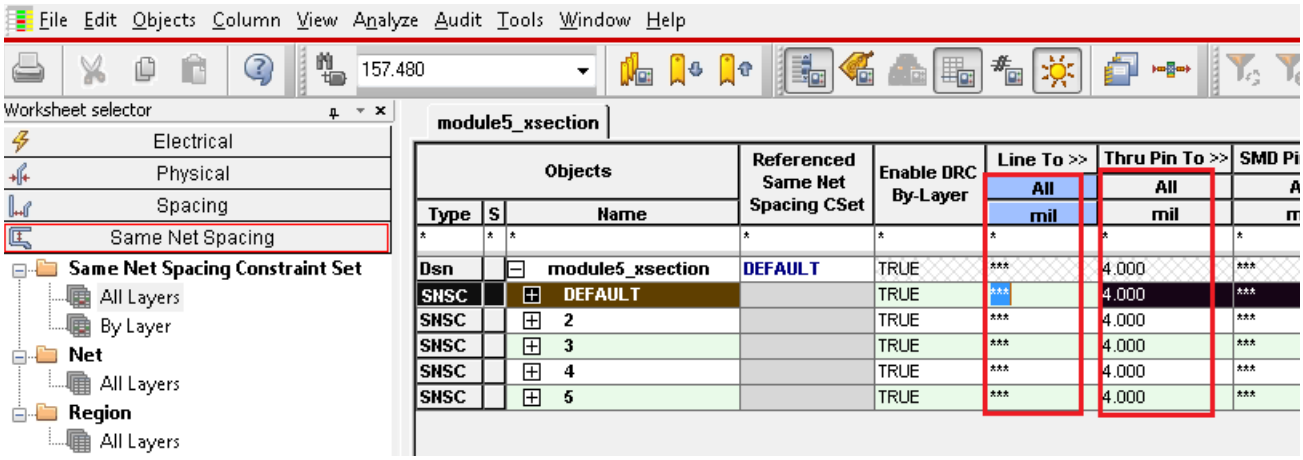


For more information, refer to the *View – Display Priority* command in *Allegro Constraint Manager Reference*.

Super Attribute ALL

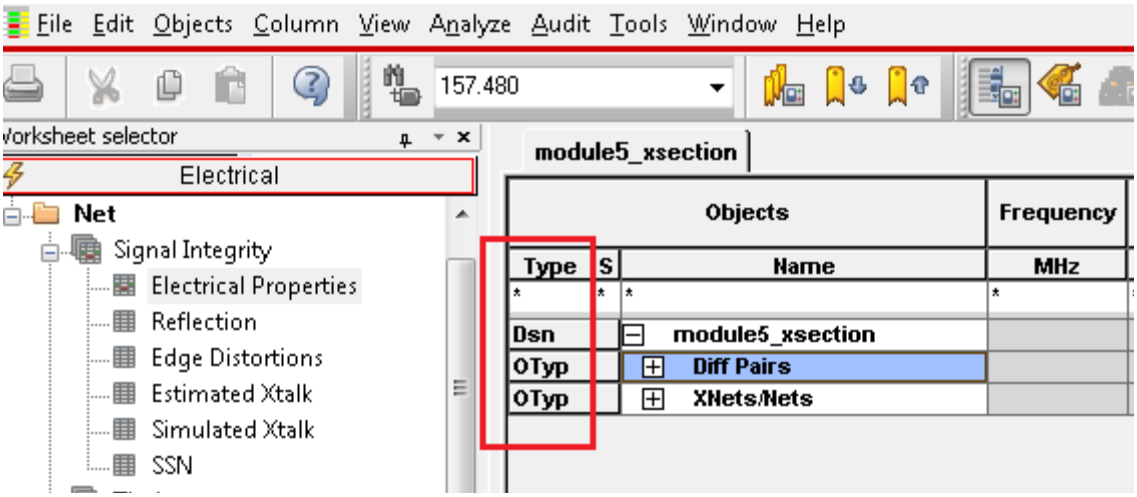
In the Spacing and Same Net Spacing domains, applying the same spacing constraints between one object type (for example, Line) and all the other object types (for example, Pins, Vias, and so on) is difficult. To minimize the effort, a super attribute type *All* is added to each spacing constraint. By setting the super attribute value, you can set all the related constraints

to the same value. If any related constraint has a different value, the value of the super attribute is displayed as ***. By default, the display priority of the super attribute is set as high.



Object Group Types

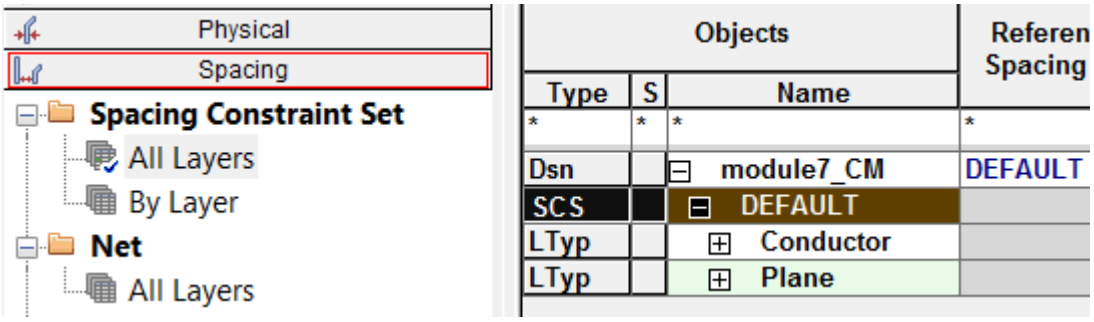
Another enhancement is made to customize the worksheet viewer. A new *Object Group Type* is added to group all the objects of the same type. You can expand the *Object Group Type* to view the objects.



For more information, see *Object Group Type* in *Allegro Constraint Manager User Guide*.

Hierarchical Layer Support

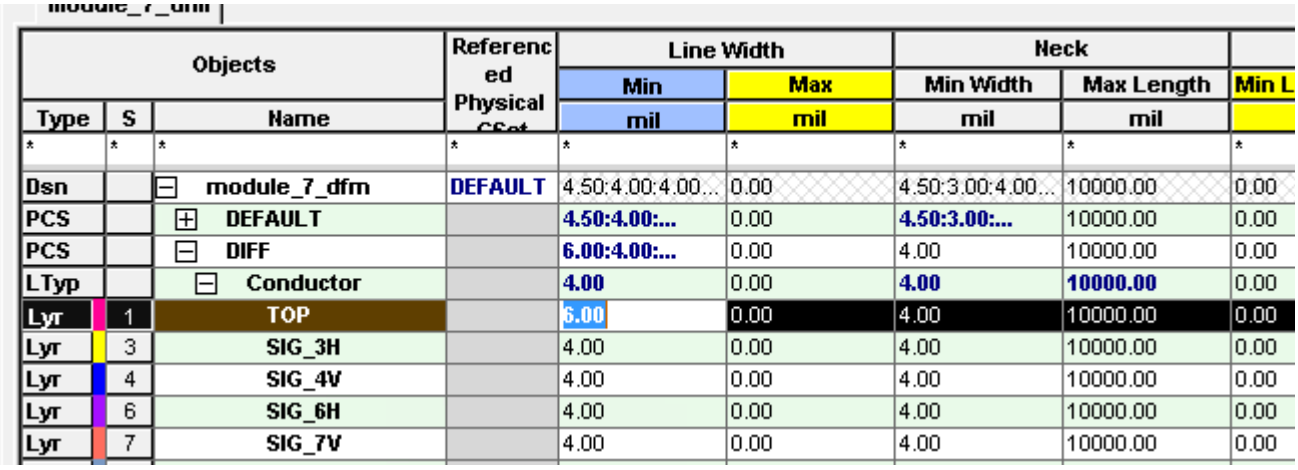
Another enhancement in release 17.2 has been made to ease the editing and reviewing of constraints. In Physical and Spacing domains, all the layers are now divided into two types; Conductor and Plane, known as hierarchical layer types. You can view and apply CSet values to hierarchical layers directly and the values will be inherited by the all child layers.



For more information, see *Hierarchical Layer Support* in *Allegro Constraint Manager User Guide*.

Alternate Rows Background Color

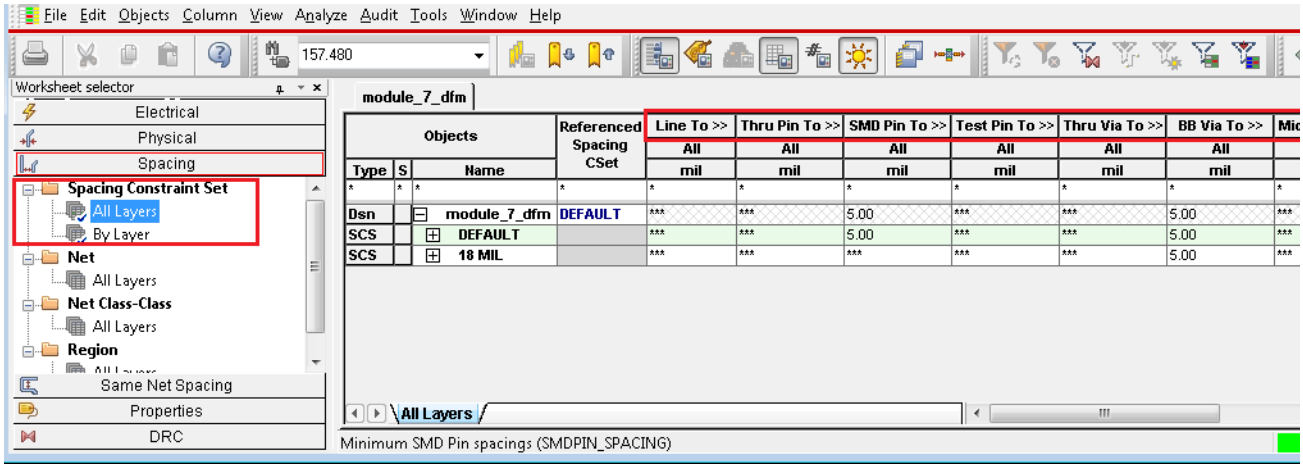
To improve the readability and comprehension, Constraint Manager assigns color to alternate rows. You can set the background color for alternate rows using the *View – Options – Colors* option.



Objects			Referenced Physical CSet	Line Width		Neck		
				Min	Max	Min Width	Max Length	Min L
Type	S	Name		mil	mil	mil	mil	
*	*	*	*	*	*	*	*	*
Dsn		module_7_dfm	DEFAULT	4.50:4.00:4.00...	0.00	4.50:3.00:4.00...	10000.00	0.00
PCS		DEFAULT		4.50:4.00:...	0.00	4.50:3.00:...	10000.00	0.00
PCS		DIFF		6.00:4.00:...	0.00	4.00	10000.00	0.00
LTyp		Conductor		4.00	0.00	4.00	10000.00	0.00
Lyr	1	TOP		6.00	0.00	4.00	10000.00	0.00
Lyr	3	SIG_3H		4.00	0.00	4.00	10000.00	0.00
Lyr	4	SIG_4V		4.00	0.00	4.00	10000.00	0.00
Lyr	6	SIG_6H		4.00	0.00	4.00	10000.00	0.00
Lyr	7	SIG_7V		4.00	0.00	4.00	10000.00	0.00

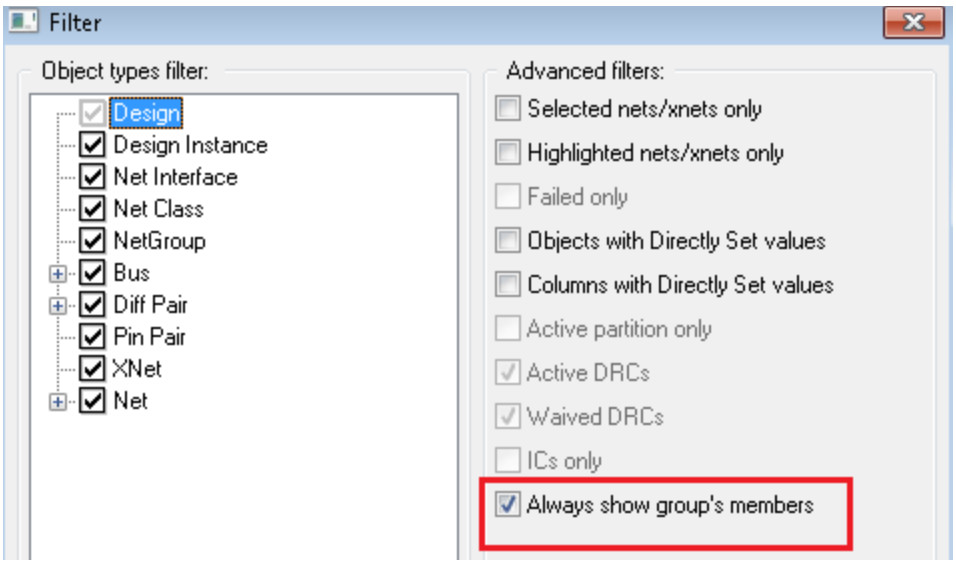
Constraints Grouping in Spacing and Same Net Spacing Domains

In the Spacing and Same Net Spacing domains, the constraints are grouped together and visible in a single worksheet.



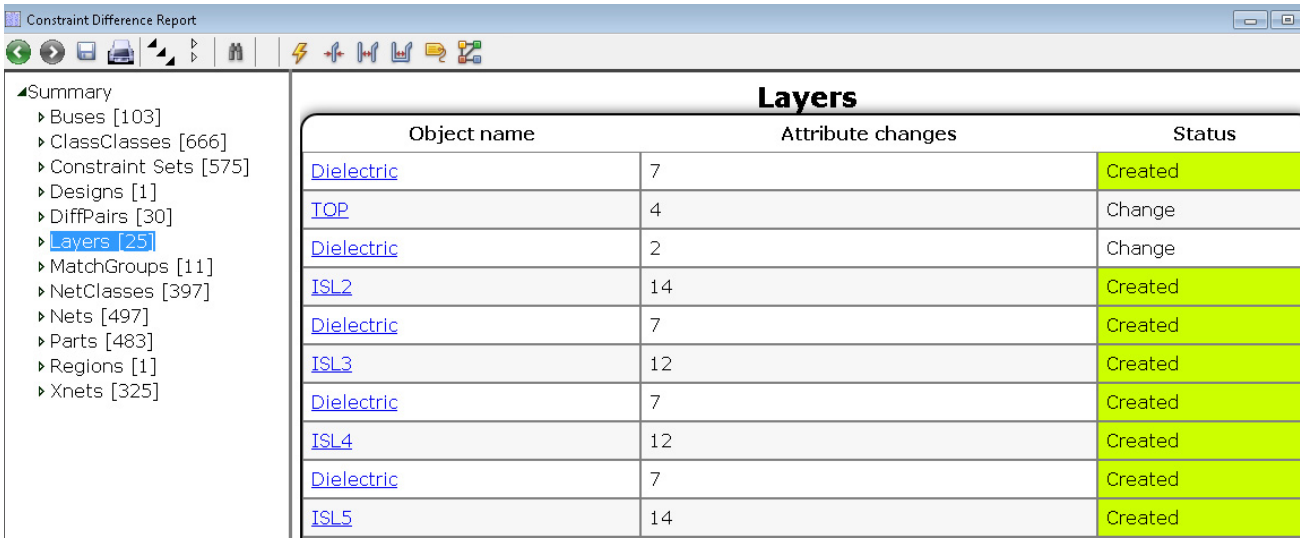
Show Group Members

A new advanced filter option *Always show group's members* has been added to the *Filter* dialog box. This option precedes object type filter settings and always displays members of a group (for example, Net Class or Net group) regardless of the object types (for example, nets) which are enabled. By default, this option is enabled. Deselect this option to work in the pre-17.2 mode.



Improved Constraint Difference Report UI

The constraint difference report UI has been upgraded in 17.2. This includes some style changes and the support to report the constraint differences on generic layers.



Drag and Drop Group Membership

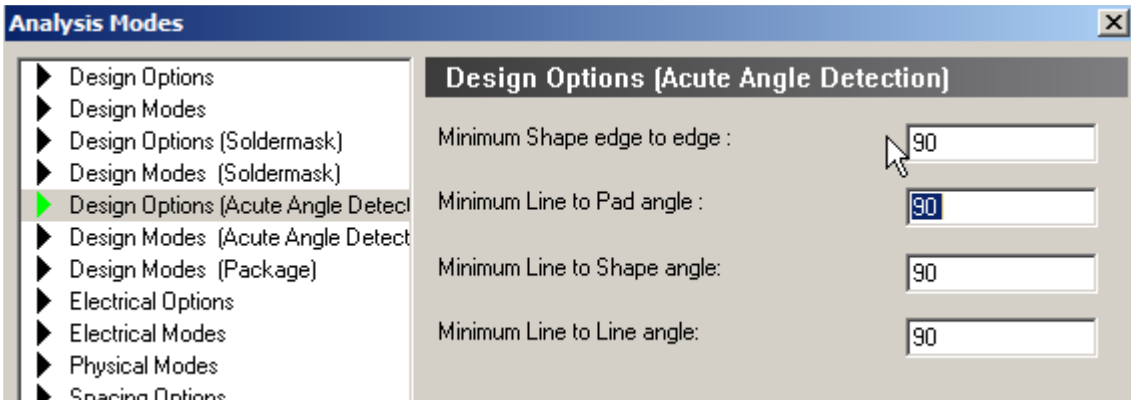
You can now perform drag and drop operations that provide a fast and easy way to add members to a group. Select a single or multiple objects at a time and add them to a group. This action is similar to the *Add to* command.

New DRCs

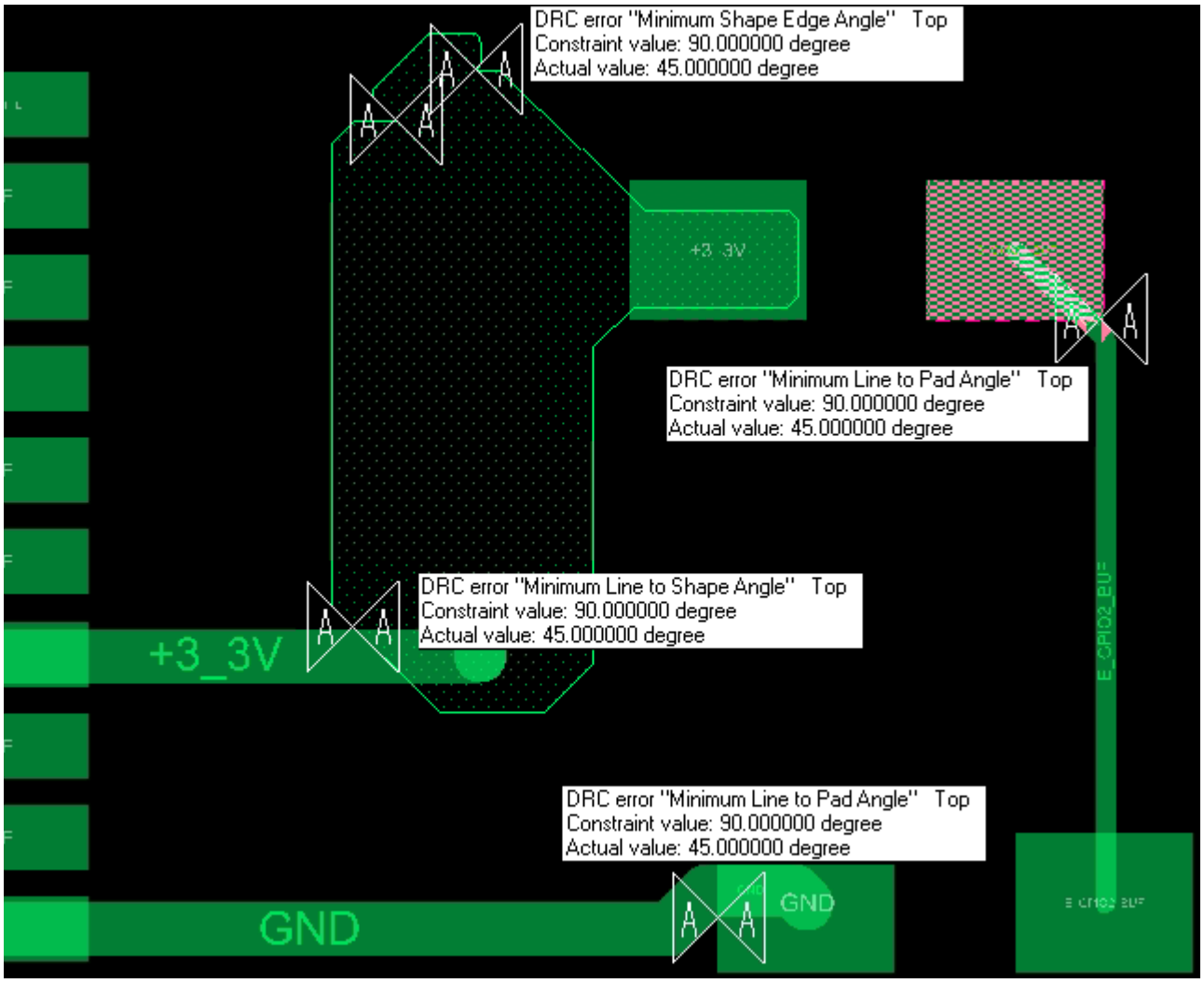
- Acute Angle Detection DRC
- Drill Hole DRC

Acute Angle Detection DRC

In release 17.2, a set of four angle-based checks are introduced at the design level. These checks measure the acute angle formed when two objects intersect. The valid objects are cline, shape edge, and pad edge. By default, these checks are disabled.



DRCs are created if the angle between objects is less than the specified value.

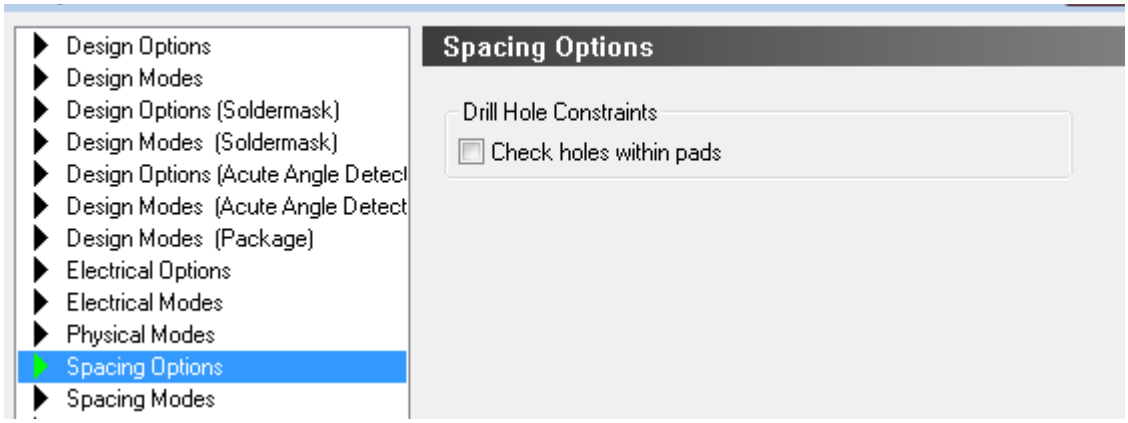


For more information, see *Design Modes (Acute Angle Detection)* in *Allegro Platform Constraints Reference*.

Drill Hole DRC

In the Analysis Mode dialog box, a new option, *Spacing Options,* is added to enable the drill hole checks in a design. If this option is on, the spacing between drill holes objects are

checked irrespective of the pad state (suppressed or unsuppressed). By default, this check is off.

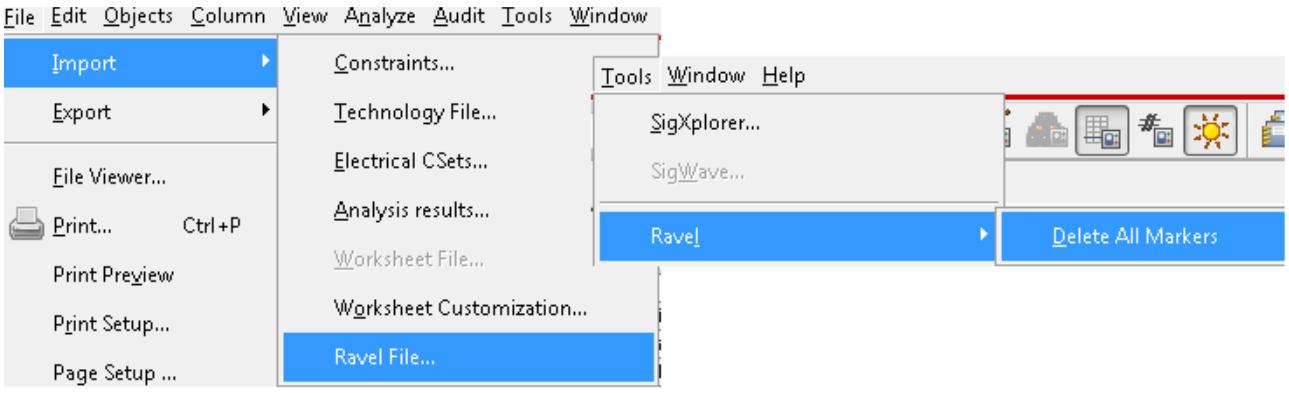


For more information, see *Spacing Options* in *Allegro Platform Constraints Reference*.

Ravel Checks Support

In release 17.2, Constraint Manager is enhanced to support the import and running of external constraint checks. These checks are advanced level design rules written in Ravel DRC language.

To provide Ravel checks support, two new commands *File – Import – Ravel* and *Tools – Ravel – Delete All Markers* are added to Constraint Manager.



You can run Ravel checks on a complete design. The DRC markers are created in the design where violations are found.

For more information, see *File –Import – Ravel* in *Allegro Constraint Manager Reference*.

Miscellaneous Enhancements

Change in Default Unit

The default units in Constraint Manager are now length-based. For example, units of Min/Max Propagation Delay are *mils* instead of *ns*.

Support for XML-based Constraint Files and Schema (XSD) Validation

In release 17.2, all Constraint Manager-owned files are based on the XML format. The following extensions are enhanced to support the XML format in this release:

- Constraints file (`.dcfx`)
- Technology file (`.tcfx`)
- Customization file (`.wcfx`)

If you edit or create any of these files, a corresponding schema (XSD) is also available to validate the structure of the edited file. The schema validation files exist in your `<installation_directory>/share/pcb/consmgr/schemas` folder.

Note: The new technology file in the XML syntax (`.tcfx`) also supports Generic layer information and uses the same read/write engine as used by other Constraint Manager files.

Performance Improvement

The front-end Constraint Manager database files are now composite files. For example, `<design>.dcf, pstcmdb.dat`, and `pstcmbc.dat`. This change has improved performance and data integrity.

You can open pre-17.2 database files in 17.2. On saving the design for the first time, the database files will be overwritten with the new database files.

Constraint Values Saved as Round Number

The constraint values will be rounded off to the precision limit. For example, any constraint value equal to 5.03 will be saved as 5.00. Similarly, any constraint value equal to 3.99 will be saved as 4.00.

Physical CSet Precedences Over Electrical CSet for Differential Constraints

Some differential constraints can be captured in both the Electrical and Physical domains in their respective Constraint Sets and Net Classes.

The following list of differential constraints can have different constraint values in the Physical and Electrical domains:

- DIFFP_PRIMARY_GAP
- DIFFP_COUPLED_PLUS
- DIFFP_COUPLED_MINUS
- DIFFP_MIN_SPACE
- MIN_LINE_WIDTH
- DIFFP_NECK_GAP
- MIN_NECK_WIDTH

In release 17.2, the value of the above mentioned differential constraints are honored from:

- Physical domain: If the object is not part of a differential pair.
- Electrical domain: If the object is part of a differential pair.

Important

To match pre-17.2 (or 16.x) constraints in a design, it is recommended that you assign the Electrical CSet values to Physical CSets for these differential constraints.

Virtuoso SiP Architect

Virtuoso® SiP Architect includes the following new enhancements and changes in 17.2-2016 release.

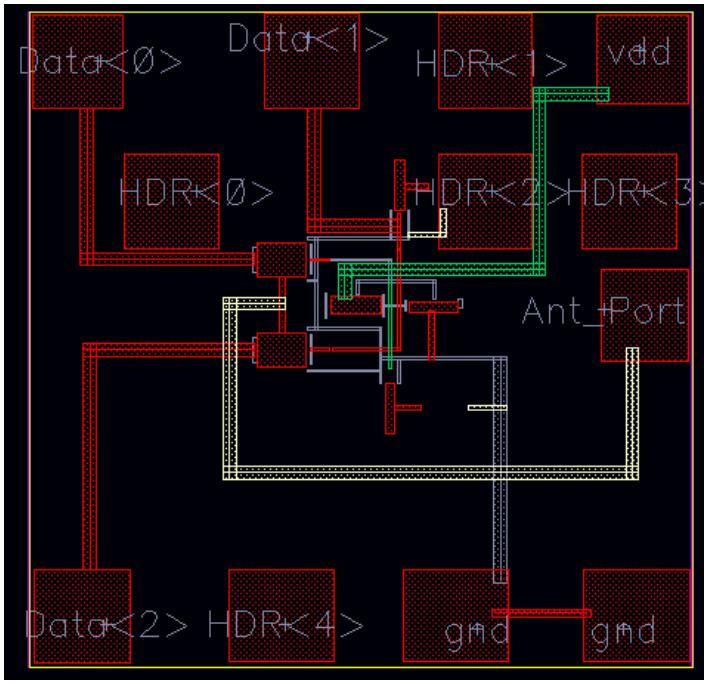
Vectored Symbol in Schematic

Virtuoso SiP Architect is enhanced to support symbols with vectored pins. For this following enhancements have been made:

Die Export Enhancement: Vector Pin Support

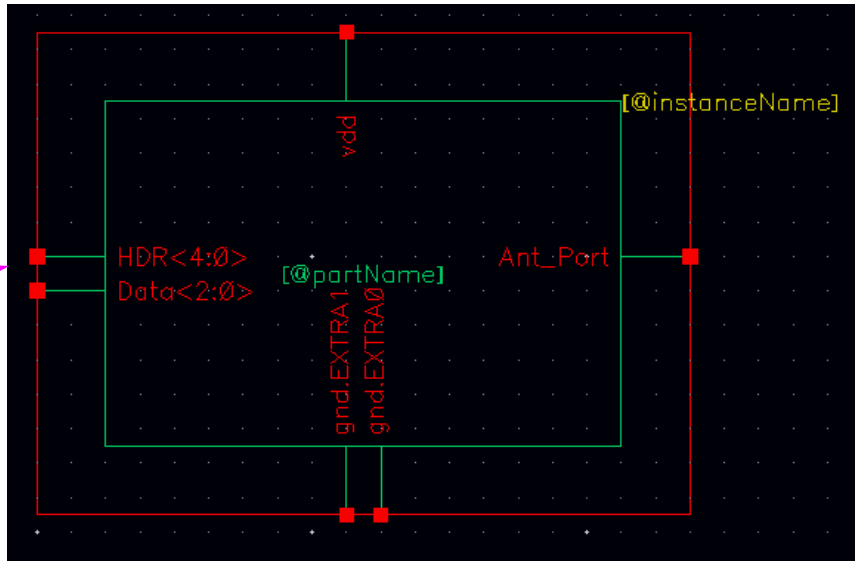
Virtuoso SiP Architect is enhanced to provide support for generating vectored symbols using Die Export. This makes it easier to handle DIEs with large pin-count, in Virtuoso Schematic Editor.

If the die layout in Virtuoso Layout Editor has pin labels with angular brackets, on Die export, these pins are represented as vector pins on the generated symbol.



Die Layout with pin labels with angular brackets

`Data<0>`, `Data<1>`, `HRD<4>` and so on



Package symbol generated after Die Export has vector pins

Caution

Virtuoso SiP Architect supports vectors naming format, `name<LSB:MSB>` ***or*** `name<MSB:LSB>`***. All other vector naming formats supported by Virtuoso Schematic Editor, such as*** `name<5,2>` ***or*** `name<3,2,1,0>`***, are not supported in Virtuoso SiP Architect.***

Model Assignment to Nets Connected to Vector Pins

Virtuoso SiP Architect also provides the ability to import and assign models to vector nets connected to the vectored pins.

When you assign a model to a vector signal, the vector signal on the schematic is replaced by a hierarchical symbol containing model information, in a way that original connectivity of the schematic is maintained.

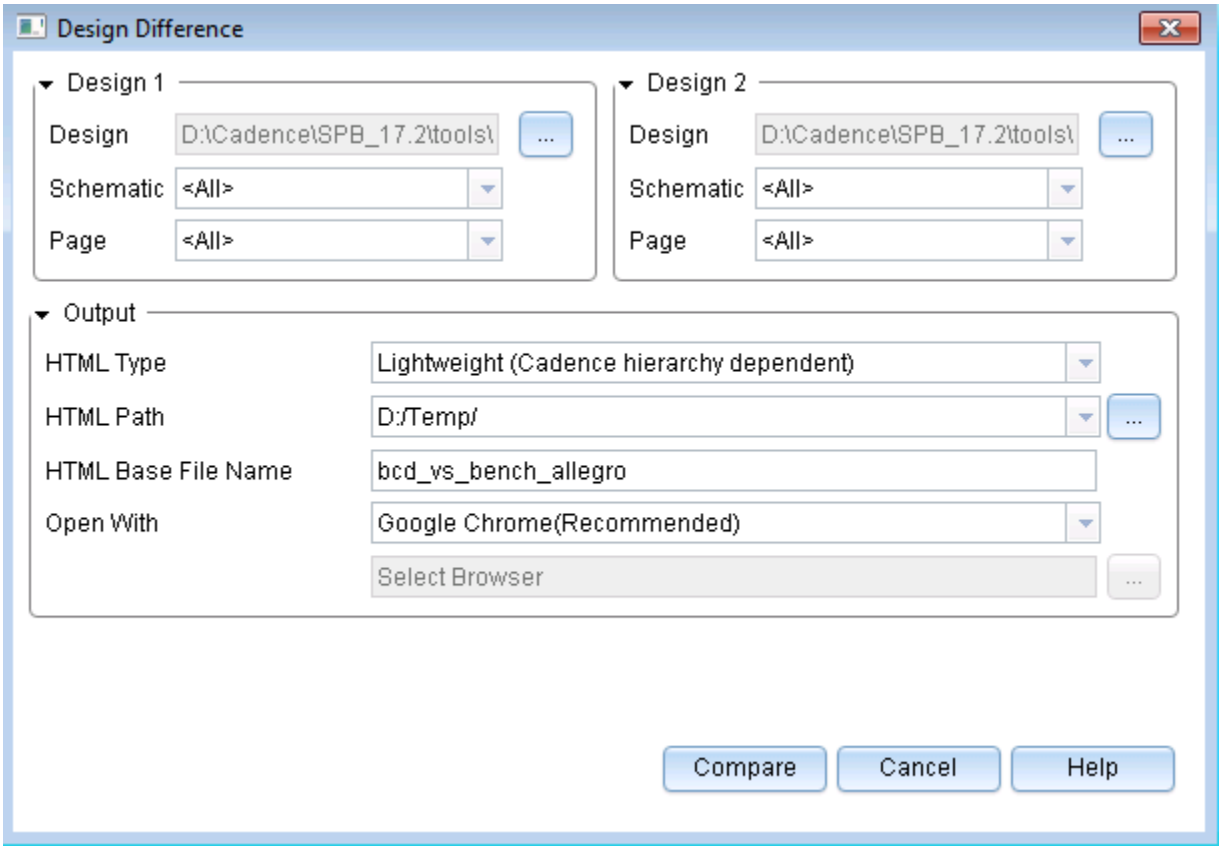
For details, see the section on *Assigning Models* in *Virtuoso SiP Architect User Guide*.

OrCAD Capture

The following sections describing the new features in the 17.2-2016 release of OrCAD® Capture.

Design Difference Viewer

Using Capture, you can now view logical and graphical differences between two designs, two schematics folders, or two schematic pages. To compare the designs or schematics, select *Compare Designs* from the *Tools* menu in Capture.



When you click the *Compare* button on the Design Difference dialog box, a Design Difference Summary window appears. The summary window displays logical and all differences (including logical and graphical differences), between the designs, schematics, or pages being compared.

Logical differences comprise the following:

- Components
- Pin Net Connectivity
- FlatNet

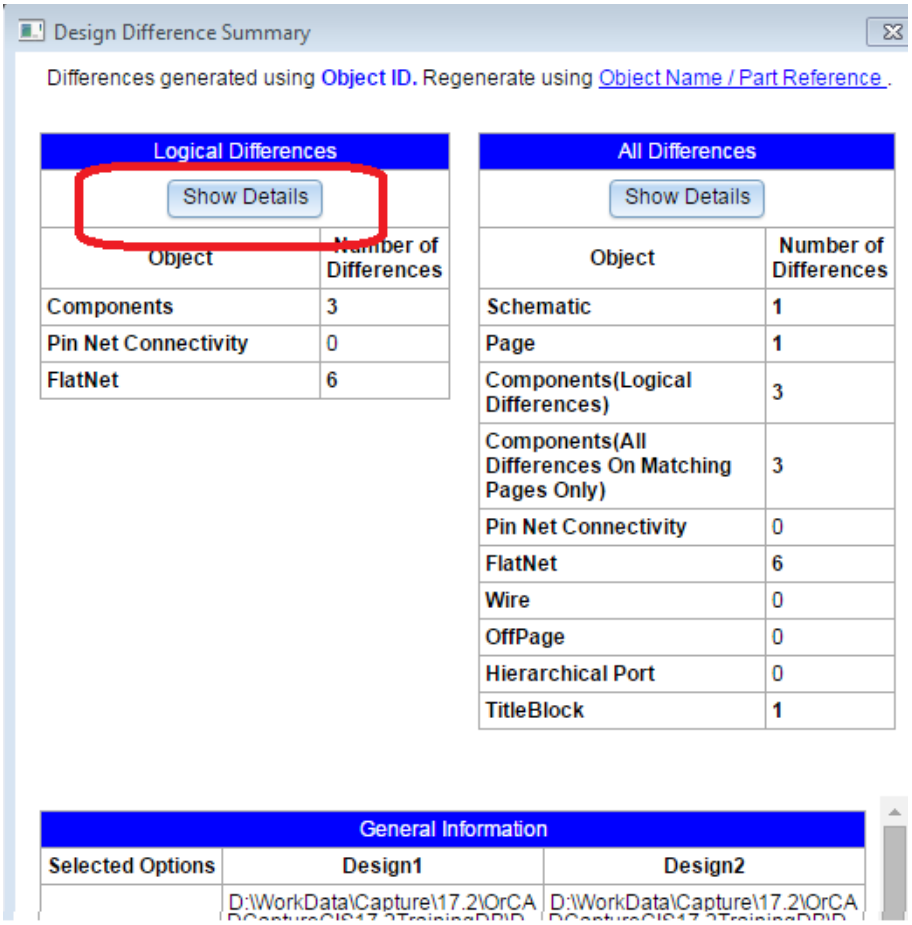
At design level, the All differences table displays the following:

- Schematic
- Page
- Components (Logical Differences)
- Components (All Differences on Matching Pages Only)
- Pin Net Connectivity
- FlatNet
- Wire
- OffPage
- Hierarchical PortTitleBlock

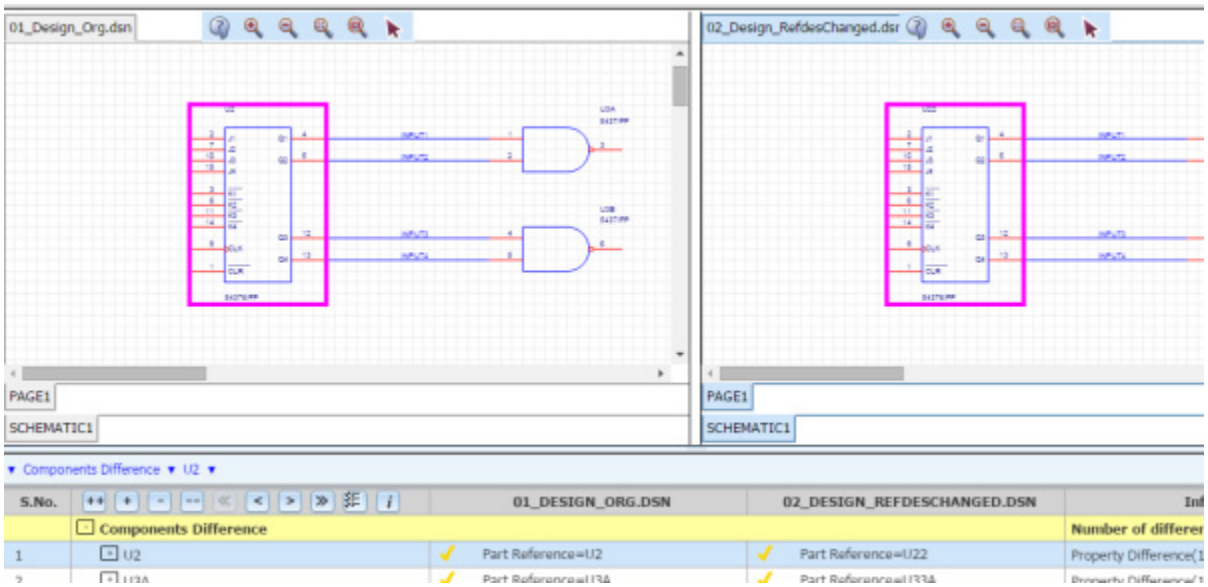
You can generate either a *lightweight HTML* or a *portable HTML* to view the differences. The lightweight HTML requires the Cadence hierarchy on the machine. The portable HTML, which requires more space on the disk than the lightweight HTML, does not require the Cadence hierarchy and can be launched from any machine.

Note: Google Chrome is the recommended browser to view the differences using the Design Difference feature.

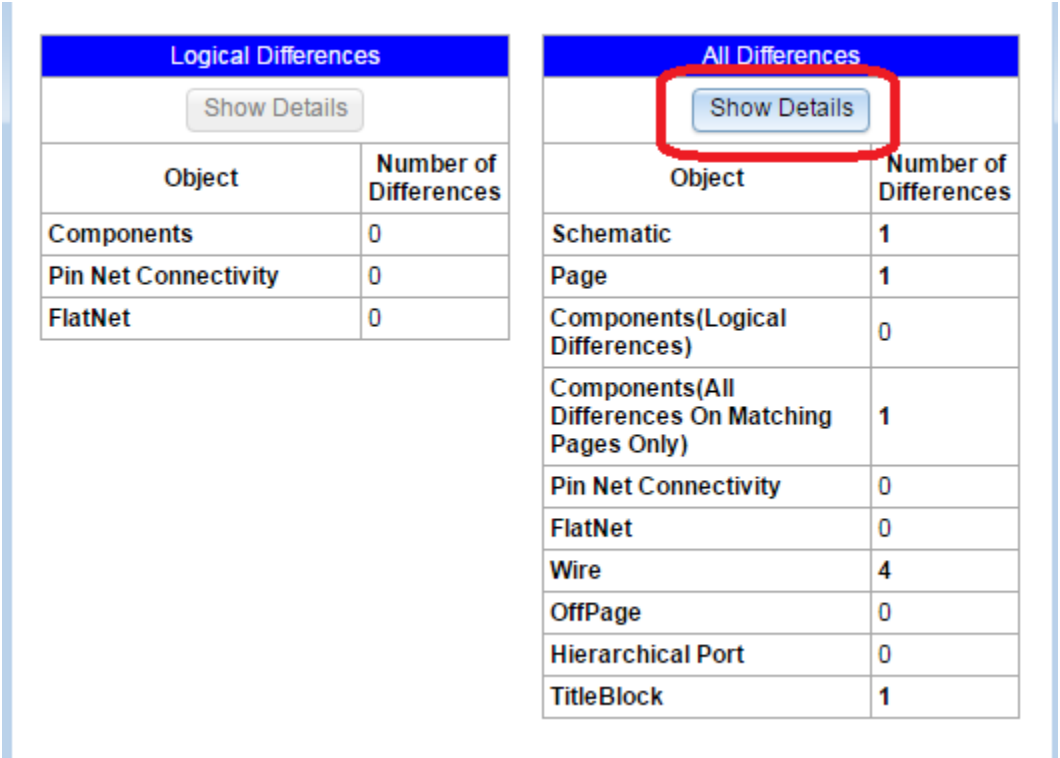
To view the details of logical differences, click the *Show Details* button in the Logical Differences table of the Design Differences Summary window as illustrated in the following image:



An example of logical differences displayed in the HTML browser is illustrated in the following image:



To view the details of all the differences, click the *Show Details* button in the All Differences table of the Design Differences Summary window:



Logical Differences

Show Details

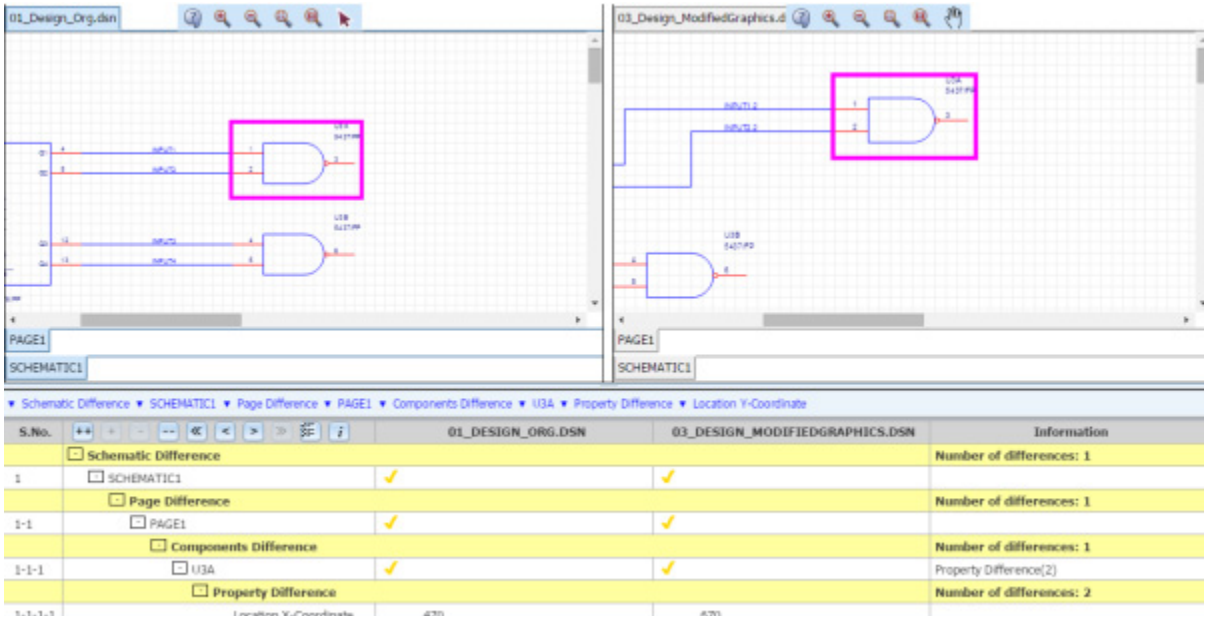
Object	Number of Differences
Components	0
Pin Net Connectivity	0
FlatNet	0

All Differences

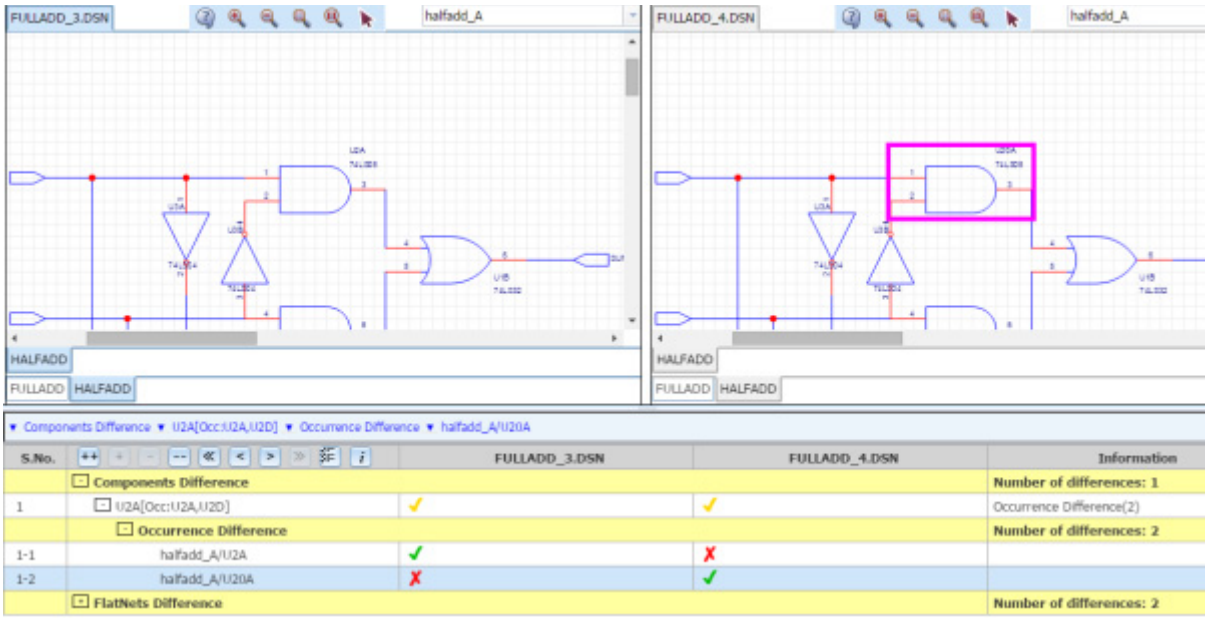
Show Details

Object	Number of Differences
Schematic	1
Page	1
Components(Logical Differences)	0
Components(All Differences On Matching Pages Only)	1
Pin Net Connectivity	0
FlatNet	0
Wire	4
OffPage	0
Hierarchical Port	0
TitleBlock	1

An example of all the differences (including logical and graphical) displayed in the HTML browser is illustrated in the following image

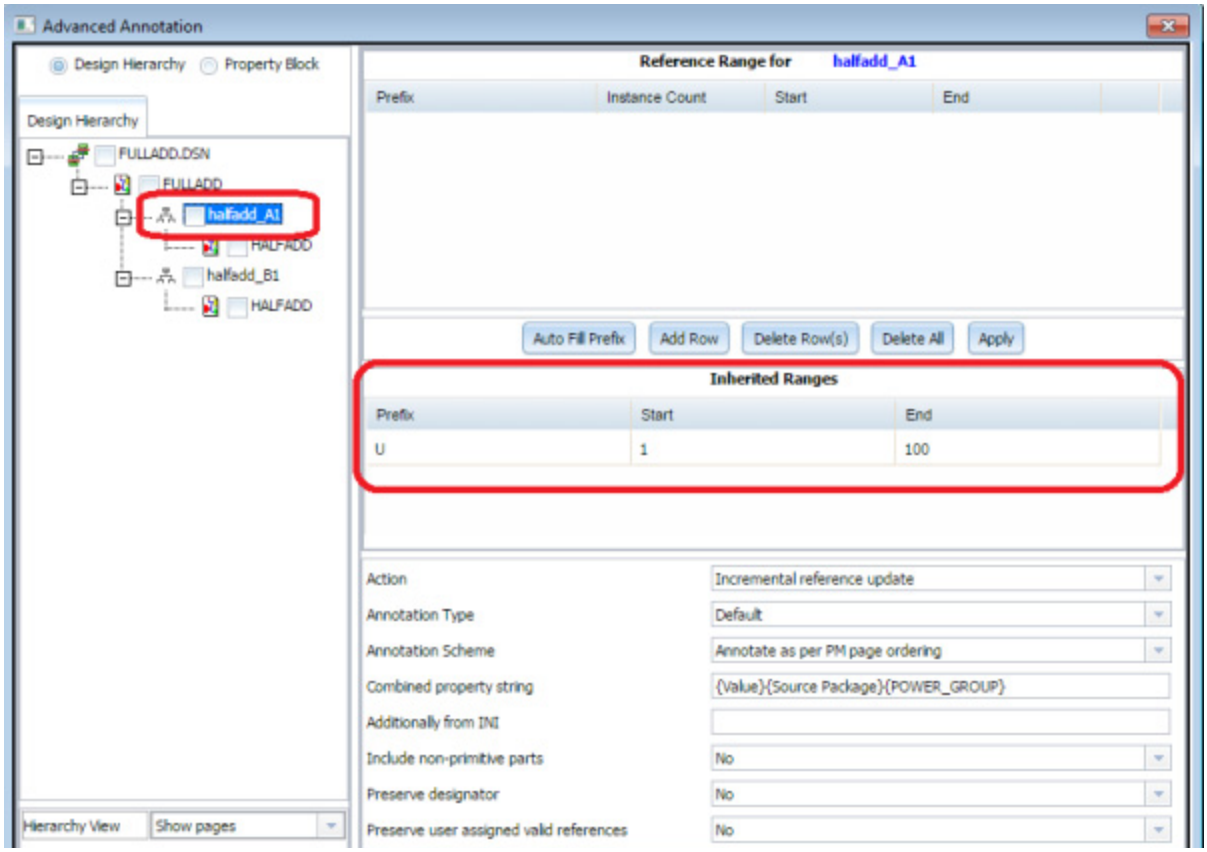


An example of logical differences displayed for different occurrences in the HTML browser is illustrated in the following image:



Advanced Annotation

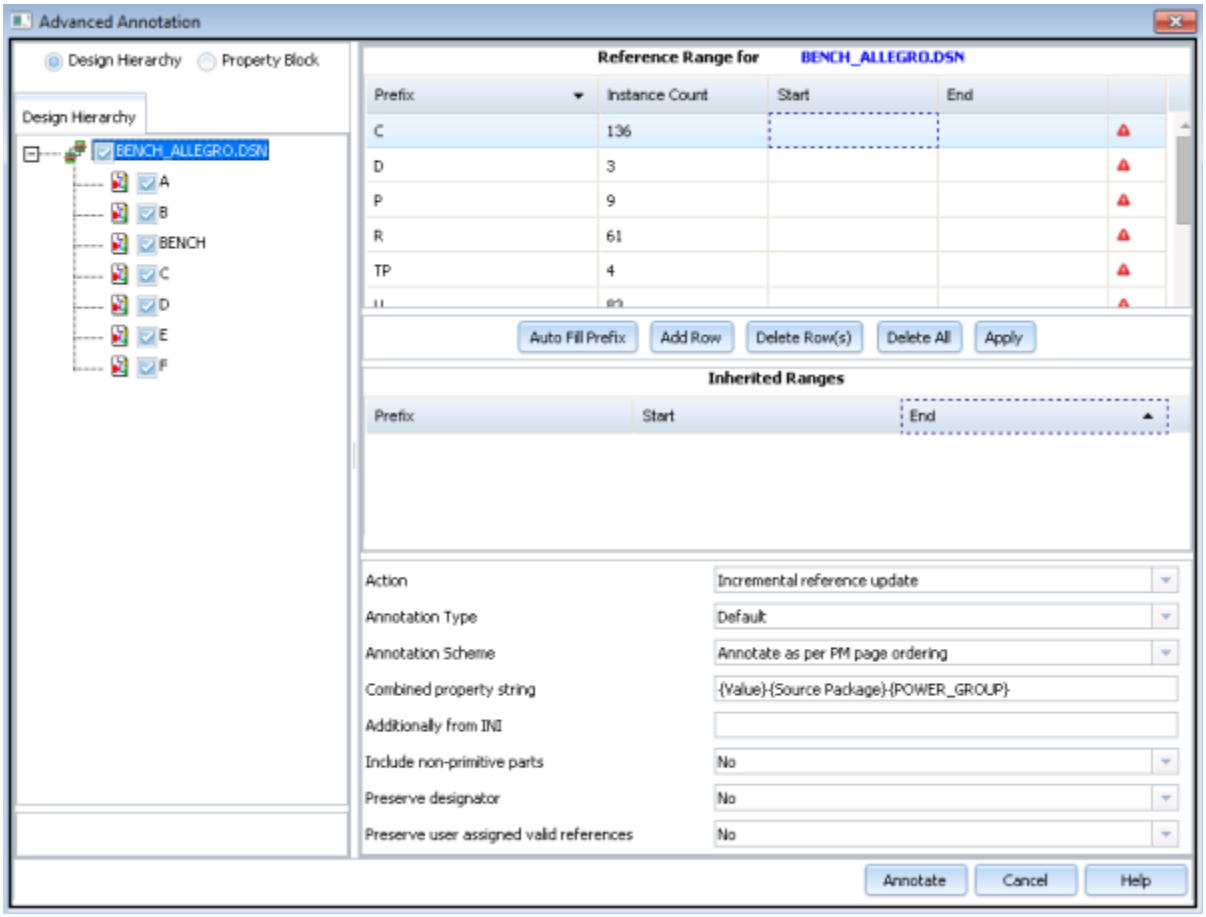
Advanced Annotation is the next level of the Annotation feature in Capture. With Advanced Annotation, you can annotate multiple schematic pages at a time. The following image illustrates annotation on different schematic pages. For example, schematic *page A* can have different reference range than schematic *page B*.



To access Advanced Annotation, select *Tools – Annotate – Advanced Annotation*.

Design Level and Schematic Page Level

You can also specify a reference range at the design-level (or global level) instead of schematic page level (or local level), but if the reference range is specified at the schematic page level the design-level reference range is not honored. If you have not specified any reference range at the lower schematic level, the reference ranges specified at the design-level for one or more prefixes are always honored.



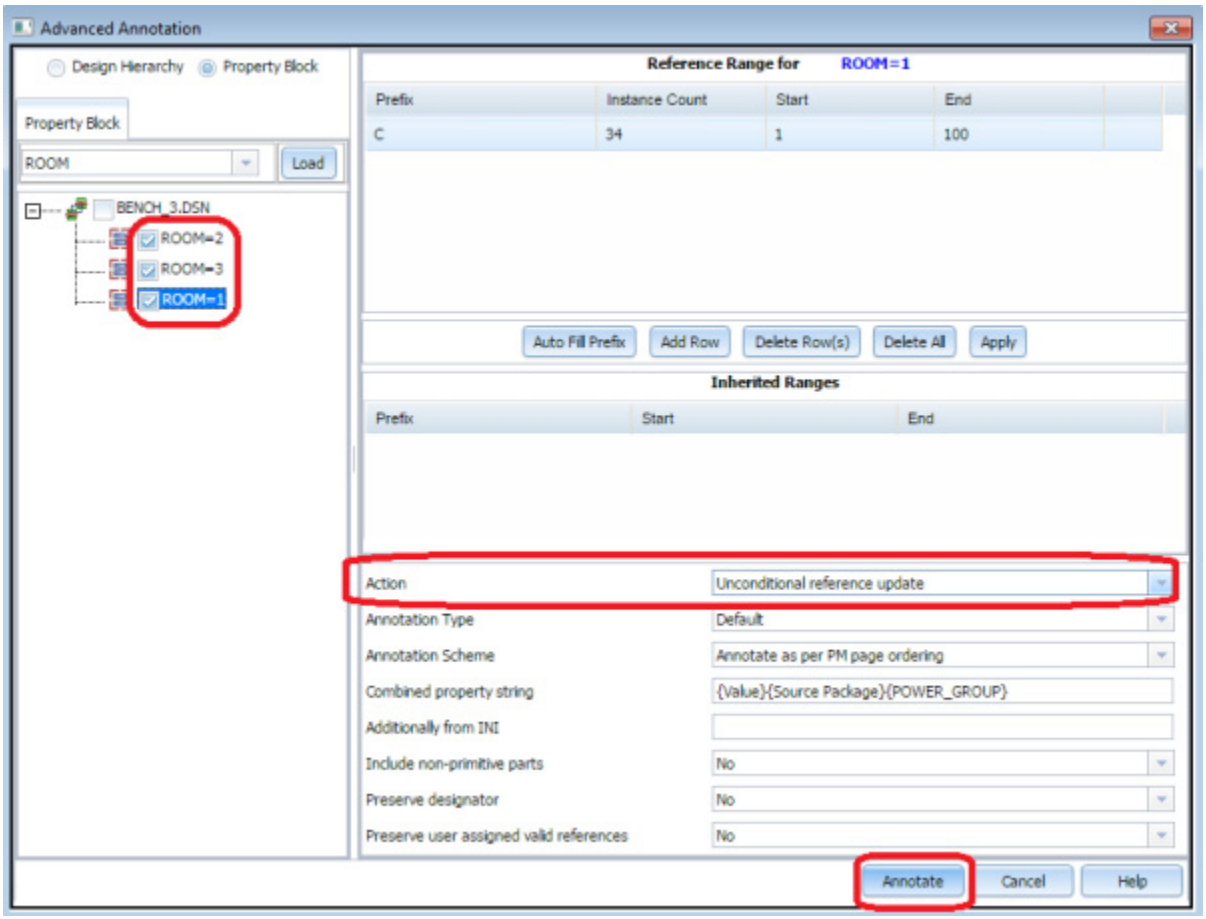
In the Advanced Annotation dialog box, you can either choose the Auto Fill Prefix option or add prefixes manually. If the *Auto Fill Prefix button* is clicked, the prefixes are autofilled under the Prefix column with the instance count automatically specified under Instance Count.

Note: After you have specified the annotation reference range at any level, either at the design-level or at the schematic-page level, click the *Apply* button to save the changes. Changes are not saved unless you click the *Apply* button.

Property Block Level

The Advanced Annotation feature allows you to specify reference ranges for different parts according to the property in a design. In the following screenshot, the *ROOM = 3* property

assignment is selected and all the prefixes with the selected property assignment are displayed in the dialog box. You can specify the reference range for annotation.



Use the *Auto Fill Prefix* button to autofill prefixes that have a common property. For more information, see *OrCAD Capture User Guide*.

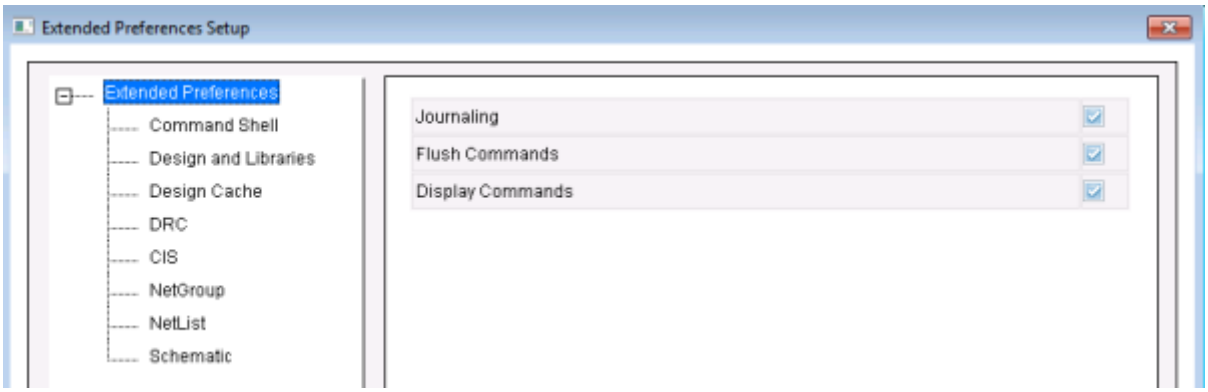
Note: After specifying the annotation reference range for the selected property block, click the *Apply* button to save the changes. Changes are not saved unless you click the *Apply* button.

Extended Preferences Setup

The Extended Preferences Setup window allows you to modify additional application settings in OrCAD Capture such as:

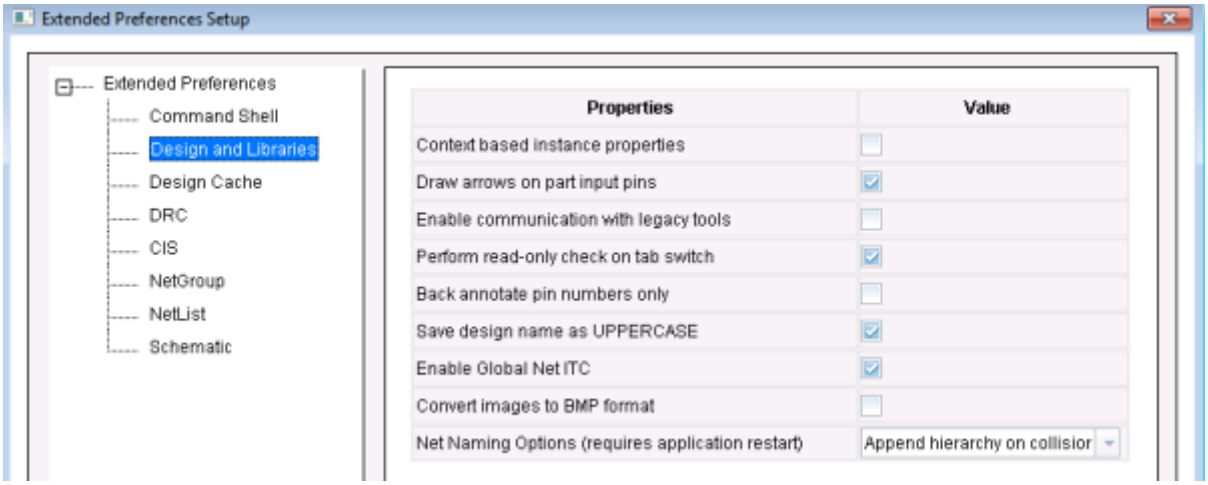
- Command Shell

Using the command shell, you can control journaling, flushing, and display commands.



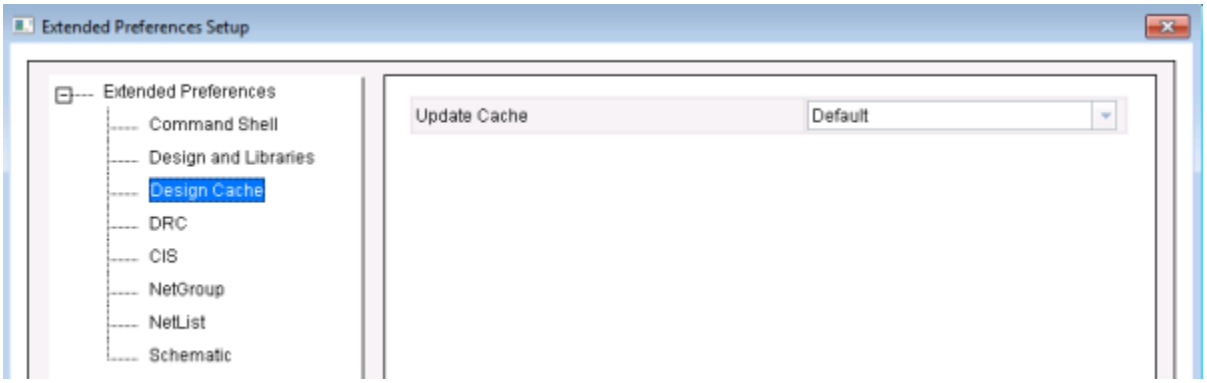
- Design and Libraries

  This option allows you to configure preferences related to designs and libraries, such as drawing arrows on part input pins, saving the design name in uppercase, and so on.



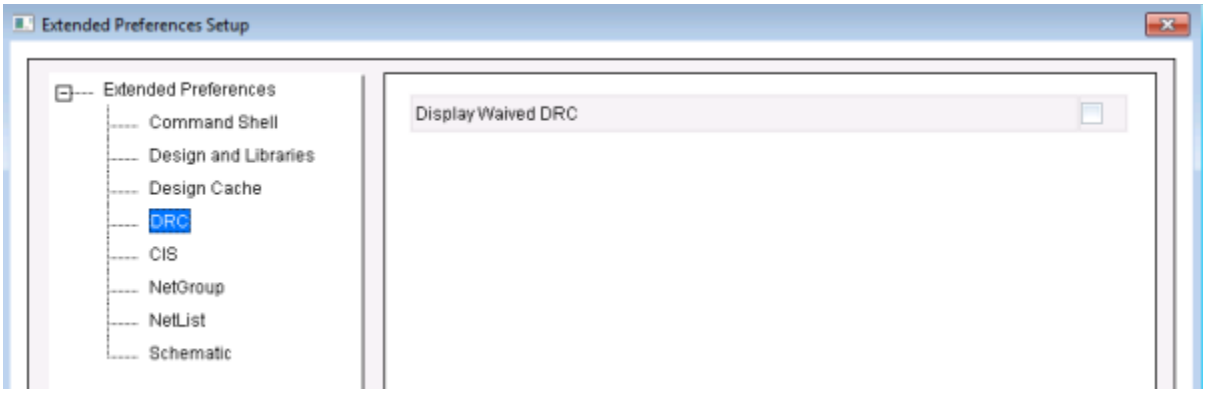
- Design Cache

  This option provides you design cache-related preferences, such as Update Cache.



- Design Rule Check (DRC)

  This option can be used to specify whether you want waived DRCs to be displayed in your design.

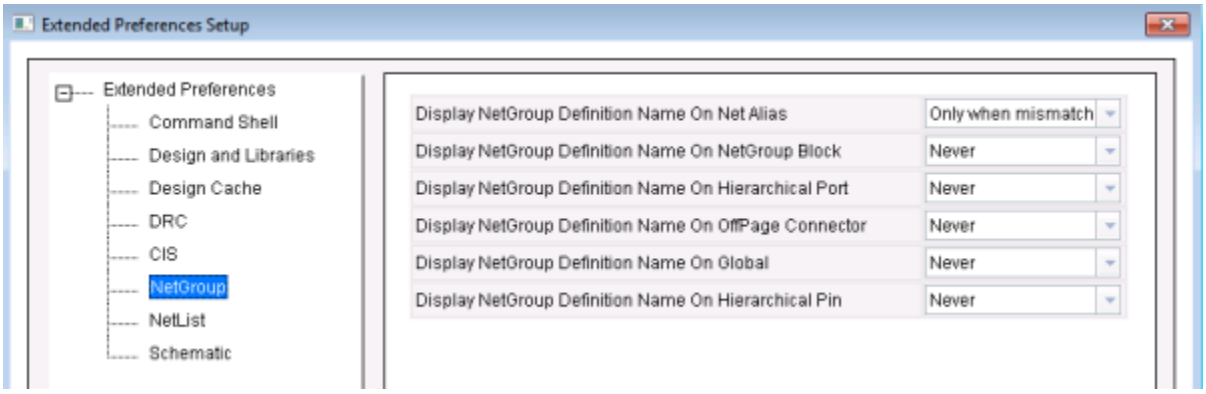


- CIS

  This option allows you to configure preferences related to CIS, such as Query All Configured Tables, and Disable Regional Settings.

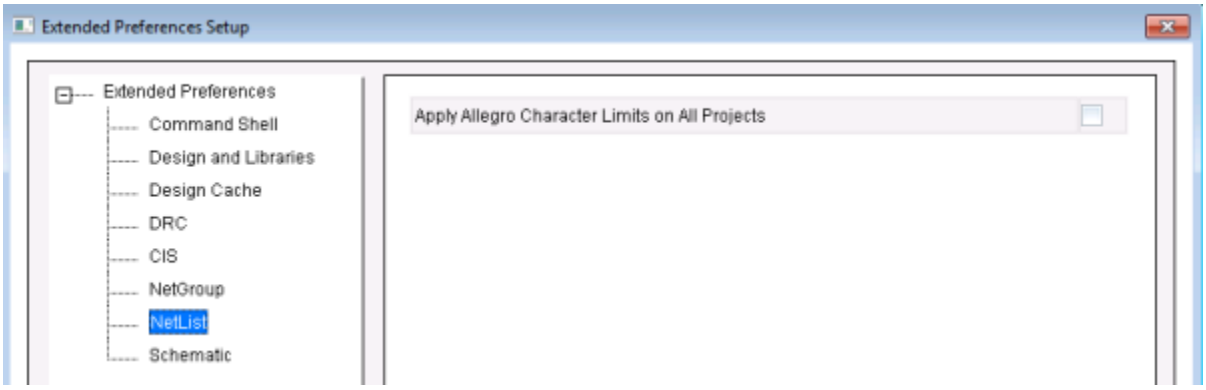
- NetGroup

  This option allows you to configure preferences related to netgroups, such as Displaying NetGroup Definition Name on Net Alias, Displaying NetGroup Definition Name on NetGroup Block, and so on.



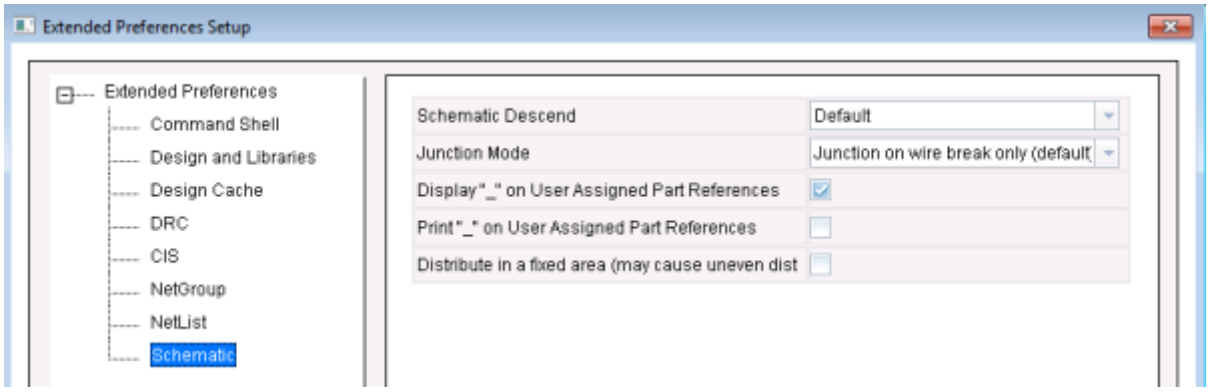
- NetList

  With this option, you can configure preferences related to netlisting, such as Applying Allegro Character Limits on All Projects.



- Schematic

Using this option, you can configure preferences related to schematics, such as Print "_" on User Assigned Part Preferences, Distribute in a fixed area, and so on.

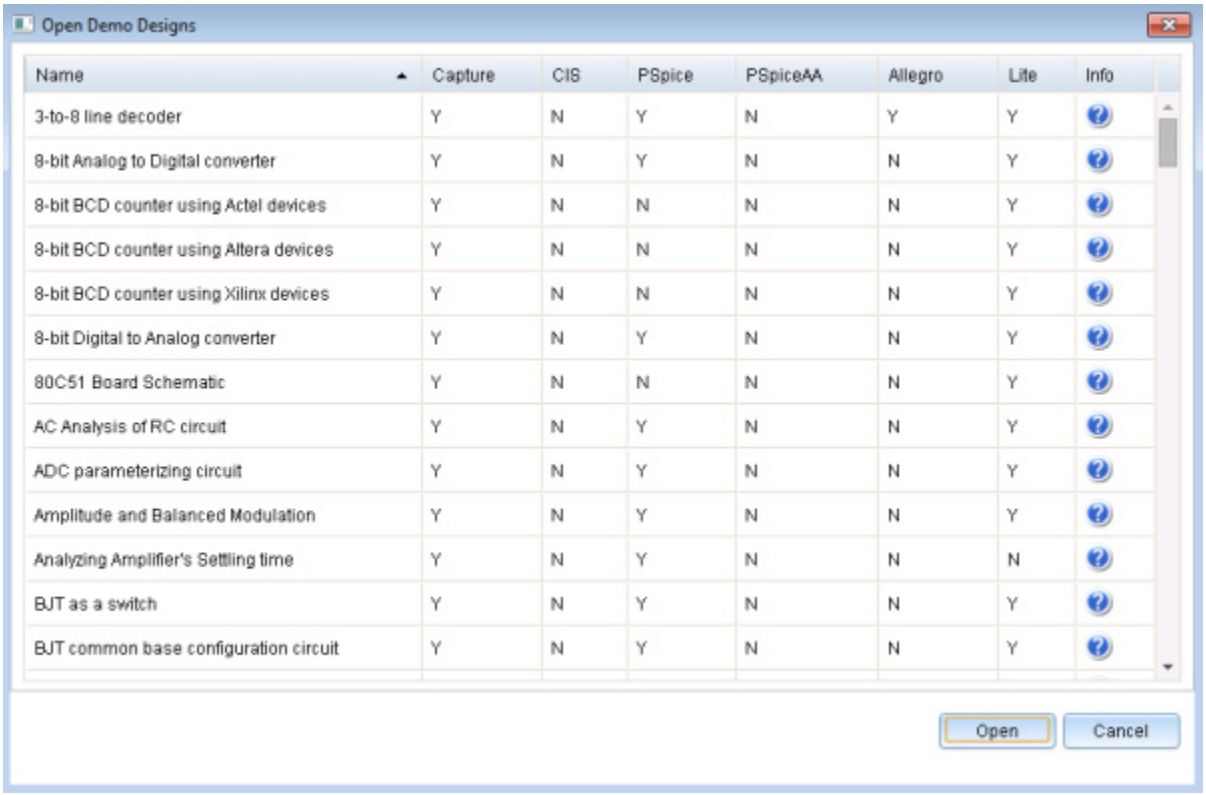


To access Extended Preferences Setup dialog box, select *Options – Preferences – More Preferences*.

Demo Design Browser

The Cadence installed hierarchy contains more than 150 demo designs to help users understand Capture, Capture CIS, and the Capture - PSpice flow. Until now, these designs were available at different locations. From 17.2-2016, all these demo designs are accessible

from *File – Open – Demo Designs*. These designs are collated from Learning PSpice, sample folders, and other locations in the installed hierarchy.



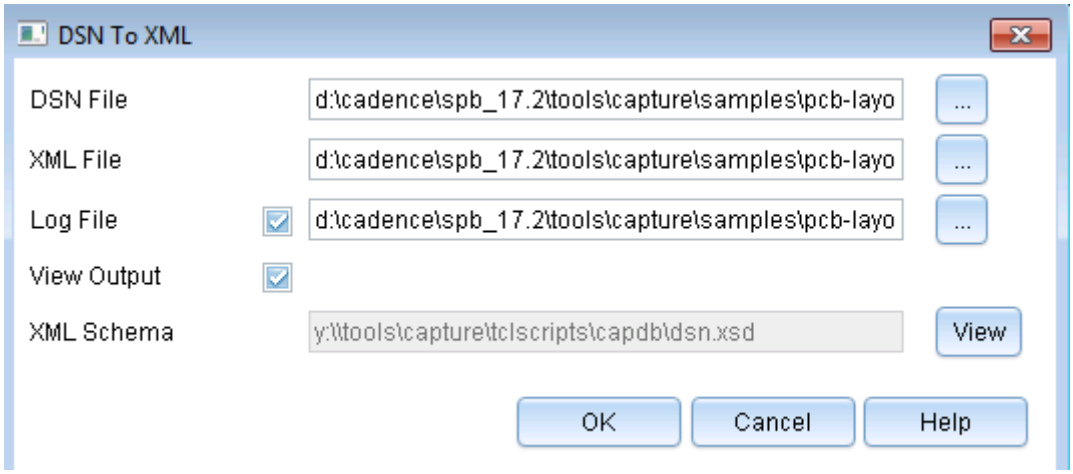
XML Export

Capture Design To XML

Starting with the 17.2-2016 release, you can export Capture designs to XML format using the DSN To XML dialog box. The DSN To XML dialog box is accessed from the *File – Export – Design XML* menu.

To convert the Capture design (.dsn) file to an XML file, Capture uses an XML schema that is located at the following path:
`<installation>\tools\capture\tclscripts\capdb\dsn.xd`.

The following image shows the DSN To XML dialog box:



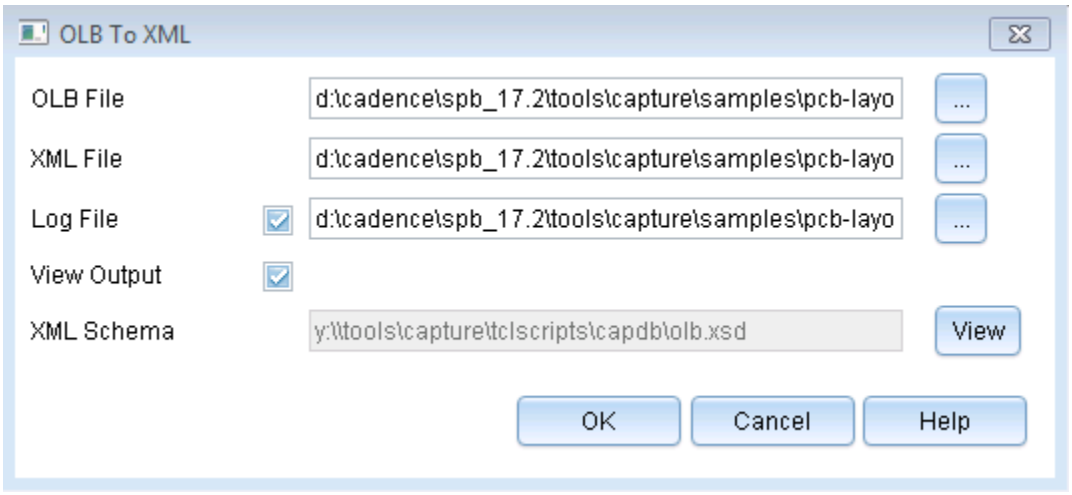
Part of the XML file generated after converting a Capture design to XML format is displayed as an example:

Capture Library to XML

Starting with the 17.2-2016 release, you can convert a Capture library (.olb) to an XML file using the OLB To XML dialog box. The OLB To XML dialog box is accessible from *File – Export – Library XML*.

To convert a Capture library (.olb) file to an XML file, Capture uses an XML schema that is located at the following path:
`<installation>\tools\capture\tclscripts\capdb\olb.xd`.

The following image shows the OLB To XML dialog box:



Part of the XML file generated after converting a Capture library to XML format is displayed in the following image:

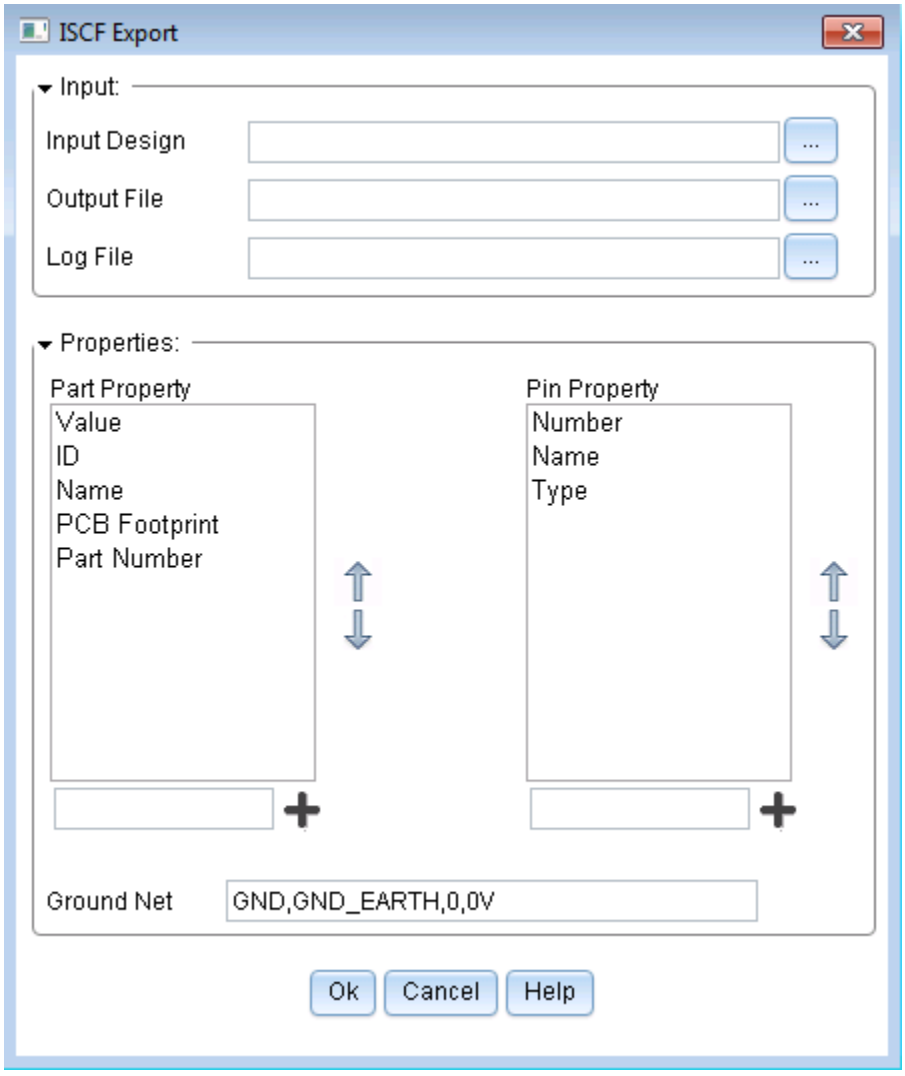
ISCF Export

You can export part properties, pin properties, and ground nets of a Capture design to Intel Schematic Export Format (ISCF) using the ISCF Export dialog box.

If you have any design opened in Capture, the design is taken as the default input source file for the Input Design field. If no active design is available, select the design whose part properties, pin properties, and ground nets you want to export to ISCF.

When launched for the first time the ISCF Export dialog box displays some default part properties, pin properties, and ground nets.

- To add other part properties, pin properties, or ground nets, specify the property name in the text field and click the add button (+).
- To delete a property from the window, select the property and press *Delete*.



- To access the ISCF Export dialog box, choose the *File – Export – ISCF Export* menu.

Whenever the ISCF Export dialog box is launched, the list of properties in the dialog box is updated in the preferences section of the Capture.ini file.

```
ISCFPartProps=Value,ID,Name,PCB Footprint,Part Number
ISCFPinProps=Number,Name,Type
ISCFGroundNames=GND,GND_EARTH,0,0V
```

PDF Export

Starting with 17.2-2016, you can export a Capture design as a PDF file provided you have the required postscript to pdf converter installed, such as ghostscript 32-bit, ghostscript 64-bit, or Adobe Acrobat Distiller. To access PDF Export dialog box, select *File – Export – PDF*.

Using the Export PDF dialog box, you can generate two types of PDFs:

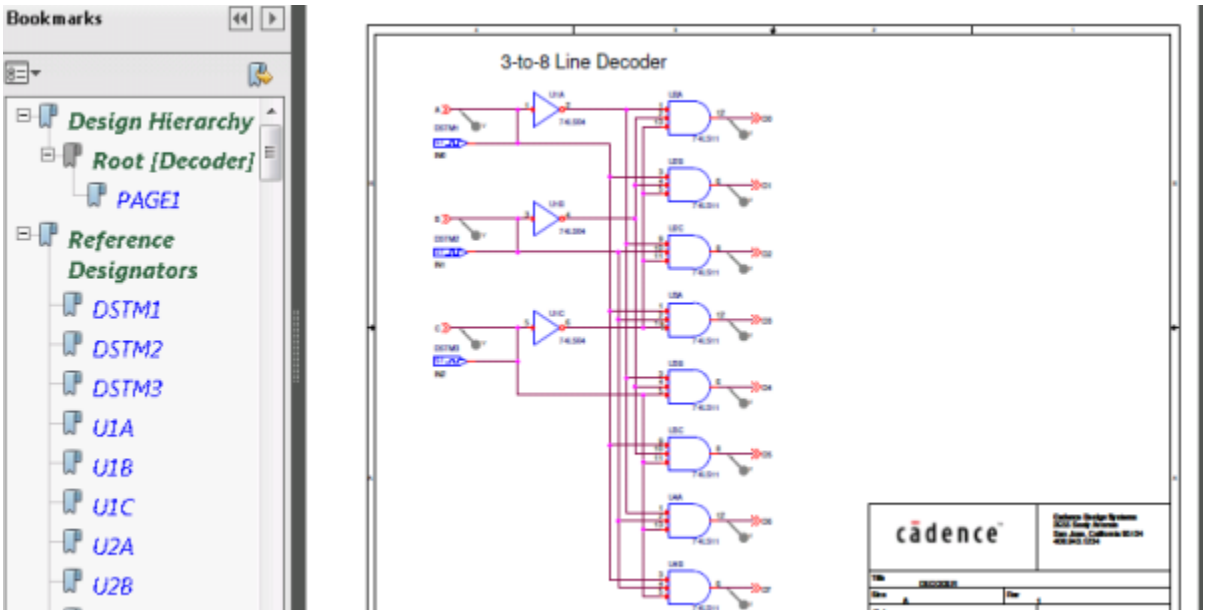
- Capture Design PDF
- Capture Design Object Properties PDF

Capture Design PDF

The Capture Design PDF displays the following properties:

- Displays Design Hierarchy Tree
- Displays Reference Designators List
- Displays Nets and Connected Component Pins
- Descends Hierarchical Blocks
- Displays Properties on Clicking an Object

- Displays Navigation to Offpage Connectors



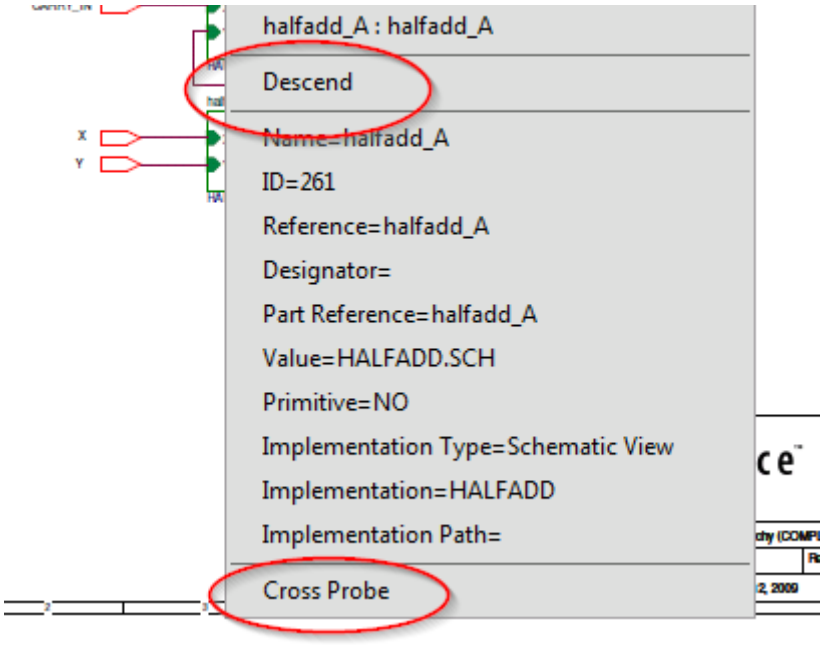
Capture Design Object Properties PDF

In addition to the properties mentioned for the Capture Design PDF, the Capture Design Object Properties PDF contains the following property:

- Bi-directional cross-probing of Capture Design Object Properties PDF with the object

Object	Property Name	F
3-to-8 Line Decoder	Name	I(
	Bounding Box Left	1
	Bounding Box Right	3
	Bounding Box Top	2
	Bounding Box Bottom	4
	Text	3
	Text Location X-Coordinate	1
	Text Location Y-Coordinate	2
	Font	A

Object	Property Name	F
N00058 : N00058 (Wire ID = 58)	Name	N



Note: The Capture Design Object Properties PDF is created in the same folder as the Capture Design PDF. The name of the Object Properties PDF uses the following naming convention: `prop<DesignName>.pdf`.

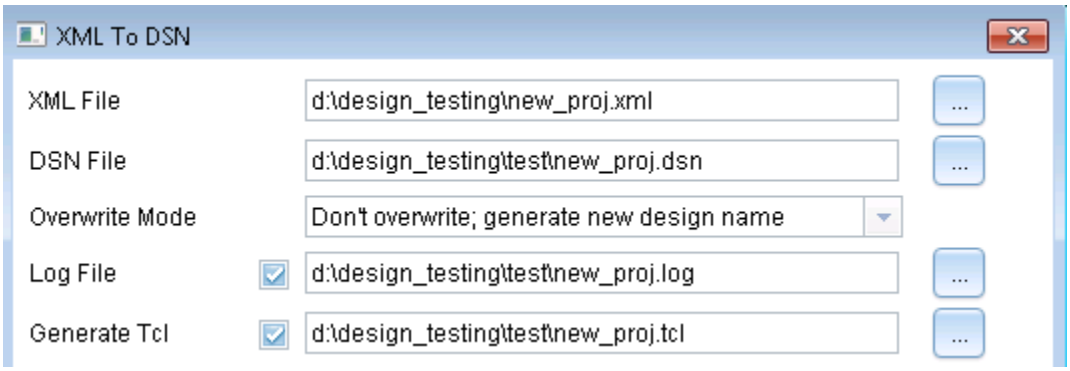
XML Import

XML to Capture Design

From the 17.2-2016 release, you can import an XML file as a Capture design using the XML To DSN dialog box. The XML To DSN dialog box is accessed from *File – Import – Design XML*.

To convert an XML file to a Capture design (.dsn) file, Capture uses XML schema that is located at the following path:
`<installation>\tools\capture\tclscripts\capdb\dsn.xd`.

Using the XML To DSN dialog box, you can generate a TCL file that can be used to generate a Capture design. To generate a Capture design from the TCL file generated using the XML To DSN dialog box, source the TCL file in the Capture command window.

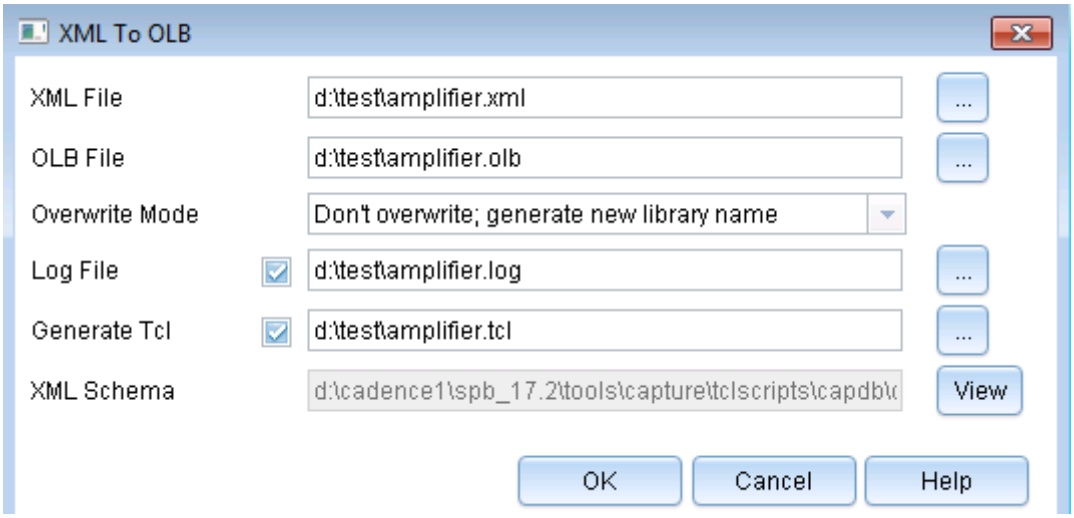


Capture Library to XML

From the 17.2-2016 release, you can import an XML file as a Capture library using the XML To OLB dialog box. The XML To OLB dialog box is accessed from *File – Import – Library XML*.

To convert Capture library (.olb) file to an XML file, Capture uses an XML schema that is located at the following path:
`<installation>\tools\capture\tclscripts\capdb\olb.xd`.

Using the XML To OLB dialog box, you can generate a TCL file that to generate a Capture library. To generate a Capture library from the TCL file generated using the XML To DSN dialog box, source the TCL file in the Capture command window.



New Models for Capture - PSpice flow

New models have been added in the 17.2-2016 release for the Capture - PSpice flow. The following model files are located at `<Installation directory>\tools\capture\library\pspice`:

- TNY274-80 model is added in the *swit_reg* library
- PC457 model is added in the *opto* library
- HCPL-M453 model is added in the o*pto* library
- PS8101 model is added in the o*pto* library
- GTO model is updated in the Breakout library

Miscellaneous Enhancements

Support for TCL 8.6

In the 17.2-2016 release, Capture supports TCL 8.6 64-bit.

Enhancement in Intersheet References

In the 17.2-2016 release, Capture allows you to add negative X offset in the Intersheet References window.

OrCAD Capture CIS

The following section describe the new features in the 17.2-2016 release of OrCAD® Capture CIS.

Crystal Report Enhancement

From the 17.2-2016 release, OrCAD Capture CIS requires the ODBC connection method to connect a Crystal report file (.rpt) to a database.

In the 17.2-2016 release, the default database required for Crystal report generation is SQLite. Following is the new ODBC connection string for the SQLite database:

```
DRIVER=SQLite3 ODBC Driver;Database=”SQLite DB file Name”;LongNames
= 0;Timeout = 1000; NoTXN = 0;SyncPragma=NORMAL;StepAPI=0;NoWCHAR=1;
```

For more information on generating Crystal reports, see *OrCAD CIS User Guide*.

Miscellaneous Enhancements

Support for TCL 8.6

In the 17.2-2016 release, Capture CIS supports TCL 8.6 64-bit.

Cadence PSpice

The following sections describe the new features in PSpice® 17.2-2016 release.

PSpice DMI Template Code Generator

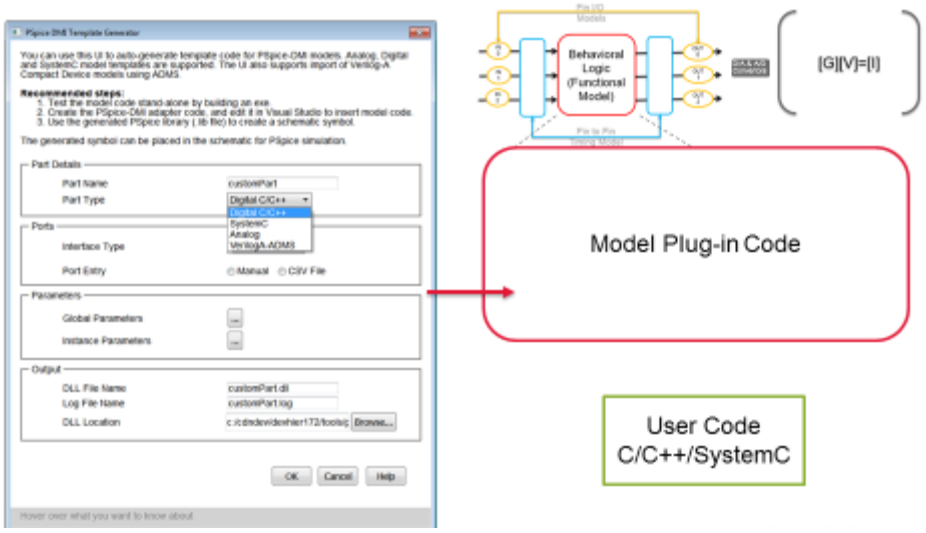
Release 17.2-2016 onwards, you can generate PSpice adaptor code using the DMI Template Code Generator dialog box available in PSpice Model Editor.

The PSpice adaptor code enables PSpice simulation using PSpice DMI Dynamic Link Library (DLL) files. After generating the adaptor code, you need to add the actual model code in the adaptor code for Analog, Digital C/C++, and SystemC models, and build the PSpice model DLL file using Microsoft Visual Studio Express 2013.

After the DLL file is built, use the generated Pspice Library (.lib) file to create a Capture part symbol.

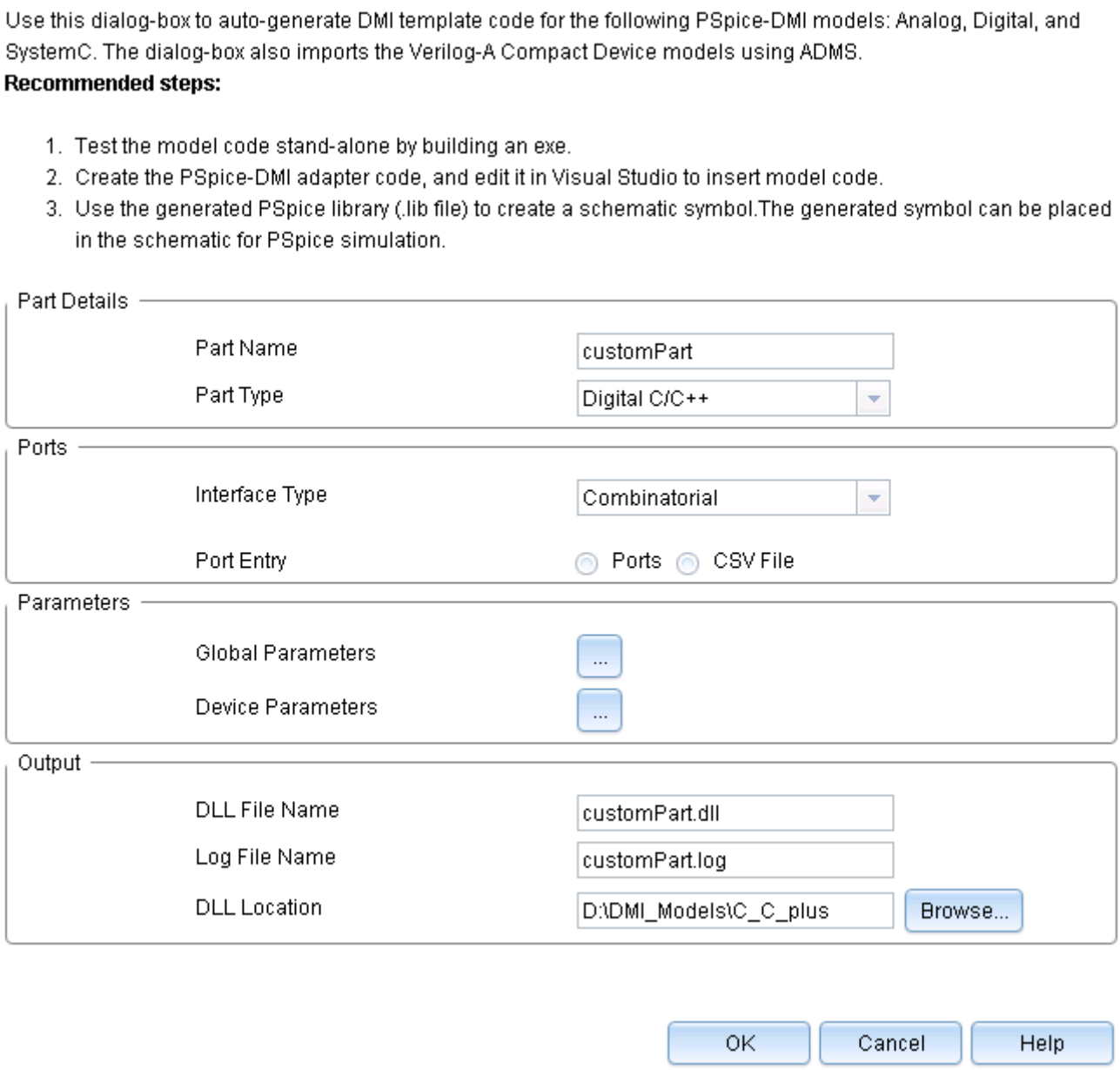
The PSpice DMI Template Code Generator feature is provided only with the *OrCAD PSpice Designer Plus* and *Allegro PSpice Simulator* licenses.

Note: Microsoft Visual Studio Community 2013 is a prerequisite to generate PSpice DMI DLL files using the DMI Template Code Generator dialog box. Therefore, it is highly recommended that you install Microsoft Visual Studio Community 2013 on your machine.



In the case of Verilog-A, the adaptor code contains the model logic from the Verilog-A file. As a result, the PSpice DMI Model DLL file is build automatically.

Note: The Verilog A-ADMS part name should match the Verilog-A file name.



The DMI Template Code Generator dialog box provides you various options to generate PSpice DMI models for the following part types:

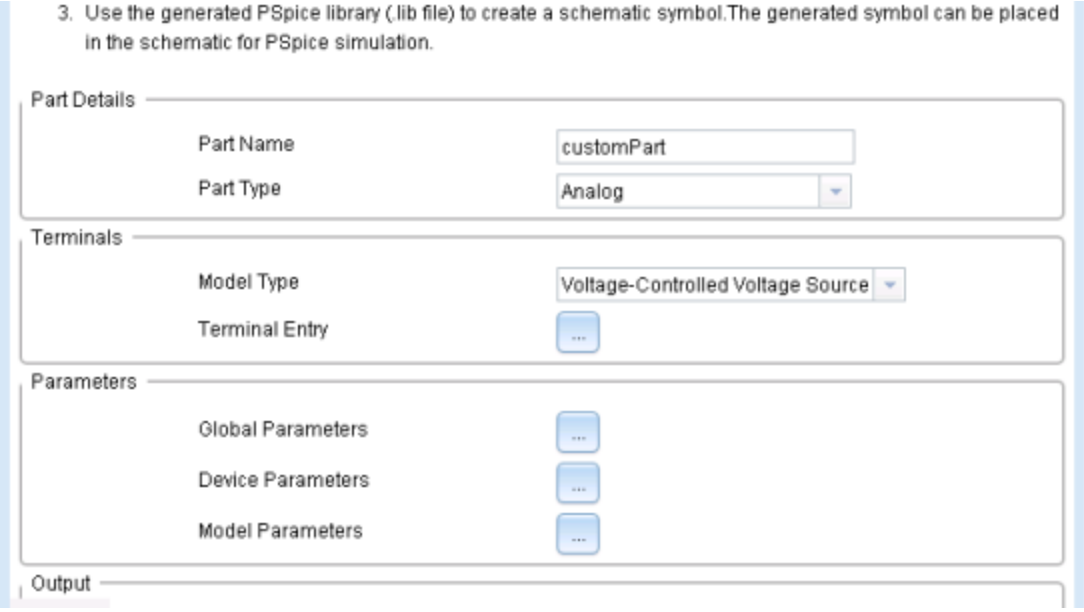
- Analog-based Parts
- Digital C/C++-based Parts
- SystemC-based Parts

- Verilog A-based Parts

Analog-based Parts

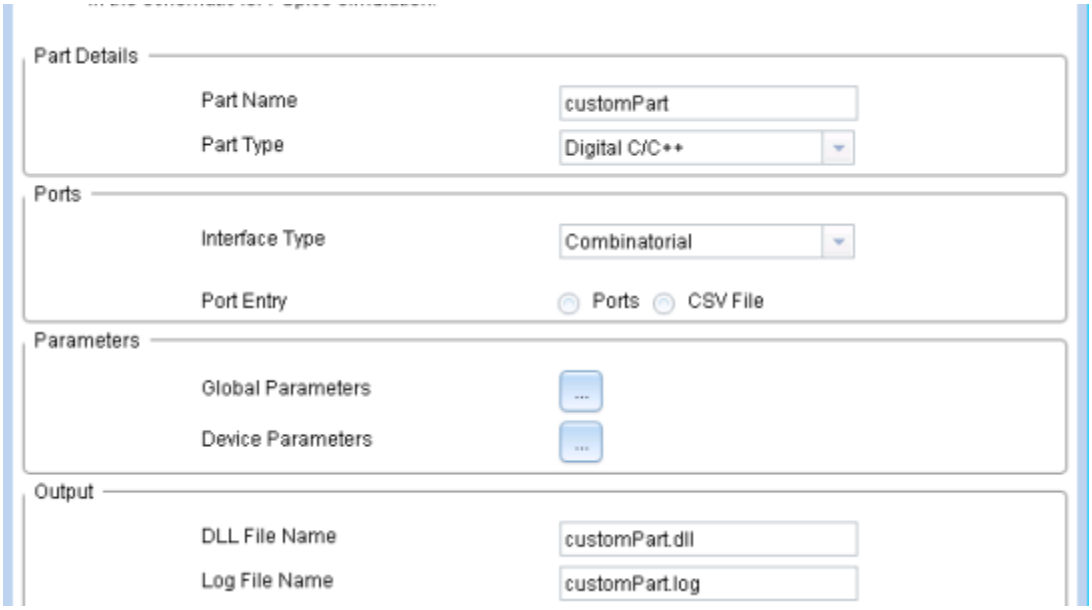
Analog Part Type lets you generate the following different PSpice DMI models:

- Generic device
- Voltage-Controlled Voltage Source
- Function-Dependent Voltage Source
- Voltage-Controlled Current Source
- Function-Dependent Current Source
- Generic Two-Node Device
- Generic Three-Node Device



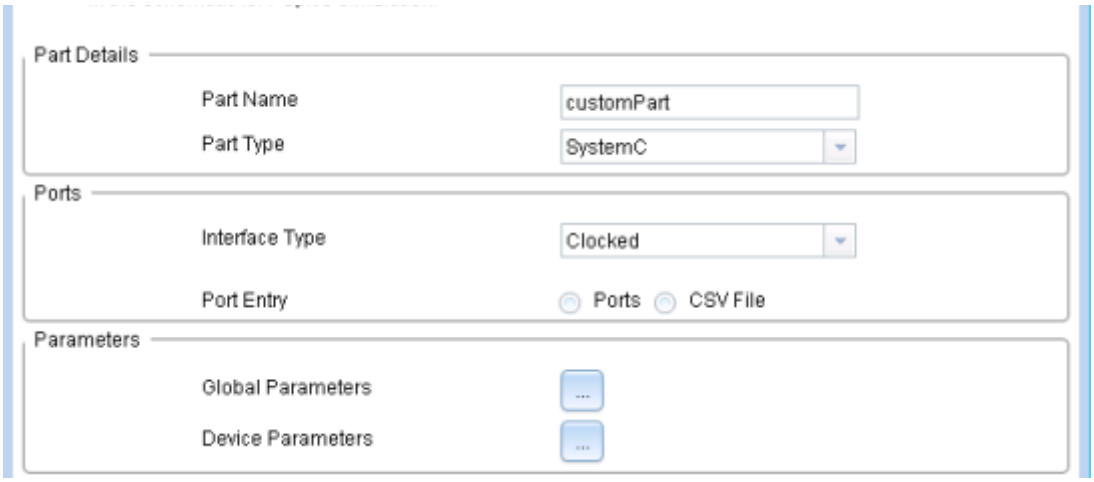
Digital C/C++-based Parts

The Digital C/C++ part type option allows you to generate PSpice DMI models with two interface type, such as Clocked Interface and Combinatorial.



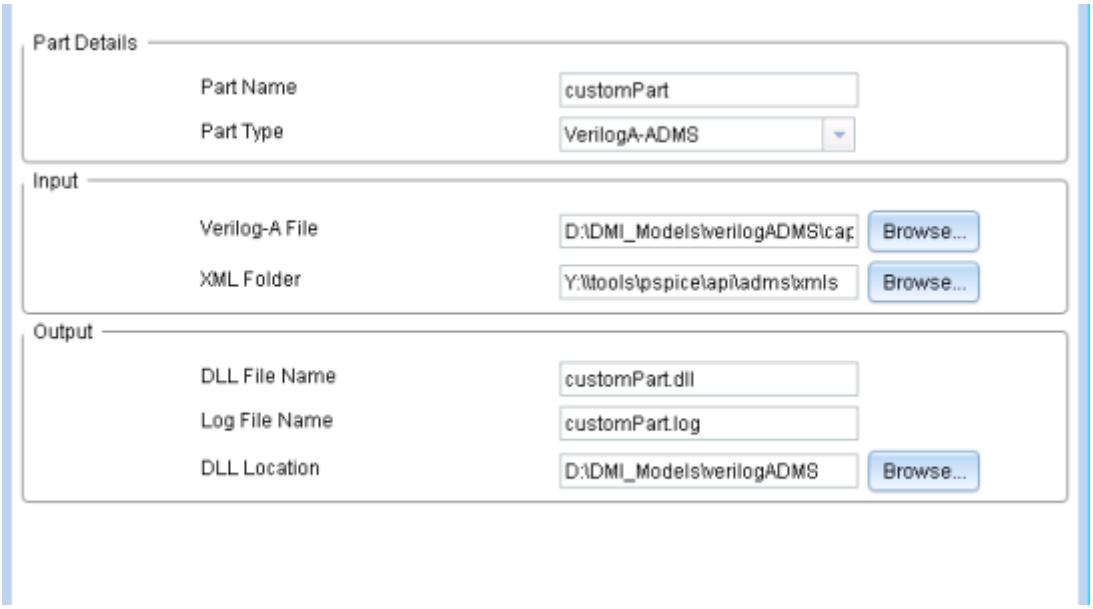
SystemC-based Parts

Using the SystemC Part Type option, you can generate PSpice DMI models based on SystemC. The generated SystemC-based PSpice DMI models have Clocked Interface.



Verilog A-based Parts

Using the DMI Template Code Generator dialog box, you can generate the PSpice DMI models using a verilog-A file. PSpice uses an open source software, ADMS, to convert the verilog-A code to a PSpice DMI DLL file.



Miscellaneous Enhancements

Support for TCL 8.6

In the 17.2-2016 release, PSpice supports TCL 8.6.

New Delay Functions for Behavioral Simulation Models

The delayt() and delayt1() functions simplify traditionally-used delay functions, such as TLINE and Laplace-based functions, and minimize the convergence issues in traditional functions. They also process faster computation on signals (voltage or current) compared to the traditional functions.

DelayT() Function

The general format of the DelayT() function is: `delayt(v(x),<delay time>, <maxdelay>)`

For the delayt() function, delay value and max delay parameters are required.

DelayT1() Function

The general format of the DelayT1() function is: `delayt1(v(x),<delay time>)`

For the delayt1 function, only the delay value parameter is required.

For more information, see the *Behavioral Simulations Functions* chapter in PSpice Reference Guide.

New Flag Option for .OPTIONS command

When the following flag option is selected, the topology checks in a Capture Design are skipped:

```
.options SKIPTOPO = 1
```

You can either use a .INCLUDE file , or Place Text on Capture schematic page to enable the SKIPTOPO flag option.

Support for Negative Values in Hyteresis Voltage and Threshold voltage

Hysteresis voltage and threshold voltage now support negative values for behavioral simulation functions.