CADENCE Allegro and OrCAD (Including EDM) RELEASE 17.2-2016 README -- Windows Version

Installation Guide

You can find the *Cadence Allegro and OrCAD (Including ADW) Release 17.2-2016 Installation Guide for Windows, Version* (pcbInstall.pdf) in the Disk 1 folder of the Cadence® Product DVD.

Migration Information

Important migration information is contained in the *Migration Guide for Allegro Platform Products Release 17.2-2016*, which is available when you install this software or on Cadence Online Support (http://support.cadence.com).

NOTE: OrCAD® customers need to contact Cadence Channel Partners. Cadence Channel Partners are listed at: http://www.cadence.com/Alliances/channel_partner/pages/default.aspx.

System Requirements

Information about minimum and recommended system requirements can be found in the Documents folder of the Disk 1 folder in the *Allegro Platform System Requirements* document (pcbsystemreqs.pdf) or on Cadence Online Support (http://support.cadence.com).

NOTE: OrCAD customers need to contact Cadence Channel Partners. Cadence Channel Partners are listed at: http://www.cadence.com/Alliances/channel_partner/pages/default.aspx.

What's New

Product release notes are available at:
http://support.cadence.com/wps/mypoc/cos?uri=deeplinkmin:DocumentViewer;src=pubs;q=landing/spb172/prodList.html

KPNS

The Known Problems and Solutions (KPNS) document is located at:
http://support.cadence.com/wps/mypoc/cos?uri=deeplinkmin:DocumentViewer;src=pubs;q=landing/spb172/kpnsList.html

Downloading and installing SPB Software

Cadence software can be downloaded from:
http://downloads.cadence.com

Log in with a valid user ID and password and click the Windows tab. In the Windows tab, click the link *SPB172*.

NOTE: OrCAD customers can contact Cadence Channel Partners to obtain their software. Cadence Channel Partners are listed at:
http://www.cadence.com/Alliances/channel_partner/pages/default.aspx.

Download CD 1 of 1 and then extract the zip file into a temporary directory such as `cdnstemp`. This will leave you with a directory structure that is similar to:

```
addons folder
Autoplay folder
Disk1 folder
LibCD folder

autorun.inf
setup.exe
setup.ini
```

Complete the installation by running `setup.exe` from the temporary directory. You can install the following using the downloaded files:

- Main Installations:
  - License Manager
  - Cadence Allegro and OrCAD Products
  - Allegro Design Entry HDL – AMS Library
  - Cadence Allegro and OrCAD Client
- Optional Installations:
  - OrCAD Document Editor
  - Allegro PCB Manufacturing Option
  - OrCAD Library Builder
  - OrCAD Component Information Portal
  - OrCAD Engineering Data Management

Consult the installation guide for detailed information.

NOTE: If prompted, reboot the machine and log in with the administrator privileges login id to successfully complete the installation.

List of Fixed CCRs

- Enhancement CCRs
- Bug CCRs

Enhancement CCRs:

CCR ID	Description
165288	Need axl SKILL function to access new Undo/Redo feature
216639	NODRC_ETCH_OUTSIDE_KEEPIN is not available for Text.
313636	Need the ability to search a layer for a text object with a property with a certain value
512826	Flex board requirements. Allow two conductor layers together.
551868	Different padstacks for backdrill vias in Allegro PCB
576215	Assign net to multiple pins
579664	Request for including the panelization feature in Allegro PCB Editor
580291	Support two or more cross-sections.
586271	DRC checking to back drilled hole wall in backdrilling
586279	Ability to drive special AntIPAD and Etch spacing to backdrilled layers without swapping or modifying padstacks.
586901	testprep should not use backdrill locations
587306	DRC checking for drilled hole wall during backdrilling
589407	Hole chart and the ncdrill file header changes
610035	Add metal usage report to Allegro PCB Editor
639288	Need a function for backdrill spacing checking.
673703	Cannot edit single padstack in SiP Layout
690470	'Unmatch All' Button in Unmatched Interface window for Place Replicate Apply
719134	Need ability to add the fix property to text entities
721609	Need layer ID for backdrilled vias
732378	dxf out command should join poly and merge shapes
747110	Hotfix notification to users in Windows Client Server method
750914	Automatic Hotfix updates
773266	Check any subclass to any other subclass in constraint mode
791695	Ability to assign/reassign nets directly to multiple vias
795889	Ability to assign or reassign a via to a net
798792	Ability to assign or reassign a via to a net
813213	Exclude pins from backdrilling
817482	Auto Assign BGA pins according to SPG ratio
820332	The option “POWER_AND_GROUND” is missing within "RATSNEST_SCHEDULE" property on schematic side.
821167	Option to check for the latest hotfix and to perform a silent-install if there is a new hotfix.
829320	Allow change in antipads and potentially pads based on the layer connected in backdrilling
829325	Need a backdrill to shape spacing check
832818	Minimum stub tolerance after backdrilling for manufacturing accuracy
833836	Need for dual-sided die
851437	Include panelization feature in PCB Editor
852795	Backdrill to metal checks
853121	Ability to add a property to text

857580	Option to ignore a part in netlist but not in CIS BOM
877943	Allow Fixed property for Text as well
891678	Need panelization function
902872	Refdes control on part level
903324	Cross Section Chart should include Backdrill information
911861	A quicker way to enable the RETAIN_NET_ON_VIAS property and to change it back.
917026	Automatically add return path vias for differential pair vias
921319	A quicker way to enable RETAIN_NET_ON_VIAS property
921952	PCB Editor enhancement for return path vias
925658	Allow NODRC_ETCH_OUTSIDE_keepin to be added to text on etch layers
958003	Need the ‘Embedded Layer Setup’ option to retain Soldermask features when a component is embedded.
959434	Option to ignore a part in netlist but show in BOM
965238	Ability to suppress text DRC by NODRC_ETCH_OUTSIDE_KEEPIN
966844	Ability to suppress text DRC by NODRC_ETCH_OUTSIDE_KEEPIN
981802	Spacing constraint for backdrill and trace
982171	Backdrill should take priority over testpoint
984346	Request of spacing constraints for backdrill
986293	Ability to swap dummy embedded components
995618	Dia file should contain shrink factor and scribe line width; and cdnsip import should use these
1000832	Need FSP support for post-layout optimization in DUT flow: Pin cannot be swapped.
1019307	New model request
1029188	Exclude pins on one side for backdrill
1031658	Ability to assign or reassign a via to a net
1035425	Model request for LM5041,LM5102, and Si8503
1049913	Feature to exclude a part from going to netlist and BOM
1052639	Ability to set to 'not check topology'
1054321	Allow NODRC_ETCH_OUTSIDE_keepin to be added to text on etch layers
1059470	Ability to create a die with padstacks on both sides.
1061056	Ability to define different cross sections per region on a Flex Rigid design
1063507	Different padstacks for backdrilled vias in Allegro PCB Editor
1067435	Need a function for backdrill spacing checking.
1085152	BACKDRILL_EXCLUDE to allow exclusion by layer
1097408	Datasheet pointing to a web address in relation table opens 4 web pages on click
1119432	Missing tapers report needed
1130760	Request to include dies for embedding into a substrate, no cavity.
1132033	Place Replicate Unmatched Component Interface window - changes needed
1132757	Ability to add BACKDRILL_MAX_PTH_STUB property to via
1145687	Multiple web pages open when clicking on the relational table's datasheet link
1145691	Multiple web pages opens on clicking the relational datasheet link in CIS explorer
1146176	Need for Min_path_stub property for backdrill
1156111	Step model support to export internal layers and provide a mechanism to calculate offsets.
1163731	PDF export issue with 64-bit systems.
1172426	Support to define multiple stack-up for rigid flexible PCB

1185241	Multiple web pages are opened if pointing to the address given in datasheet of a relational table
1186350	Ability to backdrill in Allegro Package Designer editor
1221066	Cross-section chart with backdrill details
1229087	Allow backdrilling on selected pins and vias and not the whole net
1235487	Require step export to support embedded components.
1236436	Need for Min_path_stub property for backdrill
1236554	PDF Publisher needs watermark support
1243356	SiP Layout - 3D viewer does not show pad on correct layer
1252141	Allow appropriate IPC-2581 layer function enumerated list values to be selectable from Cross Section Type column
1255757	Merge the cross-section dielectric thickness with the artwork's soldermask layers.
1256413	Provide watermark support in the Publish PDF functionality
1257667	Enhancements in Refdes control annotation
1260282	Controlled annotation to be honored when placing new parts
1260422	BACKDRILL_EXCLUDE on one side
1264141	Ref Des assignment when copying and pasting components
1268307	Datasheet pointing to a web address in relation table opens four web pages
1280466	Need backdrill oversize to etch and other objects spacing constraints
1285641	Provide an option to exclude a part from netlist but include in BOM
1288192	Relational Table Link opens multiple tabs in browser
1289048	Datasheet pointing to a web address in relation table opens four web pages on click
1289592	Place replicate Unmatched component Interface window
1293543	Create Missing Taper report
1293691	Place Replicate required for managing large number of components.
1306495	Exclude a physical part form the Allegro PCB Editor netlist only
1306980	Ability to add differential pair ground via
1313167	Cross-section chart with backdrill details
1313206	Differential pair via pattern for high speed
1313599	Add property to symbol to suppress pin to route keepout DRC
1317200	Add ability to add dynamic fillets by layer.
1328035	Web links in the Relational window opens multiple tabs
1333475	Integrate Allegro Package Designer with PVS for design rule checks in PVS
1336338	Have the option to keep soldermask on symbols when they are placed embedded
1336589	Resizing directory window when saving a project
1342565	DRC option to check for backdrilled vias/pins to any copper
1346084	Need clarity for g_value for dynamicFillMode in axlDBControl
1347127	Ability to change wire profile on non-standard bond, without having to redraw it, just like regular wire bonds
1348726	View voids and boundary of a shape drawn in the internal layers only for dynamic shapes
1350614	Text labeling for SiP wire bond design documentation needs to be automated to show needed vendor info.
1362112	Toolbar customization changes are lost when switching between Allegro Package Designer L and other licenses
1365183	Include "Oblong" for co-design symbol app mode dual-pin footprint
1365895	Incremental and unconditional annotation are not consistent with Ref Des control

1372988	Define cross-section by area
1377478	Provide template JEDEC 4P/5P wire profile definitions with release install
1395684	Customizable visibility tab
1397240	Arrangement of toolbars
1399493	Request Save Project As feature
1399495	Possibility to fill "All" field while up revving old boards.
1403719	Need ability to add layers or material by region.
1407287	SiP Layout - Symbol to Spreadsheet, include option to mirror view or top/bottom view of selected component
1410958	Need solder mask opening layers for 'embedded' passives
1412043	OrCAD Professional and Place Replicate Update
1412091	Compact output from the Export command
1415639	Do not want the bitnumber to be part of the dp_name on library defined differential pairs
1417375	Capability to backdrill from the same side the component is placed
1419853	User-defined subclass for the Format Symbol
1420305	Browse window resize
1421144	Wirebond text alignment
1425415	Cross-section chart should remember last placed location
1427839	Cross-section chart should not show '*' when options turned off
1428267	Change of number of heterogeneous parts does not copy properties
1428567	Require rotation option for GDS stream out
1430300	OrbitIO needs to support multiple pin pitches for package creation
1430550	When using Force Update or Update to Smooth in Global Dynamic Shape Parameters incorrect report name is specified
1430582	Shape dynamic state report name inconsistencies
1430971	Allow the standard reports from Tools - Reports to be saved with semicolon or pipe as separator instead of comma
1430986	Allow the standard reports from Tools - Reports to be saved with semicolon or pipe as separator instead of comma
1431233	Die abstract import filters
1432884	Need to have Personality UI to be in sync with DB capabilities
1433050	Add width by layer to drawing summary report
1434940	Toolbar customization resets
1435175	Drill symbol message error
1435961	Unmatch all option for Place Replicate Unmatched Component Interface
1435989	Resize Place Replicate Unmatched Component Interface window
1436077	PCB Editor error when item to be changed already matches
1436642	Drill to Cline DRC rightly flagged, but bubble not working around the Drill when slide/cline
1437663	Support IOPAD type for File - Export - Text
1438013	Detailed description is required for Filter in Constraint Manager
1438815	Support probe pins in I/O drivers
1441599	Add DRC checks for Molding cap to Bond wire and die in the SiP 3D Viewer.
1442010	Pop up message for Round Off Warning when changing User Units
1442032	Username variable for Windows
1442579	Change the Select Directory Window to current browse window in new Windows Operating system.
1442704	Add properties to TEXT object
1446656	Add package size, DFA layer, and DFA_DEV_CLASS property in

	BGA/DIE Generator
1447317	Allow specifying ‘pin pitch’ when exporting symbol spreadsheet for cases where pins are not aligned in rows or columns.
1447396	Add the ‘Step_name’ option to the IPC2581_UserData.txt file
1450446	STEP model support to export internal layers
1450892	Deletion of logical pins in Part Developer
1450937	Soldermask for embedded parts in cavities
1450946	Embedded components should have paste and soldermask layer
1454248	Need more options for CTE Compensation.
1454541	Merge shape command in the pop-up menu
1455533	Need to write out the search results of Find by Query
1458316	Need a message to alert users if possible backdrilling conditions are missed out.
1458355	Change the ‘Total Unconnected Pins’ to ‘Total Unconnected Pin Pairs’ in Unconnected Pins Report.
1458706	No matching function for overloaded message when running 'XMATIC_XML2DSN' command
1464918	Ability to add BACKDRILL_MAX_PTH_STUB property to via
1467267	Enhance probe pin support
1469166	Shape Edit Application Mode to include parameters from right-click operation on Shapes.
1469788	Spacing calculation for shapes calculating wrong values
1470062	Allow defining the value of ‘Min. Distance from pad edge’ in the User Preference editor
1471794	Ability to Z-copy only C-line segments instead of entire cline.
1471821	Ignore one of the duplicate outlines and provide a warning message when exporting IPC-2581
1472865	Which property sets the default Logic Import directory path?
1473718	Need Soldermask subclass for Embedded Components Geometry class
1474173	Oblong bump rotate along with the die edge
1475606	Window select (Polygon or rectangle shape) to select specific Cline elements.
1475613	Selection of Find by Query should take multiple filters
1476401	Need the ability to reduce the size of the Visibility, Find Filter, and Options windows.
1478248	Need to change the edge factor in cross section in Allegro PCB Designer with High-Speed option
1478260	Fix/Unfix should support new selection types – lasso, path, and polygon
1479246	SiP Layout DIE stack editor (DSE) - add up/down arrow in form to reorder die in stack
1481074	Die shrink relative to symbol center instead of bump center
1481559	Request for function "axlIsPointOnLine"
1482940	Add more classes to support rigid/flex users subclasses
1483508	Cross probing is not working if user name has space
1483821	Provide an option to exclude a part from netlist but include in BOM
1484855	Add ability or improve the slide shoved preferred when clines have arcs.
1485306	Alphabetically sort the film elements in artwork
1486973	Ability to rename the element ‘BOARD’ while exporting STEP file from Allegro PCB Editor

1486979	Step model support to export internal layers from Allegro PCB Editor
1487148	Enable return path vias for single-ended nets
1487149	Backdrill should have an option to add a route keepout to the drilled out via stubs
1487880	Incorrect DictionaryExtention setting in pstcmdb.dat for MOUNT on running Export Physical with user settings
1492012	Disable "Swap Properties with pins" option by default for Swap Pins command
1493910	Assigning only character for drill symbol with Drill symbol figure
1494011	NTC Model to give better simulation results
1494420	Cannot select new "Snap pick to" point after "Arc w/ Radius" command
1494797	Provide information about the file pstdmlmodels.dat generated by packager
1495023	Make Select Directory window resizable or make it aligned with current Windows dialog boxes.
1495756	Adding/removing Layers does not follow ELIC Rules correctly
1495911	Find By Query for general objects
1496769	OrbitIO should provide mil as normal distance unit
1499400	Support zcopy of cline segment
1502493	Allegro Package Designer crashes on generate package report
1503126	When moving a package ball, contact pin needs to move together.
1503559	Need a way to move shingled stacked dies incrementally within the Die Stack Editor.
1506815	PCB Editor should display DRC for non-plated padstack with connection
1507993	Place replicate needs an ‘unmatch all’ button
1510157	Disable DRC errors detected when user voids a via by manual void.
1510346	Add watermark in schematic
1510443	allegro.cfg not opening in correct format (or tool)
1511627	Step model support to export internal layers from Allegro PCB Editor
1514348	DXF_IN edit view layer should sort layers in alphabetical order
1515094	IPC-2581-B, all dielectric layers defined as DIELCORE
1517708	Ratsnest tooltip when using shape edit application mode
1518750	Compose From Geometry offsetting die
1519462	Lock the Toolbars menu all around the windows
1519464	Viewer assigns color for differential pairs
1520204	Copy and paste to Package Properties Spreadsheet ignores pin types even though GUI shows them correctly
1527307	Waived DRCs restored after DRC update
1529161	The "NO_WIREBOND" property is not available in Symbol Editor
1530350	Shape symbol should support void in a shape
1531270	Ability to assign or reassign a via to a net
1531663	Class to class form behavior needs fix
1532829	Both ‘Via List by Net” reports contain bond fingers, which they should not.
1532853	Request that Bond Finger statistics be added to the Summary Drawing Report
1533412	Ability to add subclasses to Embedded Geometry layer.
1534035	Interactive select mouse cursor can change to arrow
1534076	Differentiate assigned net from unassigned net.
1534146	Ability to set default output path for IPC2581, IDF, and IDX export.
1534159	Adding customized backdrill property to a symbol/pin/nets
1538119	Ability to create bond finger label text strings in one pass

1538657	Backdrill Setup and Analysis form: Add Enable/Disable All Layer Pairs option to pop-up under the Enable column
1539053	Enable Custom Property values to be upreved along with symbol during the symbol uprev process
1539717	Plating traces do not need fillets
1539827	Need Redo and Undo commands for user-defined skill commands
1540196	Edit - Copy should allow copying the symbols classified as IC.
1542952	Disable Function key F1 to launch help
1542993	Progress bar shown during Import pages is misleading
1544686	Mirror custom padstack layer while moving die from top to bottom
1546042	Alternative script file extension
1546725	Skill function to modify layer properties
1547265	On rotating a component by 45 degrees, the DRC marker appears
1547524	Minimum possible backdrill depth
1547629	Provide an option for entering only upper-case input for signal names
1548526	Ability to map etch, pin, and vias subclasses for IDX export.
1549650	Alternative extension for Allegro script files, for example script, so anti-virus does not report this

Bug CCRs:

CCR ID	Description
20785	Exclamation mark corrupts Capture library
1185139	Annotation with Refdes control not working correctly
1243476	The ‘axlGetFuncKey()’ SKILL function is not working using the documented syntax
1266464	Controlled annotation does not work in multiple pages in simple hierarchical design with two levels
1306995	Copying existing part using TCL crashes Capture
1310865	PSpice AA Monte Carlo with temperature sweep has more than one measurement crashes
1322242	Using ‘add connect’ along with ‘replace etch’ option causes the tool to slow down for certain constraint nets
1336443	Net name not retained for pins that are not connected to clines or vias
1349603	Missing layers during place manual - Component by refdes
1365668	Long bump master name cannot be completely shown
1369199	Irregular shape voids - Fillets proximity to the shape make its boundary irregular
1369743	Invalid character for Location are getting backannotated
1371668	Naming an offpage port causes Capture to crash
1375001	Route contour error
1377596	Capture gives incorrect error message while deleting a property in Property Editor
1400221	Convergence errors when simulating
1403005	Symbol's silkscreen disappears during placement
1406551	Capture crashes while customizing toolbar
1407079	Variant Editor does not allow use of subgroup names as variant names
1410994	Library not locking - OLBlck file is not created
1416781	3D viewer shows two overlapping shapes for Round SMD Pins on Bottom Layer
1418391	Crash in Probe with Marching set to ON(unsupported) in Digital design
1420521	Trace Colors are not as per the expected behavior
1428749	CIS Part Manager: 'Update All part Status' showing incorrect result for database resistor
1429663	Tool crashes after running the ‘Launch the Replace Path in Cache’ TCL utility
1430251	Quickplace placing symbols outside of a polygon shaped room
1430772	SiP Layout: Interactive Layer Compare problem
1432237	DFA_UPDATE adding shape beyond pins
1434225	Issue with netlist and MECHANICAL CLASS
1438981	Die text-in wizard step 3A is misleading in that it appears you can change the pad shape and dimension of an existing pad
1442676	Incorrect grammar in the variable description for icp_allow_adjacent_conductors
1444147	Data tip populate pin number for both pin number and pin name
1446248	Wrong Impedance with the symmetric cross-section
1448461	Import techfile form remains empty if browsed from other than local

	directory
1449191	Some clines appear to be highlighted
1451229	Allegro Package Designer: layer compare does not work correctly
1451766	License error message should indicate which license is required
1457080	Dynamic shape not updating correctly and results in false ‘Drill Hole to Shape Spacing’ DRC error.
1457543	XML export does not export occurrence values
1459697	Focus not in PCB Editor command window if the script contains scriptmode, invisible, and color192 commands
1463495	Wrong route keepin to shape DRC
1464865	For identical nets, topology in DE-HDL Constraint Manager is different from the topology in PCB Editor Constraint Manager
1467619	Glossing Controller Form could not be opened after running the ‘Undo’ command
1469776	Dynamic shape not clearing manual void completely
1469808	Custom color lost during the highlight-dehighlight operation on via or pin
1470458	BGA text-in wizard places the refdes and assembly outline on bottom and the padstack on top.
1471173	Class-to-Class object should not show inherited values
1471226	Shape has voids that follow the fillets until the ‘Gloss’ command is executed with no parameter changes
1471232	Shape update shows notches in boundary.
1471658	Dynamic Glob does not work well in child_interface second time
1471759	Autoconverge option is always active
1472933	Cannot locate the ‘NO_MOVE’ property for components in Allegro PCB Editor
1473691	Getting ORPSIM-16152 and ORPSIM-16368 errors
1478200	PCB Editor flags error ‘Low On Available Memory’ and then crashes
1479175	Selecting ‘Show Element’ should not cause an embedded component layer move even if the Die Stack Editor setup is wrong.
1479324	Capture crashes with custom DRC when project window is docked to the left
1479573	Inconsistency with Bus as Member in Netgroup
1481870	Die abstract rdl flight lines not displaying in SiP Layout
1484222	APD/SiP - unsupported prototype - Layer Compare not finding missing cline segment between two design files
1486227	‘Check high speed props syntax’ DRC reports error for correct value of RATSNEST_ SCHEDULE property
1486980	Allegro viewer reports ‘command not found: symbol_check’ when selecting the unplaced symbols color swatch.
1487906	Two Analog DMI dlls do not get loaded for the same design
1488362	Object Filter dialog changes Object Type items for every click of the ‘Apply’ button.
1491912	Sorting in CIS BOM is not working properly
1492812	The ‘Custom Smooth’ command is creating DRCs
1494363	The place manual icon is grayed out in the OrCAD menu
1494403	ZCOPY with small offset - the copied shape is corrupted.
1496855	The default value for Soldermask to Soldermask spacing is not transferred using Tech files from Constraint Manager.
1500586	PSpice: ‘File – Save as’ does not save file with .cir extension
1500601	No warning message appears on clicking the ‘View Warning’ button after

	modifying a split part
1501212	Invalid number error message needs more detail
1502300	Pin to pin short DRC is not reported when connection is through a NetGroup block
1503592	Sliding arc cline causes irregular and unpredictable voids to be created
1504427	Undo operation opens all the pages
1505264	Need Tcl command to prevent execution of last saved query and restart CIS explorer
1507502	Variant name is not getting added to crystal report
1508337	Leaving Constraint Manager open causes Application Mode Pre-Selection issues on Linux
1508603	Place Manual icon is grayed out in OrCAD PCB Editor
1508970	Performing replace device hangs OrbitIO
1510901	Getting ORPSIM-16152 and ORPSIM-16368 Errors
1511016	Shapes not updating after netlist
1512338	Shape broken in Allegro Package Designer
1513645	Wrong Cutout in dynamic copper shape
1513684	Place Manual icon is grayed out in OrCAD PCB Editor
1513828	Differential pair uncoupled length calculation error
1514942	AIR not permitted in stackup
1515046	IPC-2581-B Soldermask layers defined twice
1516790	Description for axlISProductStarted includes incorrect command name
1518107	Backdrill passes become corrupt and no longer report ‘Start Layer’ in the Backdrill Setup form
1520487	Error while simulating transformer in Lite mode
1521740	Place Manual icon is grayed out in OrCAD PCB Editor
1521871	Constraint Manager from DE-HDL allows creation of layer set name with illegal space without warning
1522902	Import – DXF: Text label and Macro block in dxf does not match the converted OrbitIO database.
1525971	A top-level MENUITEM added in the custom menu file to execute a command is not working
1526133	Shape Application Mode: PCB Editor cannot exit the ‘void’ command run from the ‘Add Void’ pop-up menu.
1527501	Switch to 'Query' tab runs last executed query
1527570	Capture crashes when running custom DRC
1529921	IPC-2581 rev B Invalid instantiation of <PinRef> as a child of the <Pad> element is out of sequence.
1530139	OrCAD PCB Designer: The ‘Place – Manually’ button in Toolbar is inactive (gray)
1530466	Incorrect warning for film name character limit
1533386	Min and Max values shown for Timing vision in datatip are wrong
1534841	The skill command ‘numOpenFiles()’ crashes PCB Editor
1535667	Starting PCB Editor on Linux sometimes opens a window with a white background in addition to the editor window
1536101	Drill file is generated with is missing codes
1536713	File - Viewlog looks for the incorrect brd2odb log file
1539027	Disabling the Advanced Object filter, ‘Always show members/Pin Pairs’, suppresses Layer Types under Physical Domain
1539212	Deleting a differential pair automatically recreates it

1539843	Bump overlapped while moving it
1539988	Loadstrokes is not recognized as a DE-HDL directive
1543331	Constraint Manager flashes inactive editor window while refreshing
f1545483	Many NPEs when replacing one BGA with another
1546141	Shapes missing from Artwork
1546721	Running Auto-Interactive Trunk Route on a bundle with odd angle flow segments causes a crash
1548318	The ‘Create package’ command creates package size incorrectly
1549105	'Stream out' fails with the message: 'Request to terminate detected. Program aborted'
1550508	Allegro PCB Editor child windows hide in the background
1550982	Contact pads for bumps are not following the ports in the bumps
1551713	Hole to hole DRC between via and pin are not displayed
1552336	The ‘Show Rats Between’ command does not show rats between some of the devices
1553027	Allegro PCB Editor display freezing very frequently - canvas not responsive and turns white.
1554288	Adding a menu separator using skill function ‘axlUIMenuInsert’ causes PCB Editor to crash